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PREFACE

Symposium INFOTEH®-JAHORINA is continuation of the International symposium JAHORINA that was held last time on April 1991. The main organizer of the Symposium is the Faculty of Electrical Engineering East Sarajevo and the co-organizer is the Faculty of Electrical Engineering Banja Luka. The Symposium is supported by The Faculty of electrical engineering, Belgrade, Serbia and Montenegro, the Faculty of electronics, Niš, Serbia and Montenegro, the Faculty of technical sciences, Novi Sad, Serbia and Montenegro.

The goal of the Symposium is multidisciplinary survey of the actual state in the information technologies and their application in the industry plants control systems, the communication systems, the manufacturing technologies, power system, as well as in the other branches of interest for the successful development of our living environment.

During the first Symposium INFOTEH®-JAHORINA 2001, that was held on 12-14 March 2001 in the hotel Bistrica at Jahorina, 53 works have been presented, six companies presented their development and manufacturing programs in telecommunications, power electronics, power systems and process control systems. More than hundred participants took part in the Symposium working. Round table about potentials and possibilities of economic cooperation between Republic of Srpska and FR Yugoslavia has been held during the Symposium, regarding successful appearance at domestic and foreign market.

During the second Symposium INFOTEH®-JAHORINA 2002, that was held on 25-27 March 2002, 76 works have been presented, and five companies presented their development and manufacturing programs. More than hundred and thirty participants took part in Symposium working. Round table entitled "Reforms in high education – step forward to the European University" has been held during the Symposium.

The third Symposium INFOTEH®-JAHORINA 2003 was held on 24-26 March 2003. More than hundred and fifty participants took part in the Symposium working, coming from Serbia, Montenegro, United Kingdom and Republic of Srpska. At the Symposium 73 papers have been presented and nine student papers. Four companies presented their development and manufacturing programs. Round table entitled "New Technologies and Industrial Production Capabilities for small Countries in the Transition Process" has been held during the Symposium. All papers are presented in symposium proceedings, CD version.

The fourth Symposium INFOTEH®-JAHORINA 2005 was held on 23-25 March 2003 in the hotel Bistrica at Jahorina. The main topics of the Symposium were: Computer science application in control systems, Information-communication systems and technologies, Information system in manufacturing technologies, Information technologies in power systems, Information technologies in other branches of interest. More than hundred and seventy participants took part in the Symposium working, coming from Serbia, Montenegro, Republic of Srpska, Federation of Bosnia and Herzegovina, Croatia and Macedonia. At the Symposium two invited papers, eighty and three papers and three student's papers have been presented. Three companies presented their development and manufacturing programs. All papers are presented in symposium proceedings, CD version (ISBN-99938-624-2-8).

The fifth Scientific – Professional Symposium INFOTEH – JAHORINA was held in 2006, March 23 – 25. The Symposium was dedicated to the 150th anniversary of Nikola Tesla's birth. It was the first official manifestation in the Republic of Srpska dedicated to this jubilee. The university character of this traditional international scientific and professional gathering was reflected in a complete and multidisciplinary approach to the discussion of themes within the discussion forums, lectured and presentations. The support to the Symposium was given by the representatives of the Government of the Republic of Srpska, joined bodies of Bosnia and Herzegovina and local municipalities. There were exposed 137 papers which passed the review, and 172 guests of the symposium were registered.

The sixth Scientific – Professional Symposium INFOTEH – JAHORINA was held in 2007, March 28 – 30. and it was dedicated to global warming and its side effects. The opening lecture by call was held by Ana Pavlović, physicist of meteorology and living environment modeling from Faculty of Technical Sciences, University of Novi Sad. The support to the Symposium was given by the representatives of the Government of the Republic of Srpska, joined bodies of Bosnia and Herzegovina and local municipalities. 160 papers were written for the Symposium, and 131 of them were accepted, including 6 students' works.

The seventh Symposium INFOTEH - JAHORINA 2008" was held in Jahorina, March 26 – 28, 2008. The Symposium was dedicated to the life and work of Milutin Milanković, and Professor Milić Stojić, Ph. D. from the University of Belgrade had an extraordinary introductory lecture about the life and achievements of this great Serbian scientist. The university character of this traditional international scientific and professional gathering was reflected in a complete and multidisciplinary approach to the discussion of themes within the discussion forums, lectured and presentations. The support to the Symposium was given by the representatives of the Government of the Republic of Srpska, joined bodies of Bosnia and Herzegovina and local municipalities. The Symposium was opened by the inspiring speech of the academician Rajko Kuzmanović, the President of the Republic of Srpska. Over 220 papers were written for the Symposium, and 169 of them were accepted.

This issue of international journal "Electronics" includes the most interesting papers selected from the seventh Symposium INFOTEH®-JAHORINA 2008.

I would like to invite all readers of the "Electronics" journal to take active participation at the next Symposium INFOTEH®-JAHORINA. Updated information can be obtained from the Symposium web page: http://www.infoteh.rs.ba.

Professor Božidar Krstajić. Ph. D.

Chairman of the Organizing Commitee, INFOTEH®-JAHORINA 2008

Biography of Prof. Božidar Krstajić, Ph. D.

Božidar M Krstajić was born in Žabljak, Montenegro, on July 7, 1948. He graduated at Faculty of Electrical Engineering in Sarajevo in 1972. He finished his master studies at University of Zagreb in 1977, and finished his doctoral studies in 1986 at University of Sarajevo. In September 1972, he started working as a teaching assistant at Faculty of Electrical Engineering, University of Sarajevo. In 1986, he was elected in the title of Assistant Professor, and in 1989 in the title of Associate Professor on the subject "Electromagnetics". From October 1994 to October 2000 he worked as a guest professor at Technical University in Munich, at High Voltage Institute. In that period, he worked on the development of mathematical models and software modules for modelling, calculation and visualization of electromagnetic fields in high voltage devices. The Asea Brown Boveri AG Research Center, Heidelberg, used those newly created modules in a software package POLOPT®. He led research projects supported by international organizations and commercial enterprises. His current research interest involves the computer-aided design of electromagnetic devices. Prof. Krstajić is one of the authors of monograph "Integral Methods for the Calculation of Electric Fields, for Application in High Voltage Engineering", Scientific Series of the International Bureau Research Center Juelich - Germany, 1992, ISBN 3-89336-084-0. He is also author of 2 books, 2 monographs and over 10 scientific journal papers, 25 conference papers and 50 research projects. Since 2003, he has been elected to be a Full-time Professor in narrow scientific field "Theoretical Electrical Engineering". He was the supervisor of nearly 20 Diploma engineering thesis, 4 Master thesis and 1 Ph.D. thesis.

From 2002 to the present moment, Prof. B. Krstajić is the dean of the Faculty of Electrical Engineering, University of East Sarajevo.

IMPLEMENTATION OF AN ULTRA-LOW POWER THERMOSTAT WITH SLOPE A/D CONVERSION

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Abstract: *This paper presents an implementation of an ultra-low power thermostat. Temperature measurement is accomplished with slope A/D conversion: discharge time intervals of a capacitor charged to a reference voltage, through a reference resistor and through a thermistor are compared and used for calculation. The device is based on microcontroller MSP430F413 (Texas Instruments) that has internal analog voltage comparator and LCD driver (7-segmented LCD is used for user communication). This is ultra-low power microcontroller, which greatly increases battery life. It also supports in-circuit programming of flash memory via the JTAG port. NTC thick-film segmented thermistor, used as a temperature sensor, has been developed and fabricated and then calibrated for this particular application. The thermostat is built for temperature range from 10 ℃ to 90 ℃, which enables various useful applications.*

Keywords: *Thermostat, NTC thermistor, Microcontroller.*

1. INTRODUCTION

Thermostats are devices used for regulating the temperature of a system, so that the system's temperature is maintained near a desired setpoint temperature. The thermostat switches heating or cooling devices on or off as needed to maintain the correct temperature. Different types of thermostats are produced, depending of the type of used sensor. They can be based on bi-metal mechanical sensors, electrical thermocouples or electronic thermistors.

Digital thermostats are replacing classic analog ones. They are fast, precise and efficient. They can easily be connected to other digital devices, and therefore have a much wider field of application. Different types of thermistors are usually used as temperature sensors in the thermostat realization.

Bulk thermistors based on Co, Mn, Cu, Fe oxide systems have been known for many decades [1]. New technologies enable production of faster and more precise film thermistors, which ca be used as sensors. Because of their small thickness, compared to bulk thermistors, they have faster temperature response. Film thermistors are fabricated in different shapes and sizes so that the different applications can be enabled. The goal of this work is application of newly developed thick-film segmented NTC thermistor for practical realization of modern digital ultra-low power thermostat.

2. NTC THERMISTORS

NTC thick-film thermistors are made of ceramic materials, based on a mixture of oxides chosen from the elements Mn, Ni, Co, Cu and Fe. By varying the composition and the size of the semiconducting elements, resistance values between 1Ω and 1MΩ at room temperature can be achieved with temperature coefficients lying between -2% and -6,5% per °C.

All NTC thermistor materials are prepared by heat treating a mixture of metal oxides to a temperature around 1100-1200°C so that the oxides combine chemically to form compounds which exhibit semiconducting electrical properties. All of these compounds possess a common crystallographic structure which is termed the spinal structure due to its similarity with the mineral spinal ($MgAl_2O_4$). This spinal structure may be represented chemically by the formula $A^{2+}B_2^{3+}O_4$, where A represents one or more divalent metals which form oxides of the type AO, and B represents one or more trivalent metals that form oxides of the type B_2O_3. Semiconducting properties of materials with the spinal structure are described by a 'hopping' mechanism in which charge carriers 'jump' from one ionic site to the next. It has been determined empirically that electrical conduction will occur if ions of the same element, but of different valence, are present on B-sites. Furthermore, these ions must differ in valence by one unit only. The conductivity of the material is determined by the number of ions capable of either donating or accepting electrons in the electron transfer. In order that an electron can escape from the positive charge surrounding the ion, it must possess a certain minimum energy, which is called the activation energy of the hopping mechanism. The total number of electrons taking part in conduction will depend upon the number of available electrons whose energy is greater than a certain minimum transfer energy. Hence the energy of an electron is primarily temperature dependant; the number of transfer electrons is growing with temperature increment.

For practical thermistor materials a plot of $\log\rho$ against 1/T is found to give lines which are straight enough for most purposes. However, it has been found that a good fit to practical values can be achieved by using the empirical relationship:

$$\rho = \rho_\infty \exp\left(\frac{q}{k(T+\theta)}\right) \tag{1}$$

where ρ_∞ is infinite temperature resistivity, k – Boltzmann's constant, q – activation energy of the hopping mechanism, θ - small constant expressed in degrees Kelvin.

Thermistor's characteristics can be assorted in two groups. The first group includes semiconducting material characteristics with resistivity-temperature curves. The characteristics in the second group depend on shape, size and the way the thermistor is mounted, and they are represented by voltage-current curves, time constants and dissipation factors.

A low temperature NTC thick-film paste NTC 3K3 95/2 with nanometer particle powder (Mn, Ni, Co, Fe)$_3O_4$, 4% of glass binder and organic vehicle was developed in Iritel A.D [2]-[4]. Paste was screen printed on alumina substrate and Ag epoxy electrodes were printed on the top of the NTC layers. The segmented thick-film NTC thermistor,

which can be seen in Fig.1, was fabricated to be used as the temperature sensor in realized thermostat.

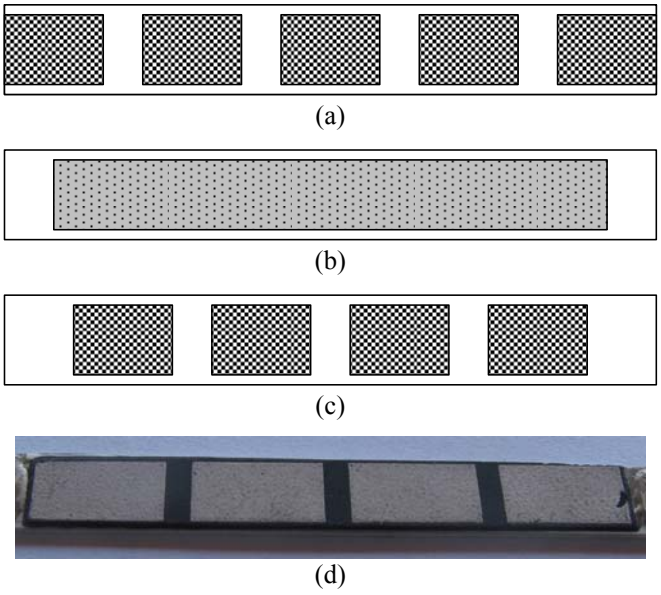


Fig.1. *Segmented thick-film NTC thermistor: (a) bottom electrode, (b) NTC layer, (c) top electrode, (d) segmented thermistor construction.*

3. SLOPE A/D CONVERSION

Realized thermostat is based on slope A/D measurement of a resistance, which can easily be implemented with MSP430 [5]. Slope A/D conversion is implemented with MSP430's on-chip comparator and timer, rather than a standalone ADC module. The technique is based on the charging/discharging of a capacitor with a known value. The number of clock cycles required to discharge the capacitor is then counted. Longer discharge times indicate larger voltages. The voltage is derived from the discharge time using a standard equation for capacitor discharge. Many techniques can be used to measure resistance. Unlike voltage measurement, where the key relationship is between voltage and time while the resistance is constant, the key relationship in resistance measurement is between resistance and time, while the initial voltage remains constant. The R/t relationship is linear, which means the calculation is easier and less-costly to implement in a microcontroller than for the exponential V/t relationship.

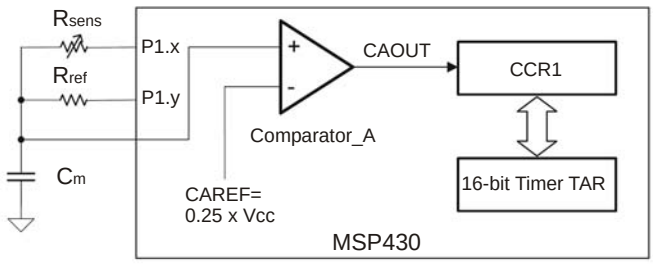


Fig.2. *The principle of resistance measurement*

Fig.2 shows the hardware configuration of a slope A/D resistance-measurement implementation using the MSP430. This circuit measures the resistance of R_{sens} by discharging capacitor C_m through it. To measure R_{sens} resistance value, capacitor C_m is first charged to the digital I/O high voltage ($V_{OH} \cong V_{CC}$) by outputting a high on either P1.x or P1.y. After configuring the timer, the capacitor is discharged through R_{sens} via P1.x by outputting a low level voltage. At the start of capacitor discharge, register TAR is cleared, and the timer is started. When the voltage across capacitor C_m reaches a comparator reference value V_{caref} of $(0.25)\cdot V_{CC}$, the negative edge of the comparator output CAOUT causes the TAR value to be captured in register CCR1. This value is the discharge time interval t_{sens}. The process is repeated for the reference resistor R_{ref}, which will be used to translate t_{sens} into the resistor value R_{sens}. C_m is given time t_c to charge, where t_c is between 5τ (for 1%) and 7τ (for 0.1%), where $\tau = R_{ref} \cdot C_m$. The value within this range depends on the accuracy required.

From basic circuit theory, the voltage across the capacitor C_m discharging through the resistor R_{sens} is:

$$V_{caref} = V_{CC} \exp\left(\frac{-t_{sens}}{R_{sens} C_m}\right) \tag{2}$$

The only unknown value in Eq. 2 is R_{sens}, which means R_{sens} can be calculated using this equation. However, it depends highly on the accuracy of C_m, which is a problem since most capacitors have relatively wide tolerance. Another problem with Eq.2 is that it involves an exponential calculation, which is expensive either in execution cycles (if calculating) or memory (if using a lookup table).

An easy way to solve both of these problems is to measure the discharge of a reference resistor R_{ref} attached to the same capacitor, and using the resulting value to normalize R_{sens}.

If C_m is discharged through such a resistor R_{ref}, the new equation would be identical to Eq.2 except with the new values of R_{ref} and t_{ref}. Since V_{caref} is equal in both cases this equation can be simplified and expressed in the following form:

$$\frac{R_{sens}}{t_{sens}} = \frac{R_{ref}}{t_{ref}} \tag{3}$$

This is the calculation used in most slope A/D resistance-measurement applications.

4. THERMOSTAT REALISATION

Thermostat is based on Texas Instruments' MSP430F413 microcontroller. It is a new generation microcontroller which incorporates 16-bit RISC CPU, memory (8kB + 256B Flash, 256B RAM), peripherals, flexible clock system [6]. Built-in analog voltage comparator and various timers make it ideal for precise instrumentation. It is an ultra-low power microcontroller designed especially for portable battery fed devices.

User communication is realized by three buttons, connected to interruptible Port1 pins. Interrupt is generated on a rising edge of input signal. These interrupts eliminate need for other keypad drivers with keypad scan and bebounce functions.

A 3.5-digit 7-segmented numeric LCD is used for display. MSP430 incorporates LCD driver module, which generates all needed segment and common signals, thus simplifying the device's hardware. LCD controller has

internal memory with information of all active segments. Static and four multiplexed types of LCDs are supported. Static LCD is used in this application, as there are enough output pins to address each display segment.

Built-in analog voltage comparator is used for temperature measurement, as it has been described in the previous section. The output of the comparator can be used with internal filtering in order to reduce errors associated to comparator oscillation. Timer_1 running in capture mode is used to measure time intervals in process of slope A/D conversion.

Basic_Timer1 is used for real-time clock functions and is configured to generate interrupt each second. All functions, except button generated interrupt service routines, are being called after this interrupt. Another important function of Basic_Timer1 is generation of LCD control signals.

Setpoint values are stored in flash memory. All data stored in this memory is saved after power cut-off or reset.

MSP430 microcontroller family has the ability of in-circuit programming of the flash memory module via built-in JTAG interface. Verification of both software and hardware is possible using JTAG interface, as the program that is being monitored, is executed on the device itself, not on a simulator. Bootstrap programming is also supported [7].

As it was mentioned before, MSP430 microcontrollers are designed for ultra-low power applications and use different operating modes. There is one active and four low power (sleep) modes. When entering one of these sleep modes, some of the system components (peripherals, oscillators, CPU) which are not currently used are disabled, in order to minimize current consumption. Wake up is possible through all enabled interrupts.

Electrodes of NTC segmented thick-film thermistor, which is used as a temperature sensor for this device, are made of silver epoxy paste and do not allow soldering. Conductive contact paste has been employed on the two terminal electrodes of the thermistor. Conductive wires were submerged in the paste, and left to dry and solidificate. After this, solid contact has been made and other free endings of these wires were soldered on the auxiliary board. This board is mounted beneath the primary board and the sensor is connected to the device by two conductive wires as can be seen in Fig.3.

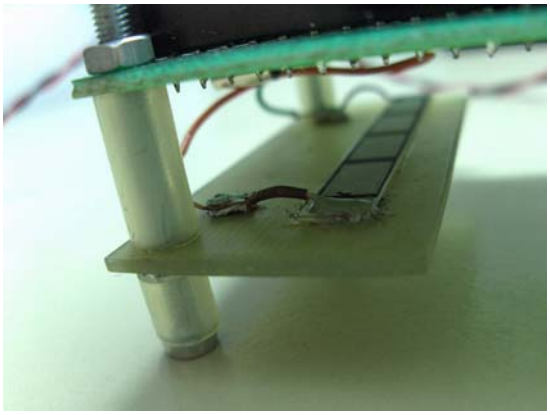


Fig 3. *Segmented thermistor mounted on the auxiliary board*

Thermistor calibration was done by exposing the thermistor to various temperatures and measuring resistance on its terminals. Standard digital multimeter was used for this measuring. The lowest satisfactory precision is of only 0.1kΩ, as the thermostat is supposed to react to temperature changes of 1°C. Measurement was done in the temperature range from 10°C to 90°C, in steps of 10°C. All other values are interpolated between measured values, and the final calibration curve is shown in Fig.4. These values are stored in a lookup table in a code section of the program code.

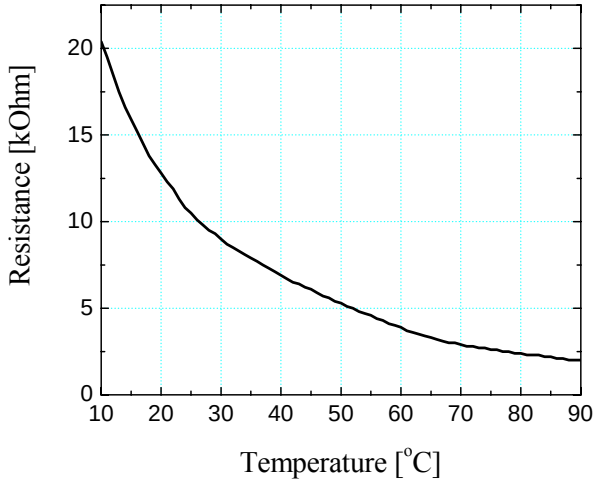


Fig.4. *Resistance-temperature calibration curve*

Designed PCB's top and bottom sides are both shown on Fig.5 and Fig.6, whereas Fig.7 shows complete electrical circuit of the realized thermostat. Complete device hardware realization is illustrated in Fig.8 where the LCD shows current ambient temperature.

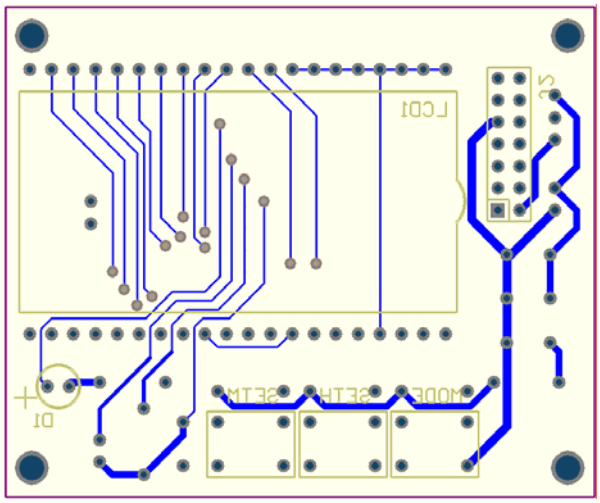


Fig.5. *Top view of the PCB*

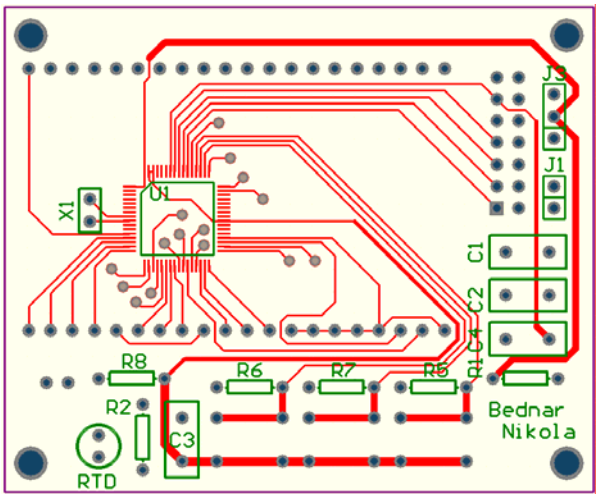


Fig.6. *Bottom view of the PCB*

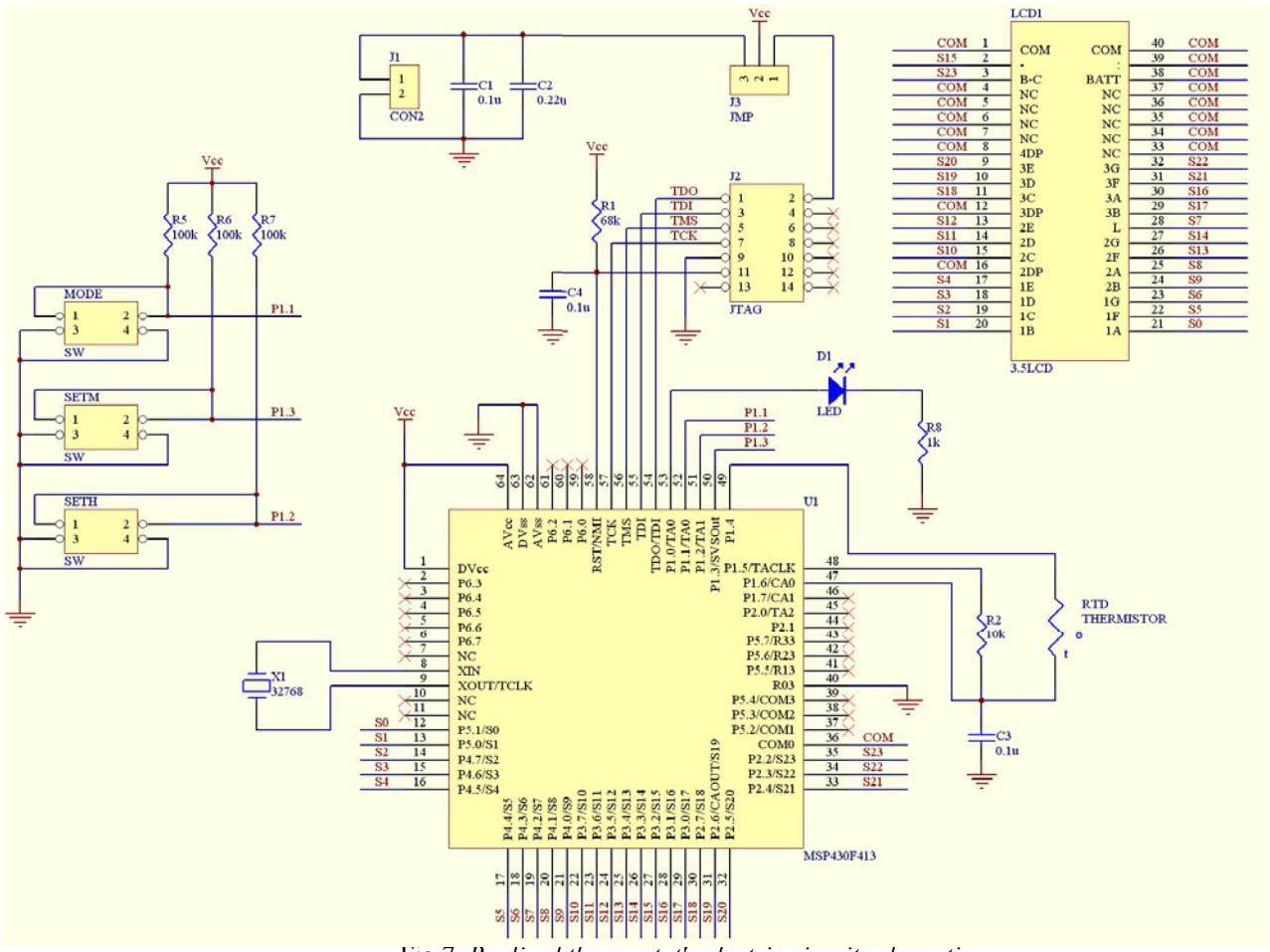
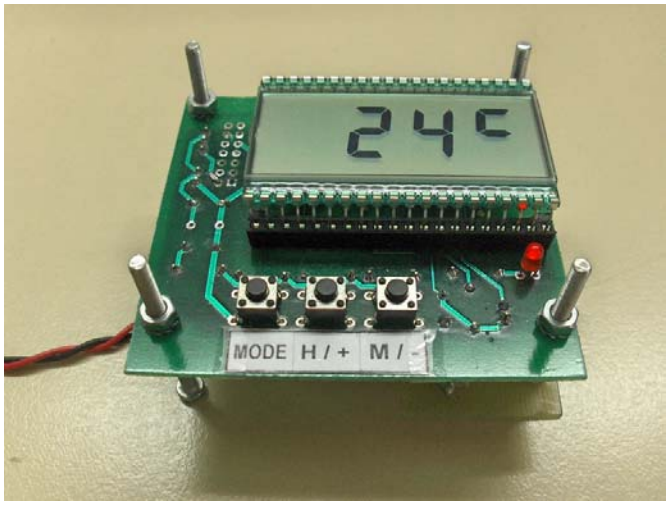


Fig.7. *Realized thermostat's electric circuit schematic*



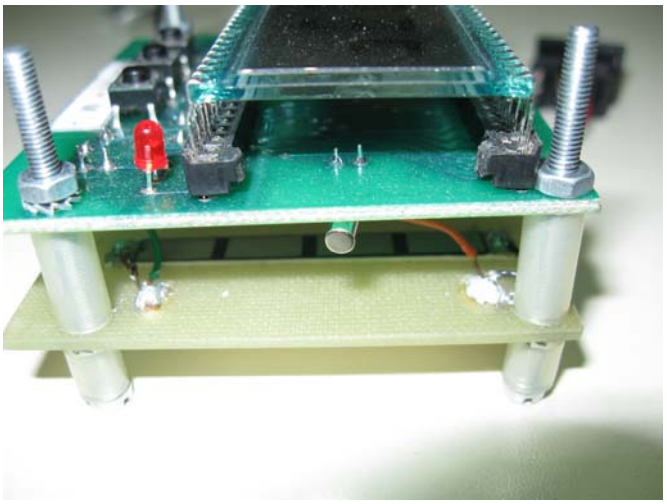


Fig.8. *The view of realized thermostat*

5. IMPLEMENTED SOFTWARE

Complete software was written in C programming language. After the initialization, program flow enters the endless loop. Timer generates interrupt periodically every second and seconds counter is being incremented. Main program loop (Fig.9) records this event and measures the thermistor's current resistance which is then used for calculation of temperature value. This result is being compared to the desired setpoint temperature and if it is lower than this value, a heater is switched off (status of the heater is indicated by the LED in this realization). The device can operate in one of four modes, selectable by MODE button. These modes are:

- Thermometer. Current temperature is being measured and displayed on the LCD.
- Setpoint. Setpoint temperature is selected using SETH/+ and SETM/- buttons.
- Time. The real-time clock is displayed on the LCD. Time can be selected by pressing SETH/+ button (increments hours by one) and SETM/- button (increments minutes by one). If the time has not been set, time that passed since the last device reset will be shown on the LCD.
- Seconds. The device simply counts seconds and displays them on the LCD.

6. CONCLUSION

In this work a realization of a digital thermostat has been presented. All earlier stated MSP430 microcontroller's features make this solution one of the more efficient ones. It is cheap, easy for installation, programming and maintenance, highly functional, and easy improvable. Serial communication between the device and a personal computer could be easily accomplished, so that the measured temperature could be monitored and the desired setpoint temperature could be set via a computer. The thermostat should be modified for real-life appliance by changing the way the sensor is mounted. If the realized thermostat is supposed to control air temperature, the thermistor should be placed freely in the air, minimizing the contact area with its bearing platform. This way the thermostat will have faster temperature response. If the thermostat is used for temperature control of a solid state object, the sensor should be located directly on the object's surface, thus enabling better temperature exchange with the object due to the thermistor's planar geometry.

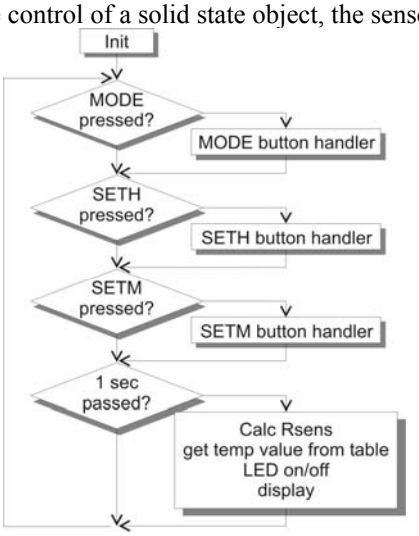


Fig.9. *The program flow diagram*

7. REFERENCES

[1] E. D. Macklen, *Thermistors.* Glasgow, U.K.: Electrochemical. Pub., 1979.

[2] O. S. Aleksić, V. Đ. Marić, Lj. D. Živanov, and A. B. Menićanin, "Novel Approach to Modeling and Simulation of NTC Thick-Film Segmented Thermistors for Sensor Application," *IEEE Sensors Journal, vol. 7, no. 10, 2007.*

[3] O. S. Aleksić, P. M. Nikolić, V. D. Jokić, V. Ž. Pejović, J. M. Pavlović, and S. Đurić "Analysis of Thick Film Thermistor Geometries," in *Proc. IEEE 21st Int. Conf. Microelectron. (MIEL'97),* Niš, Jugoslavija, septembar 1997.

[4] O. S. Aleksić, P. M. Nikolić, D. Luković, S. Savić, V. Ž. Pejović, and B. M. Radojčić "A Thick Film NTC Thermistor Air Flow Sensor," in *Proc. IEEE 24st Int. Conf. Microelectron. (MIEL 2004),* Niš, Srbija, maj 2004.

[5] http://www.ti.com/msp430

[6] MSP430x4xx Family User's Guide, Texas Instruments, 2006.

[7] Programming a Flash-Based MSP430 Using the JTAG Interface, Texas Instruments, 2006.

ONE SOLUTION OF CURRENT SOURCE DESIGNED FOR CURRENT SENSOR TESTING

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Radivoje Popović, EPFL, Switzerland
Milan Radmanović, Faculty of Electronic Engineering Niš
Dragan Mančić, Faculty of Electronic Engineering Niš

Abstract: *By the reason of research and development in company Sentronis current source for 1000A maximal DC current AD is designed and made. This device has modular construction i.e. it comprehends 20 pcs. standard PC power supply units. Thereat used voltages are +5V and +3.3V. PC power supply is elected because it is cheap and reliable. Presented configuration allows a simple extension if the requirement for higher currents exists. Additionally, realization of water cooling of power electronic components is shown.*

1. INTRODUCTION

Based on the technical label of PC power supply ATX 400W one can see that it can provide 30A for output voltage +5V and 28A for output voltage +3.3V. This power supply also has output voltages +12V, -12V and -5V, but these voltages are not of interest because we need enough strong current at as low as available voltage. The reason for such standing point is fact that applying lower voltage cause lower dissipation on strong FET in output circuit of regulator. We choused (decided) outputs with voltages +5V and +3.3V to load with maximum 25A. PC power supply is realized such that feedback for voltage regulation use output voltage +5V. It means that if we want to use some other output voltage firstly output voltage +5V must be appropriately loaded. Hence, total current available from one supply is 50A. Consequently it needs 20 supplies for 1000A. Current regulator is added to each supply. According to fact that used supplies are current sources all are connected in parallel.

2. CHARACTERISTICS OF ATX POWER SUPPLY

Minimal efficiency of ATX power supply is about 70%, for maximal load.

Voltage and frequency demands for continuous work are specified in Table 1.

Table 1. *Minimal and maximal values for input voltage and frequency*

Parameter	Min.	Nominal value	Max.	Unit
V_{in} (230Vac)	180	230	265	Vef
V_{in} Frequency	47	--	63	Hz

PC power supplies have embedded primary fuse as the protection from input over current. It is the prevention of damage and fulfill safety requirements. Also, multiple switch-on and switch-off can not induce damages in power supply or fuse.

ATX power supplies satisfy following standards:

– For safety:
UL*60950, 3rd Edition –CAN/CSA-C22.2-60950-00,
EN*60 950, 3rd Edition
IEC*60 950, 3rd Edition (CB Report to include all national deviations)
EU* Low Voltage Directive (73/23/EEC) (CE Compliance)
GB4943-90 CCIB* (China).

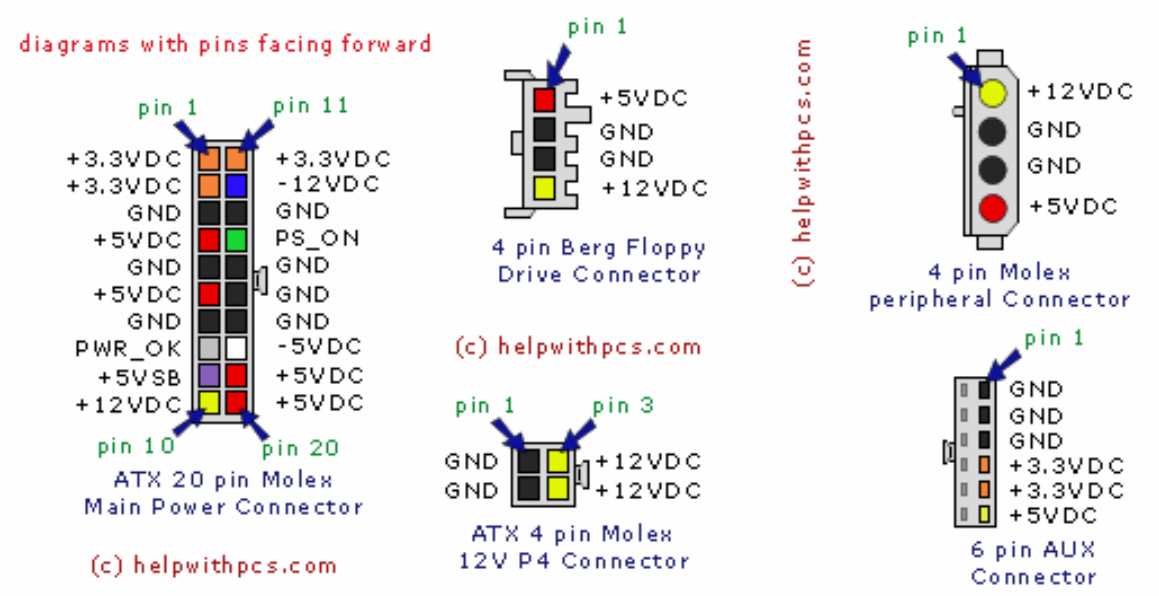

Fig.1. *Arrangement of pins for connectors of ATX supply*

– For electromagnetic compatibility:
  FCC*,Class B, Part 15 (Radiated & Conducted Emissions)
  CISPR* 22 / EN55022, 3rd Edition (Radiated & Conducted Emissions)
  EN55024 (ITE Specific Immunity)
  EN 61000-4-2 – Electrostatic Discharge
  EN 61000-4-3 – Radiated RFI Immunity
  EN 61000-4-4 – Electrical Fast Transients
  EN 61000-4-5 – Electrical Surge
  EN 61000-4-6 – RF Conducted
  EN 61000-4-8 – Power Frequency Magnetic Fields
  EN 61000-4-11 – Voltage Dips, Short Interrupts and Fluctuations
  EN61000-3-2 (Harmonics)
  EN61000-3-3 (Voltage Flicker)
  EU EMC Directive ((8/9/336/EEC)(CE Compliance)

Ripple and noise are defined as periodical or random signals in frequency bandwidth from 10Hz to 20MHz. Noise i.e. ripple for output voltage +5V and +3.3V is 50mV$_{pp}$. Power supply comprehend temperature sensor for overheat protection which purpose is to disable supply if temperature is above predetermined value.

3. SWITCH-ON OF ATX SUPPLY

ATX power supply is destined for computers and switching is controlled via motherboard. The first problem to solve is the way of switching it on. Switching-on is realized by input signal PS_ON# (green wire). PS_ON# is a TTL compatible signal activated by logical zero. When PS_ON# input is on low TTL level then power supply will be switched-on for main dc voltage levels +12V, +5V, +3.3V and -12V. Otherwise, when PS_ON# is on high voltage level or disconnected then all dc voltage outputs are on zero potential reference to the ground with no output current (Fig.2).

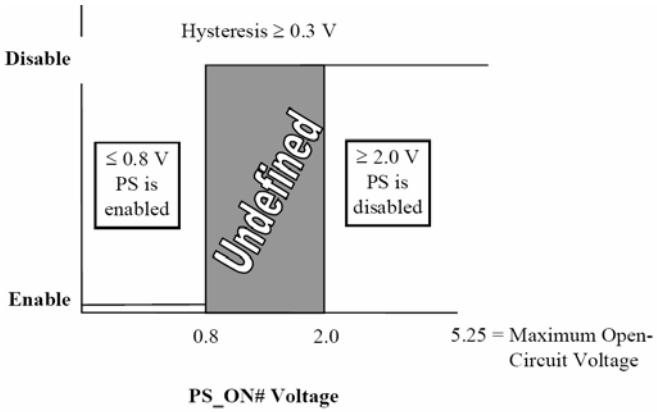

Fig.2. *PS_ON# signal characteristics*

Therefore, input PS_ON# is connected with GND via existing switch on housing of power supply. That way we allow permanent supplying on ac ~220V power-line and switching-on/off is simply realized by switch. The solution is adequate (suitable) because connecting of supplies to the ac power line induce current spikes in the ac line. The reason for that is capacitive character of the supplies. According to the fact that in our case there are 20 supplies their connection on power line can induce interrupting of the fuses.

Due to relatively great total power of all 20 supplies, they are equally arranged on all of 3 phases of ac power line.

4. CURRENT CONTROL

For every power supply, as stated above, current controller is obtained. Schematic of the current controller is shown in Fig.3.

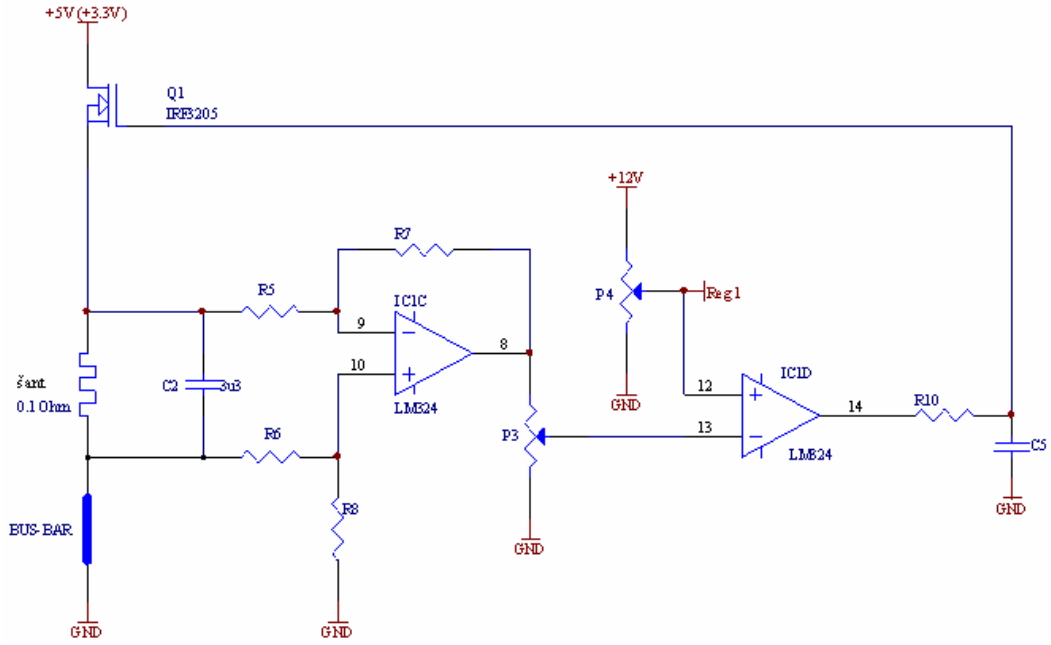

Fig.3. *The basic configuration of the current regulator of one module*

We used shunt value 0.1Ω as current sensing element. The price of commercial available shunts which satisfied requirements is significant. Because of that we used home made shunt. As shown in Fig.4, shunt is realized using wire with constantan diameter *d*=1mm and length *l*=45mm. Shunt is connected in the circuit via ceramic panel mount terminal block which prevent high temperature, which occurs on shunt, to damage elements from nearly surrounding. Current flowing through the shunt resistor produces the voltage used as input of differential amplifier which is realized by LM324.

Home made shunts are very simple but they are not calibrated, i.e. theirs output voltages are not the same for the same (determined) current. Consequently, the output voltage from amplifier needs to be directed via potentiometer P_1 to (in) discriminator. Potentiometers are adjusted so, that for determined current all current controllers provide the same output voltage.

Fig.4. *Picture of home made shunt*

During testing the current sources were maximal loaded i.e. total current was about 1000 A. At these conditions the ripple of output current is less than 1%. To emphasize that the ripple is defined as a maximal value «peak to peak» of ac voltage superimposed to the dc voltage (Fig.5). The ripple factor r is usually expressed in percents and is given by next equation:

$$r = \frac{I_{ac}}{I_{dc}} \cdot 100\% \qquad (1)$$

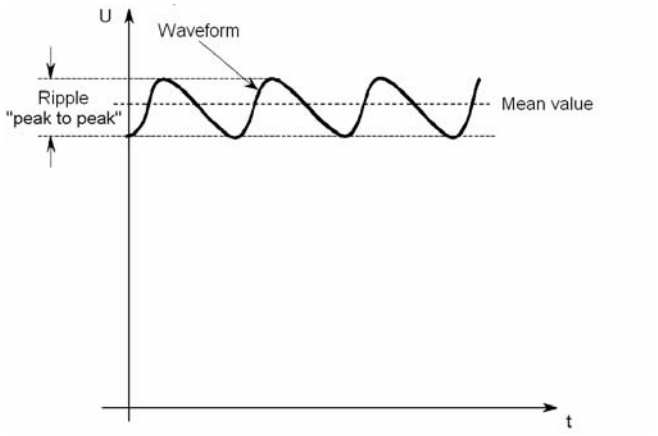

Fig.5. *Ripple of output dc current*

The main output current flow is established from all supplies via 6 pcs/pole auxiliary bus-bars (crossection 5x20mm) connected to 2 pcs/pole main bus-bars (crossection 6x40mm).

5. COOLING SYSTEM

Respecting that FETs dissipate significant amount of power, it is necessary to provide a quality cooling system. The conventional passive way for heat dissipation treatment was ineffective. Because of that we designed water cooling system. The cooler is composed from seven identical segments. Total of 12 FETs (each of two in parallel) are fixed on every segment by a screw. The segments are made from cupper bus with dimensions: width 50mm, thickness 5mm and length 555mm. On the cupper bus segments the cupper „U“ shape tubes are welded, as shown in Fig.6.

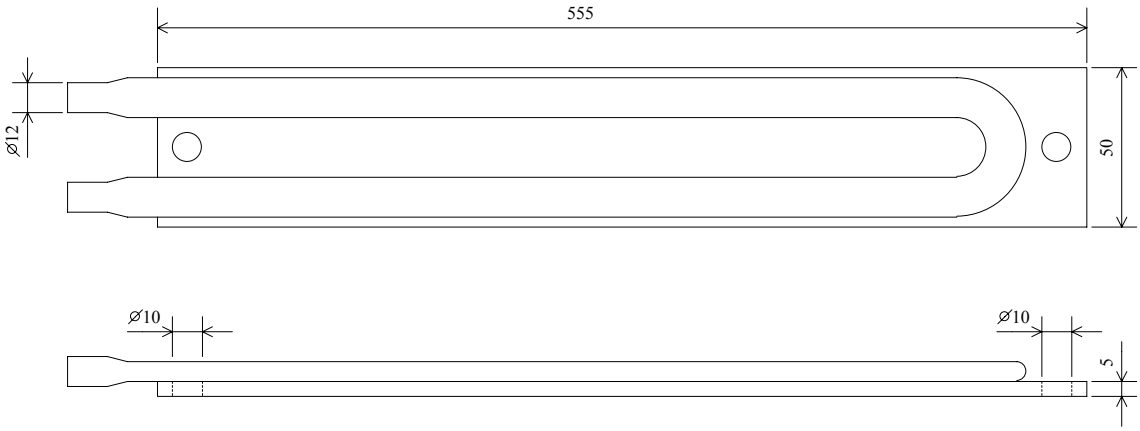

Fig.6. *Shape and dimensions of the cooler*

Considering hydraulics, the segments are serially connected, and through them flows water from waterworks and leads away to the canalization. One can note that this way of the cooling doesn't provide equal thermal dissipation from all of the segments, because the cooling of the first segment, where cool water gets into, is the best, and the cooling of the last segment is the worst, because the water is already heated. However, it is shown in the practice that this solution is enough good and the temperature differences between the segments are very small. Otherwise, if the segments are connected in parallel, it will require a valve more per segment, and more complicated way of adjusting of the equal water flow through all segments.

6. THE CONTROL OF CURRENT SOURCE

The control of current source is possible by hand (via a potentiometer), but we made the program using software package Lab VIEW for current source control. Really this program is destined for linearity measurement of current sensors. Program automatic changes the value of the control voltage on the output of A/D card. A/D card is used for current source control. Simultaneously this program reads the value of the voltage from referent current transducer. The program gives the graph of the output voltage of the tested transducer versus actual current, and automatically calculates the linearity. The front panel of this program is shown in Fig.7.

A/D card that we used is a 16 bits acquisition card NI PCI-6036E. It has 16 analog inputs (16 single ended/8 differential), PCI bus, 200KS/s, inputs ±10 to ±0.05V, 4 input ranges, 2 analog outputs 10KS/s, 8 digital inputs/outputs, two 24-bits counter/timer, digital triggering.

Realized current source is shown in Fig.8.

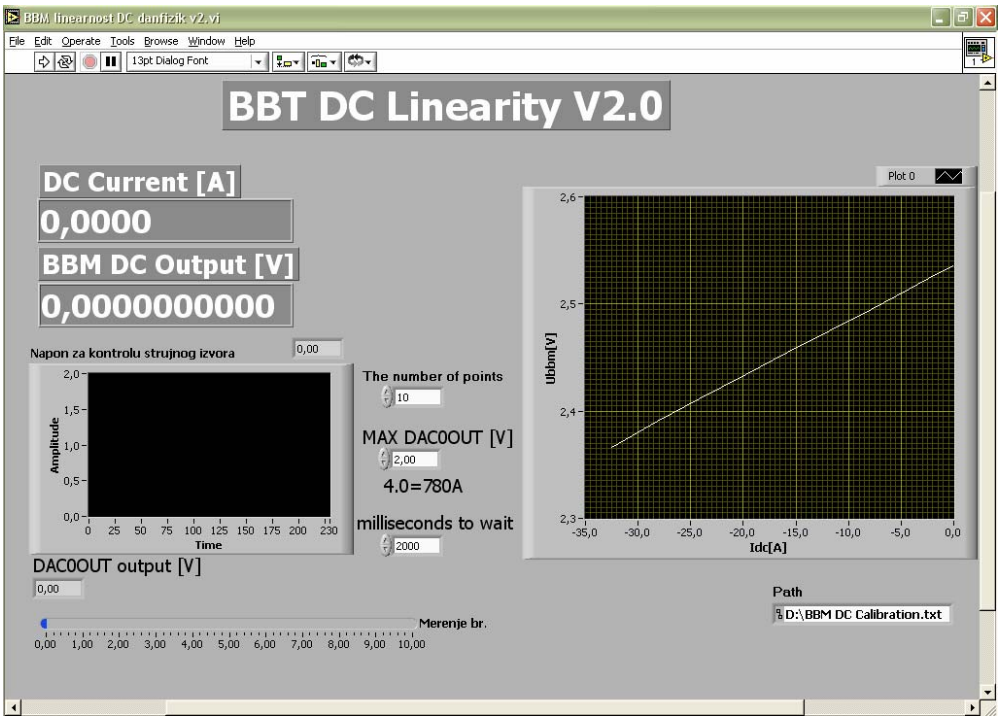

Fig.7. *Front panel of program destined for linearity measurement of current sensors*

Fig.8. *Realized current source*

7. CONCLUSION

This power supply is destined for current sensor testing and thereat it was very efficient. Current sensors were tested with maximum current of 1000A. Additionally, it is possible to modulate DC current with some NF signal, with maximal frequency of 400Hz. By this way it is possible to test current sensors at very low frequencies in the range from 0Hz to 20Hz. This is not possible with transformers.

Current source is located in a 19-inch rack mounted system as shown in Fig.2.

With this power supply we are able to test current sensors for maximal DC current of 1000A, since we used PC power supplies as modules. Because of that, in the case that it is important, we can add more modules for higher current. Respecting that we anticipate requisite for testing current sensors for higher current modular construction is very useful.

8. REFERENCES

[1] *ATX12V Power Supply Design Guide*, www.formfactors.org/developer/specs/ATX12V_PSDG_2_2_public_br2.pdf.

[2] K.H.Billings, *Switchmode Power Supply Handbook*, McGraw-Hill, 1989.

[3] D.R.Popovic, S.Dimitrijevic, M.Blagojevic, P.Kejik, E.Schurig, R.S.Popovic, "Three-Axis Teslameter With Integrated Hall Probe", IEEE Transactions on Instrumentation and Measurement, Vol. 56, Issue 4, pp. 1396-1402, Aug. 2007.

[4] K.C.Agrawal, *Industrial Power Engineering Handbook*, 2001.

APPLYING OF AJAX TECHNOLOGY IN INTEGRATION OF EMBEDDED DEVICES INTO A WEB ENVIOROMENT

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Abstract: *This paper shows the appliance of AJAX technology for asynchronous communication with XML Web services. It defines the demands an environment should fulfill in order to enable an efficient integration of embedded devices in a heterogeneous environment like the Web. In a service oriented environment, shown in this paper, XML Web services represent the basis for a middleware level in interaction between clients and embedded devices. Thanks to the implementations of the AJAX technology it is possible to generate more powerful applications in all widely accepted Web technologies like ASP, PHP, JSP and others. Concrete implementation of the described solution is realized in the system for surveillance and control of microclimate during mushroom production.*

Keywords: *AJAX, ASP, CSS, DOM, Embedded device, Middleware, SOA, SOAP, Web service, XHTML, XML, XSLT.*

1. INTRODUCTION

Today, and this will certainly be a trend in future, Internet represents the most significant technology for global integration of documents, knowledge, people and devices. Furious development of wireless and mobile communications, software, embedded systems and other technologies have significantly contributed to mass usage of the Internet as a transport medium in all areas of human activeness. Already today, many authors see the Internet, especially the Web, as a central server which connects most different resources. Mostly because of the fact that today there is a very large number of commercially available embedded devices, with built in hardware and software support for standard Internet protocols, the Web is widely used outside the common domain of B2B (business to business) applications. Unfortunately, the level of integration with embedded devices, which is accomplished in M2M (machine to machine) applications, is not on a satisfying level. Main reason for this is the fact that every solution for interaction with embedded devices is unique and applies to a specific domain, although all those solutions should enable an efficient interface to resources (sensors and actuators) of embedded devices.

This paper shows the requirements that a certain framework should fulfill in order to enable efficient integration of embedded devices into a heterogeneous environment like the Web. Modularity and service architecture of the represented framework make implementation of new technologies into specific solutions easy possible. For example, implementation of AJAX [1] (Asynchronous JavaScript and XML) technology significantly simplifies the communication between the client and the middleware realized by using XML Web services [2] (XML – eXtensible Markup Language).

2. FRAMEWORK CHARACTERISTICS

A framework, which aims for a fast and easy integration of embedded devices into a distributed environment, must fill out a large number of functional and nonfunctional requirements. Basic nonfunctional requirements are:

- A framework must be modular, expandable and flexible enough to provide possibility of interaction with a wide spectrum of hardware and software environments.
- A framework must have the capability of total control over the embedded device, either locally over the LAN network or globally over the Web.
- A framework must provide reliability, considering functionality as well as safety. Safety mechanism must be one of the components of the framework. Authentication, authorization and administration of users, which interact with the device, are mandatory functionalities of every specific implementation of the represented framework.

In order to fulfill all of these requirements the represented framework provides SOA – service oriented architecture [3] which combines key aspects of traditional REST (Representational State Transfer) [4] architecture with Web services [5]. This approach enables the embedded devices to be shown as the resources of the REST architecture i.e. enables the resources to be represented by a URI (Unique Resource Identifier). Also, complete interaction with the embedded device comes down to exchanging information about its state. Separation of state information from resource behavior is a key concept of loosely coupled components, as Web services are. On the other hand, web services make it possible for the framework to manipulate structured XML documents and do event registration as well as to apply standard HTTP and SOAP (Simple Object Access Protocol) protocols [6]. In this way, a very flexible, distributed model of concrete implementation for various applications is achieved.

On the other hand, a framework must also fulfill a large number of functional requirements, most of which are dependant of the type of embedded device the interaction should be realized with. One overview of functional requirements common for all embedded devices is shown in [7] and includes: addressing, capability of locating devices, archiving, interpretation of additional device data, defining real-time requests, event control and synchronization capabilities.

3. FRAMEWORK ARCHITECTURE

From architectural point of view components of the distributed framework, for interacting with embedded devices in network environment, can be classified in three basic layers. Those are:

- Client application – correspondents to presentations layer in the classic N – layer architecture. Beside responsibility

for user authorization and authentication, client application is responsible for interaction with a Web service. Interface with the Web service is realized by adding reference to the Web service proxy class. By using AJAX technology, periodically interaction with embedded device can be realized with out user's intervention. AJAX and Web service technologies present excellent platform for developing WEB based SCADA (Supervisory Control and Data Acquisition) systems [8]. In the shown framework, the whole interaction between a user (browser, a client application) and embedded devices is done by exchanging XML messages i.e. by using "semantic" commands. The structure of each "semantic" command (elements and attributes which describe command) as well as relationships among different commands is defined by the appropriate XML schema. The XML document, which represents set of "semantic" commands that would bee sent to the embedded device, has to be in accordance with the appropriate XML schema, i.e. a validation of the document is required. Validation of the XML document and transformation of each semantic command into a byte stream, suitable for interpretation by embedded devices, is done by a Web service.

- Web service i.e. middleware layer, is the place where all logical rules, for concrete application are realized. Validation of "semantic" commands and their transformation into a corresponding byte stream are realized at this layer. Hiding low level details of hardware and binary command set from client, Web service provide infrastructure for embedded devices integration. In this manner Web service provides "semantic" interaction between clients and embedded devices. Web service main role is to enable distributed middleware layer creation. In the distributed network applications middleware layer seeks primarily to "hide" the underlying networked environment's complexity, by insulating applications from explicit protocol and network resources handling [9]. Owning to middleware layer high level of abstraction is achieved during application design, by "hiding" complexity which is inherent to distributed network environment. Further, middleware "masks" the heterogeneity of computer architectures, operating systems, programming languages, and networking technologies to facilitate application programming and management. In other words, middleware is "glue" between distributed application, from one side, and networks functions which are responsible for sending messages to remote network components, from other side. Those remote components can be other distributed applications, servers or embedded devices with appropriate sensors and actuators.
- Embedded application, which is a part of embedded device firmware, is responsible for communicating with hardware on binary level. Beside binary communication embedded application is responsible for sensors status monitoring and actuators control.

Framework components have to provide right functionality of every embedded device and right functionality of operations which are necessary during integrating embedded devices in heterogeneous distributed networks, or Web. This primary refers to the following function types:

- Local sensors and actuators functions, which are fundamentally important for embedded devices functionality.
- Node functions i.e. specific functions, which must be executed by network application in order to maintenance network properly. Those include routing functions, Web service detecting, addressing embedded devices and so on.
- Functions at network layer which can be assumed as interface for clients and network administrators.

Fig.1 shows the logical view on an embedded systems network application.

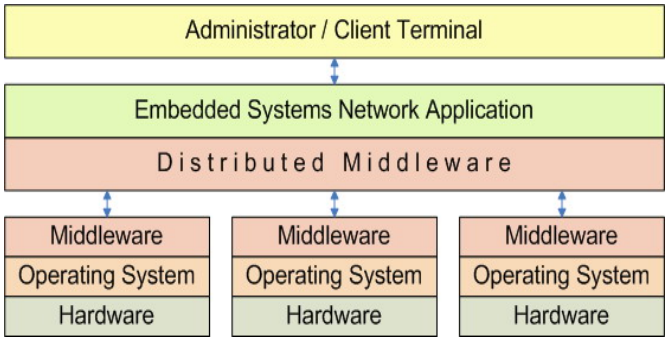

Fig.1. *Embedded systems network logical structure.*

The only way that client i.e. network application can interact with concrete embedded device, is by using services from middleware layer, as we can see at Figure 1. The Distributed Middleware coordinates the cooperation of the services within the network, and provides services "orchestration", in order to achieve desirable function. The Distributed Middleware is logically located in the network layer but it exists physically in the network nodes layer. For modern, embedded devices, with powerful microprocessor unit and enough memory space, the network node can embedded device himself, while "legacy" embedded systems use PC computer as gateway for appropriate embedded device type.

Administrator terminal is an external entity to configure network parameters, monitor network functionality and to evaluate the results. Client terminals enables interface with users. Both, administrator and client terminal can be locally connected or remote connected via the Internet.

4. AJAX

AJAX (Asynchronous JavaScript and XML) isn't a technology. It's really several technologies, each flourishing in its own right, coming together in powerful new ways [10]. AJAX incorporates: standards-based presentation using XHTML (eXtensible Hypertext Markup Language) [11] and CSS (Cascading style Sheets) [12], dynamic display and interaction using the DOM (Document Object Model) [13], data interchange and manipulation using XML and XSLT (eXtensible Stylesheet Language Transformations) [14], asynchronous data retrieval using XMLHttpRequest, and JavaScript binding everything together. Differences between classic Web applications and AJAX applications are shown on Fig.2.

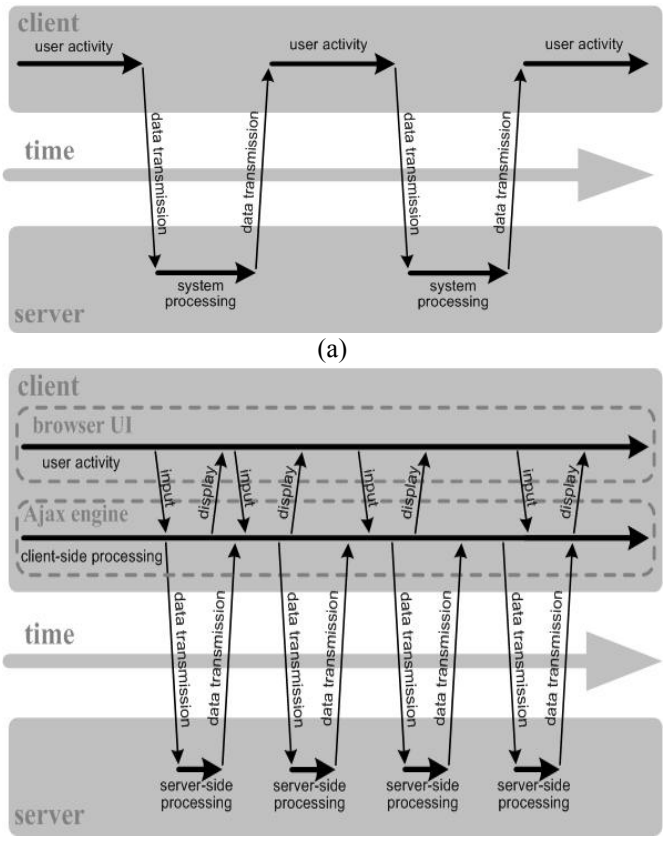

Fig.2. *The synchronous interaction pattern of a traditional web application (a) compared with the asynchronous pattern of an AJAX application (b).*

As we can see from Fig.2, AJAX application eliminates the start-stop-start-stop nature of interaction between the user and the server on the Web, by introducing an intermediary layer – AJAX engine. It seems like adding a layer to the application would make it less responsive, but the opposite is true. Instead of loading a webpage, at the start of the session, the browser loads an AJAX engine – written in JavaScript and usually tucked away in a hidden frame. Instead of loading a webpage, at the start of the session, the browser loads an AJAX engine – written in JavaScript and usually tucked away in a hidden frame. This engine is responsible for both rendering the interface the user sees and communicating with the server on the user's behalf. The AJAX engine allows the user's interaction with the application to happen asynchronously – independent of communication with the server. So the user is never staring at a blank browser window and an hourglass icon, waiting around for the server to do something.

Even if AJAX is new approach in Web programming (Jesse James Garret – February 2005.), all AJAX components are based on mature and standardized technologies. That is why all modern frameworks for developing Web applications have integrated AJAX. An example is ASP.NET AJAX, new Microsoft component, which enables developing AJAX applications by using Microsoft Visual Studio 2005. Authors used these tools to develop software modules which are part of framework shown in this paper.

5. CONCRETE REALIZATION

By integrating client applications, developed by using ASP (Active Server Pages) and AJAX technologies, with XML Web services a hardware/software module called TempHumi was developed. TempHumi is used for surveillance and control of microclimate conditions during production of mushrooms.

Hardware basis was a humidity and temperature transmitter as well as a relay control unit, made by "Bravo" – Niš. Used controller, shown on Fig.3, is based on an ATMEL AT89C4051 microcontroller [15] and has RS232 support. A SENSIRION SHT71 sensor [16] was used as a humidity and temperature sensor.

Fig.3. *Hardware for TempHumi modul.*

Basic software components of a TempHumi software module are:

- Embedded software i.e. firmware of the microcontroller. This software layer was realized by using open source C compiler SDCC (Small Device C Compiler) [17]. Communication with the device itself is defined in accordance with RS485 protocol, while I2C protocol is used for communication between the microcontroller and the sensor. Alongside these basic functions the firmware also supports other functions necessary for operation of the transmitter as are watch-dog timer and device addressing logic.
- Integration sublevel i.e. middleware, which is represented by the Web service, was developed, tested and implemented on a Microsoft .NET platform. Microsoft Visual Studio 2005 was used as a development tool, while the C# was used as the programming language. Basic function of the Web service was developed as a purpose builds Web method. This Web method receives a "semantic" command and the time in which it has to give an answer (i.e. the timeout time) as input parameters from an ASP.NET AJAX client. Role of the Web service is to do a validation of the received command word in accordance with predefined XML schema, transform the command word into a 4 byte array (start, address, command word, Irc), forward that array to the RS485 interface and then receive an appropriate 7 byte response (start, address, MsbTemp, LsbTemp, MsbHumi, LsbHumi and Lrc). Web service also does the transformation of digitalized values, received from a controller, into physical values, and generates a response object which contains logical data about temperature, humidity and the status of the execution (OK or Timeout).
- Client application is realized as three ASP (Active Server Pages). **Login page** enables access for registered users and the registration of new users. Only one user, registered with administrative credentials, can generate

commands while other users can only look at the results of previous measurements. **Administrator page**, shown on Fig. 4, is refreshed every second using an AJAX timer. Alongside the refreshment of controls, data received from the controller is written into an appropriate XML file. **Operator page**, the third page, is used by all other users to look at the contents of the XML file crated by the administrator page. Because all the results are saved in XML files, by using XSLT transformations it is possible to adjust the representation of the data for every single operator.

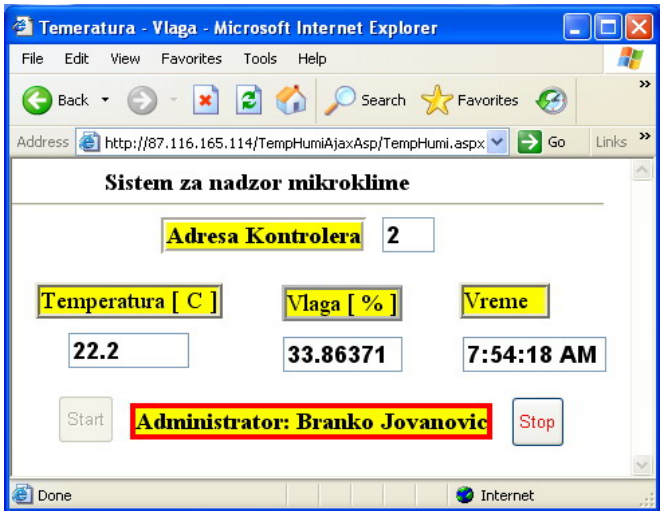

Fig.4. *Administrator page.*

6. CONCLUSION

The framework, shown here, enables design of service oriented applications with loosely coupled software components which can be independently developed and implemented. Only basic knowledge about characteristics of the framework and implementation mode of the other components is needed for successful operation of the loosely coupled components. Concrete implementations of the represented framework enable the usage of asynchronous operations and concurrent programming which further are the conditions for successful interaction, not only communication, with embedded devices. The TempHui hardware/software module for surveillance and control of micro climate conditions during production of mushrooms represents one concrete realization of the represented framework. The usage of AJAX technology on the administrator page enables periodical refreshment of the data i.e. periodical communication with a XML web service. The XML Web service itself represents the sublevel of integration between the client and the embedded device. The usage of XML files for saving data, along side the application of XSLT transformations makes data representable in many various ways.

Implementation of second generation WS-* specification in XML Web services, as well as the usage of AJAX technology are certainly going to be points of interest for further research by the authors.

7. REFERENCES

[1] W3C, "AJAX Tutorial". Available: http://www.w3schools.com/ajax/default.asp. [Accessed Jan. 2008].

[2] W3C, "Web Services Architecture". Available: http://www.w3.org/TR/ws-arch/. [Accessed Jan. 2008].

[3] T. Erl, *Service-Oriented Architecture: A Field Guide to Integrating XML and Web Services*, New Jersey: Prentice Hall PTR, 2004.

[4] R. T. Fielding, "Architectural Styles and the Design of Network-based Software Architectures", PhD thesis, University of California, Irvine, USA, 2000. Available: http://www.ics.uci.edu/~fielding/pubs/dissertation/-top.htm. [Accessed Jan. 2008].

[5] B. Jevtović, D. Oklobdžija, J. Ristić and J. Oklobdžija, "Web services as middleware for interacting with embedded devices" *6th Science-specialized symposium INFOTEH – Jahorina 2007*, Vol. 6. Ref E-I-7, Jahorina, 2007, pp 290 – 294.

[6] W3C, "SOAP Tutorial". Available:. http://www.w3schools.com/soap/default.asp [Accessed Jan. 2008].

[7] F. Jammes, H. Smit, "Service-Oriented Architectures for Devices – the SIRENA View", Science & Technology, Schneider Electric, Grenoble, France, 2006. Available http://www.sirena-itea.org/Sirena/Documents/All/SortedDocumentsList.htm. [Accessed Jan. 2008].

[8] D. Oklobdžija, B. Jevtović and N. Ristić, "Real-time information system of integrated control for asphalt production", *50th ETRAN Conference*, Belgrade, 2006, pp. 275 – 278.

[9] K. Geihs, "Middleware Challenges Ahead", IEEE Computer, Juni/2001, S. 24-31. Available: http://www.di.inf.pucrio.br/~rcerq//semGSD/sugestoes/-r6024.pdf. [Accessed Jan. 2008].

[10] J. J. Garret, "Ajax: A New Approach to Web Applications", Available: http://adaptivepath.com/ideas/essays/archives/-000385.php [Accessed Jan. 2008].

[11] W3C, "XHTML™ 1.0 The Extensible HyperText Markup Language", 2nd Edition, W3C Recommendation 26 January 2000, revised 1 August 2002, Available: http://www.w3.org/TR/xhtml1/ [Accessed Oct. 2008].

[12] W3C, "Cascading Style Sheets home page", Available: http://www.w3.org/Style/CSS/ [Accessed Oct. 2008].

[13] W3C, "Document Object Model (DOM)", Available: http://www.w3.org/DOM/ [Accessed Oct. 2008].

[14] W3C, "XSL Transformations (XSLT) Version 1.0", W3C Recommendation 16 November 1999, Available: http://www.w3.org/TR/xslt [Accessed Oct. 2008].

[15] Atmel Corporation, "ATMEL – 8-bit microcontroller with 4K bytes of Flash – AT89C4051", Available: http://www.atmel.com/atmel/acrobat/doc1001.pdf [Accessed Oct. 2008].

[16] SENSIRION inc. the Sensor Company, "Humidity and Temperature Sensor SHT7x (SHT71, SHT75)", Available: http://www.sensirion.com/en/01_humidity_sensors/05_humidity_sensor_sht71.htm [Accessed Oct. 2008].

[17] SDCC – Small Device C Compiler, Available: http://sdcc.sourceforge.net/ [Accessed Oct. 2008].

CDMA CODED WRAPPER-BASED SYSTEM BUS

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Abstract: *The recent development of Field Programmable Gate Array (FPGA) System-on-Chip (SoC) architectures, with coarse-grain processors, embedded memories and Intellectual Property (IP) cores, offers high performance for computing power as well as opportunities for rapid system prototyping. These platforms require high-performance on- and off-chip communication architectures for efficient and reliable inter-processor data transfer. By increasing the number of IP cores that are embedded in a SoC design, as well as the number of VLSI circuits that are installed in circuit boards, the problem of interconnection becomes more challenge. In this paper, we propose an efficient technique for realization of on- and off-chip system bus based on wrapper technology and CDMA techniques, in order to achieve efficient data transfer among IP cores in SoC and among chips on circuit boards. The main benefits of using this technique related to decreasing the number of wires on system bus in average for 50 %, while the main disadvantage deals with increasing the latency of Read and Write processor cycles.*

Keywords: *System bus, CDMA technique, SoC, Wrapper logic.*

1. INTRODUCTION

On-chip communications present permanent design challenge for high speed data transfer realization among building blocks in SoC design. Bus architectures (on-chip/off-chip buses), Network-on-Chip (NoCs) and point-to-point connections nowadays are used in order to successful elimination this bottleneck at complex VLSI IC design. On-chip buses can be classified into standard buses and wrapper-based buses. Standard buses are specified and realized for using protocols over wiring connections between IP cores within SoC [1]. Typical on-chip standard buses, which are used in SoC designs, are AMBA, CoreConnect, etc. Standard off-chip buses are VME, Multibus, etc. Wrapper-based approach uses the IP core interface protocol. It is independent of a physical bus protocol, and uses hardware wrappers to handle with core-to-core communications. In contemporary embedded systems, a CDMA technique is proposed as a new way for IP core interconnections. This technology relies on a principle of codeword orthogonality, such that when multiple codewords are summed, they do not interfere completely with each other at every point in time and can be separated without loss of information [2].

In this paper, we consider a realization of a system bus based on wrapper logic and CDMA technique used for data transfer between the CPU, a memory, and input/output subsystem. A corresponding wrapper structure is accompanied to each IP core in a SoC solution, or to memory/input-output module in printed circuit board solutions. By attaching a wrapper hardware the width of data and address buses is decreased, while latency of Read and Write processor cycles is increased. Implementation of a wrapper based bus is illustrated on uni-processor 32-bit system.

2. TAXONOMY OF ON-CHIP COMMUNICATION ARCHITECTURES

Taxonomy of on-chip and off-chip communication architectures is pictured on Fig.1. As can be seen from figure, communication architectures can be divided into three main classes. In this case, the term architecture relates to the structure of interconnection between processing elements, protocols and interface design [1].

In point-to-point interconnect architecture, pairs of processing units communicate directly over dedicated physically wired connections. The interconnections can be performed as custom, referred as ad hoc interconnections, or as uniform. For bus architectures, long wires are grouped together to form a single physical communication channel, which is shared among different logical channels. An arbitration mechanism is used to control sharing of the bus. Typical bus architectures are AMBA, CoreConnect etc. Network-on-Chip (NoC) is an architecture of type data communication networks, such as LANs, with inter-processor communication supported by a packet switched network.

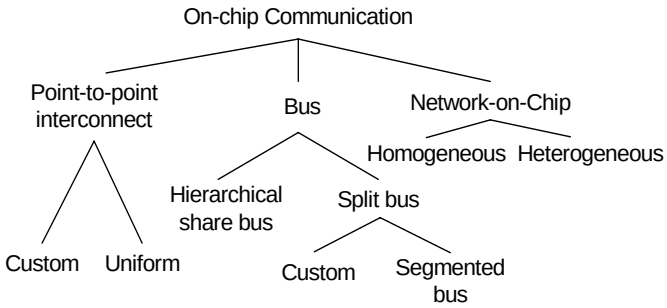

Fig.1. *Taxonomy of on-off-chip communication architectures*

Bus architectures that use the concept of a hierarhical shared bus are in focus of interest for us. Accordingly, in the sequal we will consider the implementation of uni-processor CDMA wrapper based bus.

3. UNI-PROCESSOR SYSTEM BASED ON STANDARD BUS ARCHITECTURE

A typical 32-bit uni-processor system is sketched in Fig.2. The system consists of several IP core/modules. Modules can be of master or slave type. The structure given in Fig.2 is suitable for SoC or PCB implementations. In our case, a system composed of one master and several slaves will be analyzed. The CPU is a master core, while memory blocks, MEMi, i=1, ..., *m*, and peripheral units, PERj, j=1, ..., *k*, are slave cores. All cores are connect via a system bus. The system bus is composed of unidirectional 32-bit address bus, ADR[31:0], bidirectional 32-bit data bus, DATA[31:0], and bidirectional control bus. Constituents of a control bus are: STATUS[2:0] lines - point to a current processor cycle; M/IO line - defines selection of a memory or input-output module; RD line - active when *Read* cycle is in progess; WR

line - asserted when *Write* cycle is in progess; INTR - interrupt request initiated by peripheral modules, INTA - interrupt acknowledge; RDY - assertation for data transfer readiness initiated by a slave module; CS_{Mi} (CS_{Pj}) - chip select for memory/peripheral module. The building blocks Memory_Address_Decoding_Logic, MADL, Input/Output_ Address_Decoding_Logic, IOADL, and Wait_State_Logic, WSL, are realised as interface units located between the CPU and memory/peripheral modules. In our case, the MADL and IOADL are implemented as combinational multilevel chip select decoders, while the WSL is implemented as a shift register with possibility to insert variable number of wait states.

4. MOTIVATIONS FOR USING CDMA TECHNIQUE

As a consequence of shrinking transistor dimensions, a complexity of VLSI ICs, from aspect of number of transistors, increases at faster rate than designer's possibilities to use these benefits are. Such a trend in development and research has created in a well-known gap in VLSI production. This gap appears due to limited intellectual designer's capabilities, from one side, and technology possibility to reuse IP cores in a SoC design, from other side. In average, daily, an engineer can design a logic circuit which hardware complexity doesn't exceed forty gates, while the reuse concept enables to build IC blocks with hardware complexity up to 1000000 gates. Having this in mind, but with aim to decrease the productivity gap, nowadays, many designers use extensively the reuse concept, based on pre-designed and pre-verified IP cores. Typically, IP cores are realized as microprocessors, microcontrollers, DSP processors, dedicated functional units, bus interfaces, and numerous others peripheral components. Until recently, the design-space exploration for SoCs has been mainly focused on the computational aspects of the problem, i.e. increasing microprocessor and peripheral chip performance. However, as the number of IP blocks on a single chip and their performance continue to increase, a shift from computation-based to communication-based designs becomes mandatory. As a result, the communication architecture plays a major role in the area, performance, and energy consumption of the overall systems. In order to increase system performance it is necessary to design high speed and high bandwidth data transfer buses. In contrary, further performance increase of computer constituents will be without effect on overall system performance. This is a reason way during the last several years too much research efforts in high speed bus development is devoted. But, during realization of high speed buses we meet with numerous problems. These problems are typical for realization of a interconnect. To solve this problem various techniques are used. In most cases, these techniques include implementation of additional hardware. An alterative solution to increase bus throughput consists of increasing bus data transfer lines. As a consequence, by using this approach, the number of lines, system complexity, occupied PCB area, and PCB tracing increase. In all cases, the buses with corresponding interfaces become very complex system. As a number of bus lines becomes higher the cost of these systems increases. Bearing this in mind, a bandwidth improvement achieved by increasing the number of bus lines, for most design solutions, is not a rational economical solution.

Code division multiple access (CDMA) has been proposed as an alternative way for interconnect of IP cores in a SoC design, or as a solution for interconnecting modules within a system realized in several PCBs. Compared to a conventional TDMA-based bus, a CDMA-based bus has better features concerning channel's isolation and channel's continuity in time domain since channels are divided by the spreading codes [3]. CDMA technology relies on the principle of codeword orthogonality, such that it enables efficient separation of information.

5. SYSTEM BASED ON WRAPPERS AND CDMA TECHNIQUE

A structure of a system is shown in Fig.3. From aspect of functionality, it is identical to the system presented in Figure 2. A main difference relates to the implementation of data transfer technique between master and slave modules. In both cases, for data transfer, a system bus is used. In Fig.2 it corresponds to classical solution, while in Fig.3 a system bus based on CDMA technique is implemented. In order to implement CDMA technique corresponding bus wrapper logic is appended to each module.

Wrapper based bus as an innovation technology enables reusing of IP cores in SoC designs, in an efficient way [4, 5]. From logical point of view, by using this approach, the operation of a communication logic and IP core logic can be analyzed separately. This allows us to bridge a connectivity problem, which relates to physical bus protocols. Naimely, a wrapper based approach provides us to use: a) IP core interface protocol independently of a physical bus protocol; and b) hardware wrappers to handle the core-to-core communication. Consequently, IP cores complying with the interface protocol can be easily integrated into SoC designs that use different physical buses (AMBA, CoreConnect, etc.) as backbones. However, by attaching a simple wrapper hardware we decrease, from one side, the interconnect complexity, but, from the other side, we increase the system latency. In general, an optimal solution represents a compromise between two contradictory reqirements. In order to solve this problem corectly a spetial design attention is needed.

In a concrete proposal sketcked in Figure 3, to the CPU a wrapper `BW_CPU` called master is appended. A slave wrapper denoted as BW_MEM_i is appended to memory block `MEMi`, and a slave wrapper BW_PER_j to a peripheral block `PERj`. In order to achieve a low hardware system complexity, a CDMA data transfer technique is implemented on address and data buses, only. The control bus is identical for both solutions. Let note, that the wait state logic and the logic used for selection of memory blocks or peripheral units (`WSL`, `MADL`, and `IOADL` - see Fig.2. is appended to the wrapper logic (see Fig.3.). After a system reset the CPU initializes all wrappers connected in a chain. Initialization is performed by inputing a corresponding configuration file through CIB pin.

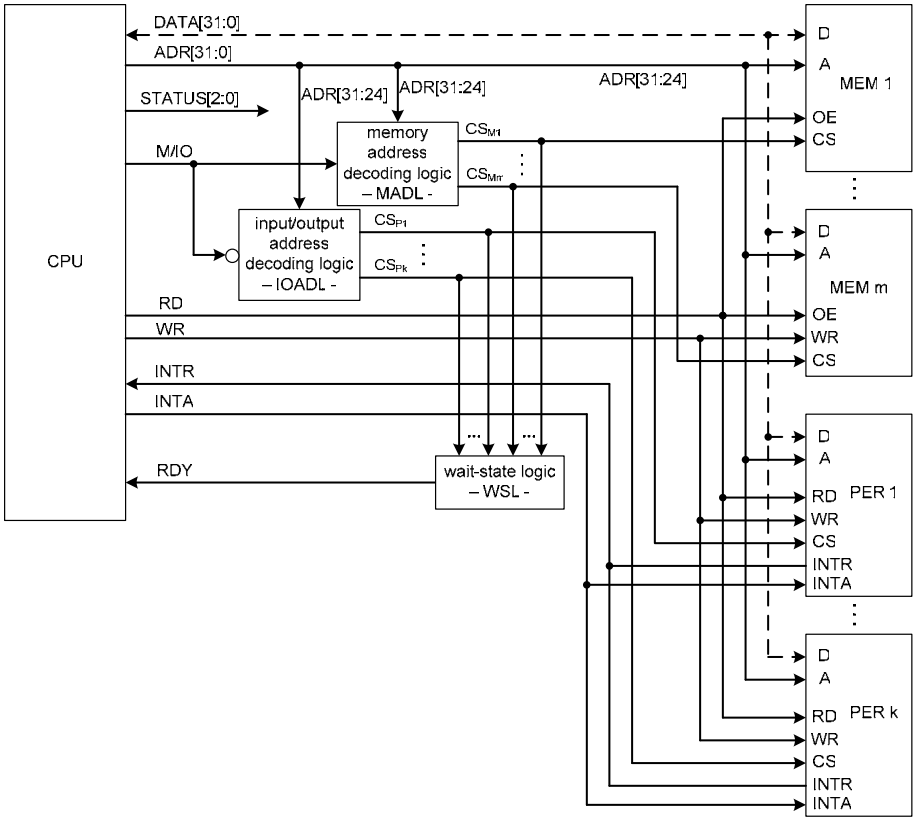

Fig.2. *Uni-processor 32-bit system based on standard bus architecture*

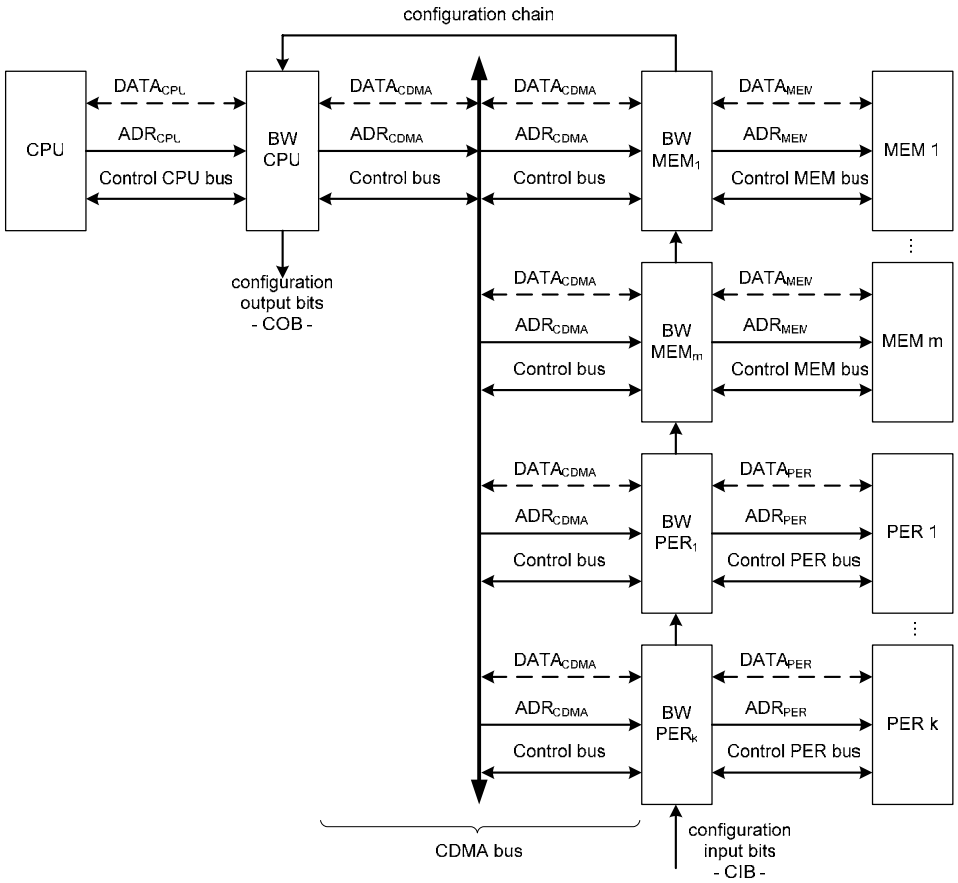

Fig.3. *Uni-processor 32-bit system organized around system bus which uses wrappers as interface logic and CDMA transmission technique for data transfer*

Master and slave wrappers are of similar hardware structure. From operating point of view the main difference between them is the following:

a) At its inputs the master wrapper accepts signals compliant with VCI 2.0 standard defined by VSIA [6], and at its outputs generates signals that are used for CDMA bus transfer.

b) At its inputs a slave wrapper accepts signals from CDMA bus, and at its outputs generates signals compliant with VCI 2.0 standard.

Since the structures of a master and slave wrapper are similar, in the sequel, we will explain the structure of a master wrapper, only (see Fig.4.).

Constituents of a BW_CPU are: the functional units BWCU (*Bus Wrapper Control Unit*), AE (*Address Encoder*), DED (*Data Encoder/Decoder*) and CD (*Command Decoder*), and system control units CG (*Clock Generator*) i CR (*Configuration Register*). The CR unit accepts and stores a configuration file [7]. CG acts as a PLL system. It generates clock signals for all functional units. A BWCU is realized as a finite state machine (FSM). It generates control signals for driving BW_CPU functional units. The AE converts a binary coded address into a CDMA address. A DED is bidirectional converter. It operates in half-duplex mode using time division multiplexing. In a direction CPU → CDMA bus a DED converts CPU output data into CDMA data. In opposite direction, it converts CDMA data into binary coded CPU input data. A CD unit passes through the CPU control signal lines to CDMA control bus.

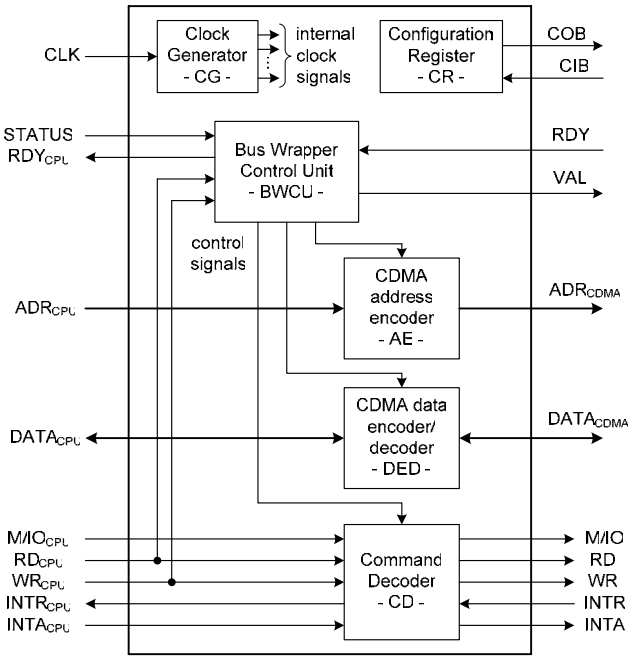

Fig.4. *Wrapper structure*

The operation of a CDMA coded wrapper-based bus we will explain on execution of processor Read (see Fig.5.) and Write cycles (see Fig.6.). The Read cycle begins at instant t_0. After a time period t_a the CPU sets its address and status output lines at valid states and the MW accepts them. As a response, the MW activates a signal RDY. It signals CPU to insert wait states. In addition, the MW converts address from binary to CDMA code and sends it via a CDMA bus to slave wrappers. A total time period, t_{12}, used for address transfer in a direction CPU → MEM/PER module (see Fig.5.), is defined as $t_{12} = t_{MW} + t_{cc} + t_p + t_{SW}$; where: $t_{MW}(t_{SW})$ is a needed time to latch address in a master (slave) wrapper; t_{cc} is a transfer time of CDMA coded information; and t_p corresponds to signal propagation time over CDMA bus. t_{cc} is proportional to number of bits in a spreading code and is equal to $t_{cc} = s * t_{br}$; where s is number of bits in a spreading code, and t_{br} is time for processing and transfer of single bit through CDMA bus. Since, $t_{cc} >> t_{MW} + t_{SW} + t_p$ than $t_{12} \approx t_{cc}$ is valid. Let note that in Fig.5. time intervals t_{MW} i t_{SW} are not presented. After t_2, an access to memory or peripheral module is performed, for time period t_{acc}. At instant t_3, the addressed module has ready data and sends them to SW. A module SW codes data and delivers them to MW. MW block decodes data and sends them to CPU-u. After that, SW deactivates a signal RDY which passes through MW and drives CPU. In this moment, the wait state is terminated. Next, the CPU accepts data present on data lines and after t_b, in t_5 it terminates a Read cycle.

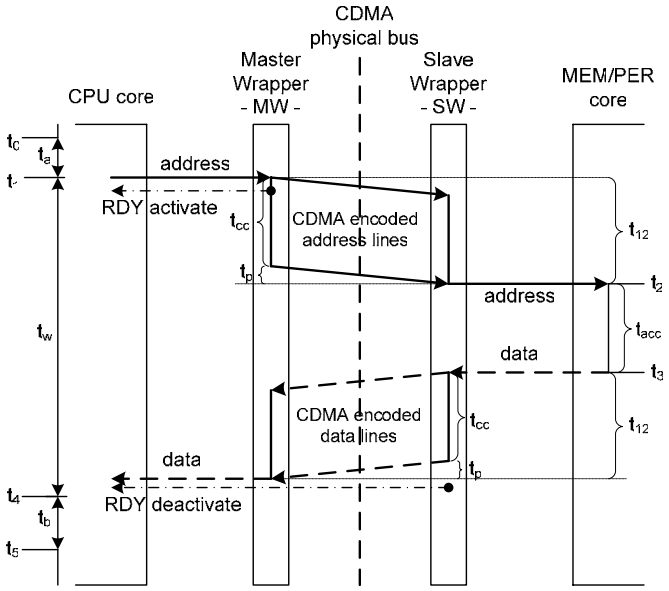

Fig.5. *Signaling scenario of a* Read *processor cycle*

In Fig.6 a Write cycle is sketched. The scenario of this cycle is simpler in respect to the Read cycle. The main difference is the following: During the first part of a Write cycle, at instant t_1, the CPU generates an address, while at t_1' it generates a binary coded valid data. Both address and data bus signals drive the BW_CPU which converts them into CDMA coded signals. During this $\tau = t_1' - t_1 \approx 0$ is valid. In order to make visual presentations (Fig.5. and 6.) more illustrative, the address transfer is pictured by a full line, while data transfer is pictured by a broken line.

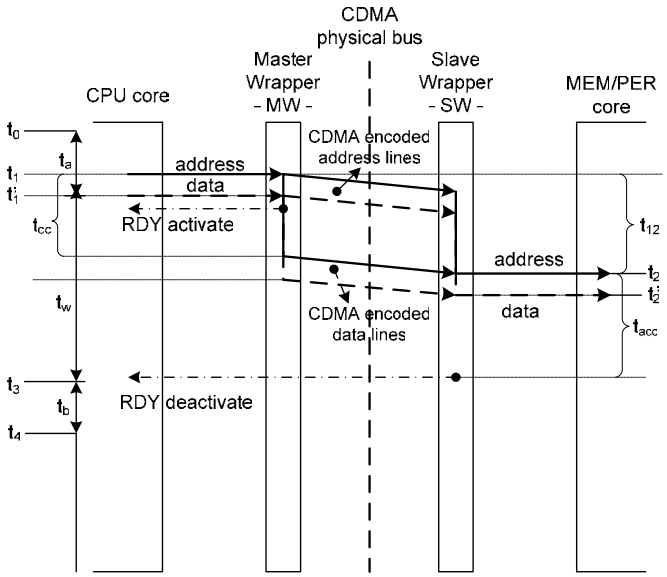

Fig.6. *Signaling scenario of a* `Write` *processor cycle*

RESULTS

The proposed method can be implemented to any address and data bus as constituent of a system bus. In a concrete case, we use S orthogonal codes for CDMA coding. As a result, if unencoded buses are of n bits width then the CDMA coded equivalent buses will be reduced to $p = \frac{n}{S}\lceil \log_2 S + 1 \rceil$ bits. For 8-bit spreading code a bus reduction is 50%. Results concerning an average bus reduction, denoted as R_{BL}, are given in Table I. As a consequence of implementation a CDMA data transfer the system latency increases. It is expressed as a number of clock pulse periods in term of a spreading code width. For Read cycle a latency is denoted as T_{RCP}, and for Write cycle as T_{WCP}. The results which relate to T_{RCP}, and T_{WCP} are given in Table 1.

Table 1. *Performance concerning bit reduction and latency*

n / S	8	16	32	64	128	256	R_{BL} (%)	T_{RCP} (clk)	T_{WCP} (clk)
4	6	12	24	48	96	192	25	8	4
8	4	8	16	32	64	128	50	16	8
16	-	5	10	20	40	80	68.75	32	16
32	-	-	6	12	24	48	81.25	64	32

6. CONCLUSION

An efficient technique for realization of on- and off-chip system bus based on CDMA techniques and wrapper technology is proposed in this paper. It is intended to achieve an efficient communication between IP cores in on-chip bus, and CPU and memory/peripheral modules in off-chip system bus. The benefits of the proposal relate to decreasing data and address bus width. The drawback deals with increasing system latency. The proposed solution is not implemented on a control bus in order to be compliant with already well know wrapper based solutions for standard buses such as AMBA, CoreConnect etc. The wrapper logic, realized on FPGA platform, provides a possibility to implement a reconfigurable solution. The reconfiguration is possible to achieve by modifying the configuration file during FPGA/system initialization phase.

7. REFERENCES

[1] Terrence S. T. Mak, N. Pete Sedcole, Peter Y. K. Cheung, Wayne Luk , "On-FPGA Communication Architectures and Design Factors", *in International Conference on Field Programmable Logic and Applications*, 2006, pp. 1-8

[2] X. Wang, T. Ahonen, and J. Nurmi, "Applying CDMA Technique to Network-on-Chip", *IEEE Transactions On Very Large Scale Integration (VLSI) Systems*, Vol. 15, No. 10, October 2007, pp. 1091-1100

[3] B. C. Lai, P. Schaumont, and I. Verbauwhede, "CT-bus: A Heterogeneous CDMA/TDMA Bus for Future SOC" in *Proc. 38th Annu. AsilomarConf. Signals, Systems, and Computers*., Vol. 2, Issue 7-10, Nov. 2004, pp. 1868 – 1872

[4] K. Anjo, A. Okamura, M. Motomura, "Wrapper-based bus implementation techniques for performance improvement and cost reduction", *IEEE Journal of Solid-State Circuits,* Vol. 39, Issue 5, May 2004, pp. 804 – 817

[5] R. Lysecky, F. Vahid., "Pre-fetching for Improved Bus Wrapper Performance in Cores" *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 7, No. 1, January 2002, pp. 1-33

[6] On-chip Bus Development Working Group, "Virtual Component Interface Standard Version 2", April 2001.

[7] A. Athavale, C. Christensen, *High-Speed Serial I/O Made Simple*, Xilinx Connectivity Solutions, San Jose, April 2000.

MICROCONTROLLER SELECTION IN EMBEDDED SYSTEMS

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Abstract: *A large assortment of microcontrollers on the semiconductors market, and convergence of their prices in a range of 20$, often produce a serious dilemma for embedded system designer: what microcontroller to choose? Typical mistake made in such situations is to take a single criterion in to account – defined budget. As a result, a powerful modern microcontroller is selected, with diverse and complex set of peripherals. Since selected device is usually oversized and too much complicated for intended application, the consequences are prolonged time to market and increased production cost. The proposed paper suggests that usefulness of the particular microcontroller mostly depend of its speciality for intended application.*

Keywords: *Microcontroller, RISC, CISC, embedded systems.*

1. INTRODUCTION

Not long ago, the computer word was flooded with many different promising computer architectures with lot of exiting alternatives, advances and innovations. But nowadays, there is no doubt that the mainstream of computer architecture development, designated for personal computers, servers and workstations, has collapsed into a single architecture: Intel x86 [1]. Once-mighty processors, like MC68000, MIPS, ALPHA, PowerPC, SPARC and other, one by one, have faded from the scene, replaced by the ubiquitous Pentium II and its descendants [1]. It has turned out that crucial influence on processor performance hasn't been architecture, nor instruction set, nor even CISC/RISC conception, but the semiconductor fabrication process, reducing the computer industry into an improving and repackaging exercise for Intel, AMD, and several smaller manufacturers. Based on those facts, a logical question arises: is there any sense to deal with anything different form x86 architecture? The answer is yes, although it sounds contradictory! The reason is a great versatility of a special kind of microprocessors – microcontrollers.

According to *World Semiconductor Trade Statistics* [2], calculated on a net market income, x86 microprocessors designated for personal computers, servers and workstations, occupy 50% of the microprocessor market, but counted on a number of the sold units, more than 99.5% of the market belongs to microcontrollers.

What is a microcontroller? Contrary to classical microprocessors, which are designated for desk-top or server computer manufacturing, microcontrollers are primarily designated for realization of small controller applications – called embedded applications. It is common for microcontrollers to have several devices integrated on the same silicon chip: CPU, RAM, ROM, and a combination of other peripherals – digital ports, analog ports, communication controllers, timers, counters etc. According to [2] the calculation is simple – on each x86 sold unit there are 199 sold microcontrollers, and if the average price of x86 microprocessor is 199$ then the average price of a microcontroller is only 1$. Low microcontroller prices produce radical change in design philosophy of electronically controlled devices; microcontrollers are embedded everywhere, in TV sets, monitors, hard disks, keyboards, vacuum cleaners, toasters, mixers and even in children toys – any battery powered toy has embedded microcontroller. Compound equipment in which microcontrollers are integrated together with mechanical or electromechanical hardware, and where microcontroller ménage relatively small number of control functions, is often called embedded systems.

There are several different kind of microcontrollers, 4-bit, 8-bit, 16-bit, 32-bit, with signal processing capabilities, low power, with lot of memory, with USB support, with TCP/IP support, based on CISC or RISC architecture etc. Such diversity often makes difficult for embedded system designer to make a proper choice. The most common solution is to fix the upper price for microcontroller, and then to choose controller with maximum processor strength within demanded price limits. Low microcontroller prices (average price of 32-bit, 16-bit and 8-bit families converge to few $ for each family) makes that such approach causes selection of a microcontroller with excessive performances. As a result, usually more disadvantages than benefits appear: the software is not simpler, but the hardware is more complicated and more expensive.

Deliberate review of selection practices is presented in this paper. Several main criteria that should be considered in microcontroller selection procedure are discussed, from viewpoints of development tolls, architecture and technology. Several characteristic examples are presented; in order to disprove widespread misunderstanding that the imperative criterion for microcontroller selection is the processor strength/price ratio.

2. MICROCONTROLLER SELECTION CRITERIA

Contrary to x86 microprocessors, where the execution speed of the system software is the main and almost singular criterion, for microcontrollers instruction execution the speed is only one among many criteria – usually the least important: many industrial processes, controlled by microcontrollers are very slow, duration of a control cycle is 10ms and more! The most important hardware selection criteria, along with execution speed, are: a) architecture specificity, b) code density, c) the amount of memory and d) the power demands. A discussion about these criteria will be illustrated by code examples for two microcontroller families, one "old-fashioned" and one "modern" family:

- 80C51, the oldest CISC family, that occupies major part of 8-bit microcontroller market, and
- MSP430, modern 16-bit RISC family, dominant on low power microcontroller market.

2.1. CISC/RISC dilemma, code density and execution speed

A superficial statement that still exists in academic and engineering community is that RISC type of computer architecture has many advantages compared to CISC architectures [3]. RISC processors are considered more modern, efficient, and cost-effective than older CISC chips. They're generously endowed with better performance, lower power consumption, and higher speeds. In many cases,

microcontroller selection is based on that criterion – it is "fancy" to use RISC microcontrollers. However, the progress of semiconductor manufacturing technology made that such a statement has been pointless for more than 15 years: pure RISC architecture concept virtually disappeared with increased number of available transistors per silicon chip. In all modern processors, instruction set is designed to execute main instructions in a single machine cycle, while other useful non-RISC instructions are multi-cycle and accelerated as much as available transistor count permits. In that way, all RISC advantages are preserved, and in addition rich CISC-like instruction set allows efficient compiling, together making final code both fast and memory efficient. Compilers written for those processors have wide scale of compiling opportunities: from maximally fast code, to maximally compact code.

It is well known that original RISC concept implies that CPU core efficiently works with data stored in great number of internal general purpose registers [3], while communication with memory and peripherals is occasional and managed by LOAD and STORE instructions. In embedded applications such a concept is unfavorable – control applications need frequent access to peripherals. Microcontroller designers were aware of this and other RISC disadvantages, so they formulated modified concept: "RISC architecture without RISC-disadvantages" [4]. In Table 1 a comparative characteristics review for two microcontrollers, 80C51 [5], and MSP430 [4] is shown. It is satisfied for both families:

- There are no LOAD and STORE instructions.
- Operands for arithmetic and logic instructions must be only in general purpose internal registers.
- There is no fixed instruction format.
- There are multi-cycle instructions.
- There are plenty of addressing modes for memory and peripheral access.

Table 1.

	Family	
	80C51	MSP430
Working registers	A, R0–R7	R4–R15
Instruction count	51	27
Addressing modes count	5	7
Execution speed in machine cycles count	1, 2 & 4 (4: mul & div)	1 – 6
Instruction length	1,2 i 3 bytes	1,2 i 3 words

According to the previous analysis, it is clear that both families have conceptually similar architecture, and that both equally deviate from "academic RISC philosophy". It seems that microcontroller manufacturers declare their microcontrollers as a RISC machines as a marketing claim with no serious meaning for engineering selection criterion.

When the execution speed is considered, the usual misunderstanding is that duration ratio of machine cycle and main clock cycle is a reliable speed measure. For example, if a machine cycle of one microcontroller lasts four clock periods, and duration of the second microcontroller machine cycle is two clock periods, it is usually assumed that the second microcontroller is faster. But in the reality, the information about the (machine cycle)/ (clock cycle) ratio, segregated from the other facts, is worthless. It is possible that the first microcontroller can be driven at much higher clock speeds, or that instructions of the second microcontroller last a lot of machine cycles, making the first one much faster in real program executions. In example 1.a, a fragment of a simple C code is illustrated, while in examples 1.b. and 1.c. assembly code listings of compiled C code from 1.a, are presented, for P89LPC901 (8051 family) and MSP430x11x1 (MSP430 family) microcontrollers. The used compilers were Keil Cx51 Compiler [6] and MSP430 IAR C/C++ Compiler [7], both configured for speed optimization.

```
void Test_1(void){
register unsigned char i,m,c;
   c=P2; // c:=port P2
   for(i=10;i!=0;i--){
                      m=i*c+1;
                      proc (m);
                     }
}
```

Example 1.a.

```
Test_1:
   MOV   R6,#10
   MOV   R5,P2
   ;     R6 := i
   ;     R5 := P2
L1:
   MOV   A,R6
   ;     A := i
   MOV   B,R5
   MUL   AB
   ;     A := m
   INC   A
   CALL  PROC
   DJNZ  R6,L1
 RET
```

Example 1.b.

```
Test_1:
   MOV.B  #010,R11
   MOV.B  P2IN,R10
   ;      R11 := i
   ;      R10 := P2
L1:
   MOV.B  R11,R12
   MOV.B  R10,R14
   CALL   #MUL8
   ;      R12 := m
   INC.B  R12
   CALL   #PROC
   DEC.B  R11
   JNE    L1
 RET
```

Example 1.c.

Example 1. *Listing of simple C program and related assembly listings of compiled C code for P89LPC901 and MSP430x11x1 microcontrollers.*

If the number of machine cycles inside loop is counted, one can observe that RISC (MSP430x11x1) microcontroller needs much more cycles, because of slow 8-bit software multiplication managed by calling MUL8 routine. If multiplication is neglected, the number of machine cycles is similar for both controllers. It is obvious that the lack of multiplying instruction in that particular case significantly reduces program execution speed, while 16-bit RISC architecture doesn't yield any improvement in realization of program flow control.

Contrary to personal computers, the size of RAM/ROM inside microcontrollers is always limited, making code density of embedded programs a very important demand. The code from 1.b. example occupies only 11 bytes of ROM and it is much better than code from 1.c, which occupies 13 program words (13 words = 26 bytes). Example 1 is a typical situation in which a modern 16-bit "RISC" device can manifest inferior performance compared to outdated 8-bit "CISC" device.

In conclusion, when architecture, code density and

execution speed are important criteria for microcontroller selection, some directions should be considered:

1. RISC/CISC dilemma is unreasonable. It is important for an instruction set to be fast and rich with instructions, in order to write short and fast programs. A typical example for poor instruction set is 8-bit Microchip controllers, families from 10 to 16 [8].
2. If embedded system doesn't need intensive math calculations with 16-bit or 32-bit numbers, the best choice are 8-bit microcontrollers (with direction 1 satisfied). Control algorithms in most cases are implemented as state machine, causing that the control program is organized trough lots of loops, branches, interrupt responses, etc, what can be implemented by 8-bit devices with better efficiency then with 16-bit and 32-bit controllers.
3. The same control algorithm (without 16-bit or 32-bit math calculations) coded in 8-bit microcontroller, occupy approximately half of the memory compared to 16-bit devices and a quarter of the memory compared to 32-bit devices.

2.2. Architecture specificity

Any microcontroller family has some particular characteristics that made it specialized for some application type. A good illustration is the old-fashioned 80C51 family and binary data processing.

There are plenty of applications in which single-bit binary signals should be processed. In such applications good choice are microcontrollers with a hardware support for bit-oriented arithmetic (devices with bit-oriented ALU) [9]. In 80C51 microcontroller family, all digital ports are bit-addressable, there is a bit-oriented ALU, and part of RAM is bit-addressable. The advantage of such an architecture compared to the universal MSP430 architecture is illustrated in the next example.

Suppose that one should construct a device for binary signal processing according to hardware schematic of 5-bit shift register, Fig.1.

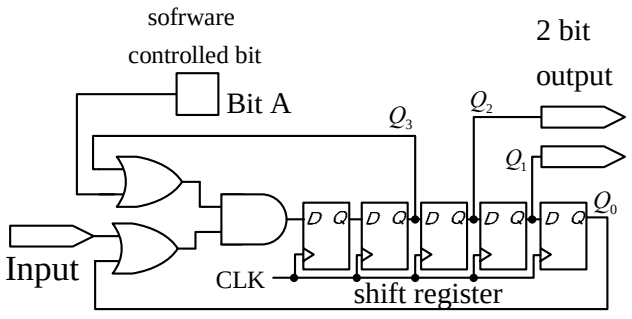

Fig.1. *Hardware schematic for binary signal processing.*

C program fragment and corresponding assembly code listing for P89LPC901, which implement one step of shifting, are shown in example 2.

Duration of code fragment from example 2 is always 19 machine cycles, and it should be synchronized with shifting clock CLK. Implementation of the same hardware algorithm with microcontroller MSP430x11x1 is shown in example 3. In that case, executions of code fragment last between 26 and 32 machine cycles. In addition to larger execution time, counted in machine cycles, this execution time is variable and depends on conditions inside "**if**" instructions. This behavior induce dither in the output binary sequence that can't be tolerated in many applications. Moreover, memory requirements for MSP430x11x1 is approximately doubled compared to P89LPC901: 58 bytes vs. 28 bytes.

```
// definitions and declarations
#define Input     P3_1
#define Output1   P3_2
#define Output2   P3_3
bdata char ShReg;// bit address. byte
   sbit Q4=ShReg^7;
   sbit Q3=ShReg^6;
   sbit Q2=ShReg^5;
   sbit Q1=ShReg^4;
   sbit Q0=ShReg^3;
bit BitA ,Tmp;
// part of the C code which
// execute one-bit shift
Tmp=(BitA|Q3)&(Input|Q0);
ShReg >>=1;
Q4=Tmp;
Output1=Q1;
Output2=Q2;
```

Assembly code of compiled C code:

```
      MOV   C,Q0
      ORL   C,P3.1   ; C=(BitA|Q3)
      MOV   B.7,C
      MOV   C,Q3
      ORL   C,BitA   ;C=(Input|Q0)
      MOV   A,ShReg
      RRC   A        ; ShReg >>=1;
      MOV   ShReg,A  ; Q4=Tmp;
      MOV   C,Q1
      MOV   P3.2,C   ; Output1=Q1;
      MOV   C,Q2
      MOV   P3.3,C   ; Output2=Q2;
```

Example 2. *C code listing and corresponding assembly code listing for P89LPC901 which implements device from Fig.1.*

The previous discussion shows that during the process of microcontroller selection, it is very important to be aware of microcontroller specialization for intended application, what is usually much more important than the universal processor speed and performance.

2.3. Size of RAM/ROM memory

A typical practice in a case of microcontroller software design is that program code is loaded into ROM (Flash, EPROM or EEPROM), while RAM is used for storing program working variables. The size of RAM in various microcontrollers typically varies between 64 bytes and 16 Kbytes and ROM between 512 bytes and 512 Kbytes. But the memory size doesn't have the same meaning for 8-bit, 16-bit, and 32-bit microcontrollers, because of different code density.

```
// definitions and declarations
#define Input  P1IN&0x01
#define Q4     ShReg&0x80
#define Q3     ShReg&0x40
#define Q2     ShReg&0x20
#define Q1     ShReg&0x10
#define Q0     ShReg&0x08
```

```
#define BitA   BitAReg&0x01
register char ShReg, BitAReg;
// part of the C code which
// execute one-bit shift
  if((BitA||Q3)&&(Input||Q0)){
    ShReg>>=1;
    ShReg|=0x80;}
  else{
    ShReg>>=1;
    ShReg&=0x7F;}
  if(Q1) P1OUT|=0x02;
  else P1OUT&=0xFD;
  if(Q2) P1OUT|=0x04;
  else P1OUT&=0xFB;
```

Assembly code of compiled C code:

```
      ;if((BitA||Q3)&&(Ulaz||Q0))
      bit.b   #0x1,R15
      jc      L1
      bit.b   #0x40,R14
      jnc     L2
L1:   bit.b   #0x1,&P1IN
      jc      L3
      bit.b   #0x8,R14
      jnc     L2
L3:   rrc.w   R14    ; ShReg>>=1;
      jmp     L4     ; ShReg|=0x80;
L2:   rra.w   R14    ; ShReg>>=1;
                     ; ShReg&=0x7F;
      ;if(Q1) P1OUT|=0x02;
L4:   bit.b   #0x10,R14
      jnc     L5
      bis.b   #0x02,&P1OUT
      jmp     L6
      ;else P1OUT&=0xFD;
L5:   bic.b   #0x02,&P1OUT
      ;if(Q2) P1OUT|=0x04;
L6:   bit.b   #0x20,R14
      jnc     L7
      bis.b   #0x04,&P1OUT
      ;else P1OUT&=0xFB;
L7:   bic.b   #0x04,&P1OUT
```

Example 3. *C code listing and corresponding assembly code listing for MSP430x11x1 which implements device from Fig.1.*

It is doubtless that an advantage of the larger memory size is the relaxed programming of control applications using object-oriented programming languages and software tools – it is well known that programming using C++ language together with the extensive use of class libraries produce large machine code with plenty of internal variables, which means large RAM and ROM are needed. But contrary to the pure C or assembly language, application development in C++ needs less time, source code is shorter and more readable, program maintenance is easier, and migration to other microcontrollers is much easier. On the other hand, the size of RAM/ROM is the main factor in microcontroller price and many microcontrollers with a good and useful architecture have modest memory size. On the other hand, it is well known that complex embedded systems that need complicated control algorithm and large ROM size, can be more efficiently designed in a distributed arrangement (a network of many small microcontrollers adequately outspreaded trough the whole embedded system) than in a centralized arrangement (a single powerful microcontroller that manages the whole system)[10]. In distributed case, each microcontroller executes algorithm that is responsible only for a particular part of the system, what makes its software smaller, more specific, and easier for size optimization.

When the size of ROM is a design criterion, several recommendations should be followed [10]:

It is necessary to divide the control program in many subroutines; all instruction sequences that are repeating more than once should be arranged as subroutine.

1. More similar instruction sequences can be organized as one subroutine, which particular sequence is executed depends on input parameters
2. If more than one subroutine uses the same input variable, this variable can be globally declared
3. Microcontrollers with rich instruction set generally have compact machine code and have advantages in the required ROM size
4. If there is a need for many interrupt routines, microcontrollers with hardware selection of working register banks manifest significant saving of ROM - instead of coding instructions for pushing working register on the stack, only register bank should be switched [5].

If the size of RAM is critical, and there is enough ROM, good microcontroller architecture can't help a lot. In that case, a good compiler which takes care of variable overlaying, and extensive usage of inline functions can significantly reduce RAM needs.

For applications where both ROM and RAM should be large, microcontrollers with an external system bus can be selected and large RAM end ROM memories can be externally connected.

2.4. Power supply issues

In certain number of embedded applications, microcontroller power consumption is not important – some controlled equipment consume much more power than any microcontroller, and if the price of controlled equipment is high, it is senseless to take special care about microcontroller price. In that case application of some miniature industrial PC is the best solution [11].

Modern low power microcontrollers are usually supplied with 3.3V or less power supply. But in large noisy environment this characteristic can be troublesome – noise margins for those controllers are reduced compared to microcontrollers with 5V power supply.

Low power controllers are usually equipped with several power-down modes. Embedded system designer should be convinced of time required for leaving of power down mode. If that time is long, then servicing of the real-time events can be unreliable.

3. CONCLUSION

Microcontroller selection procedure during the early phases of embedded system design, in many practical situations is meter of improvisation: chosen microcontroller was used in previous projects, or modern microcontroller with big processing strength is selected. In both cases final design can be more expensive and it is not uncommon that

whole system must be redesigned and based on another microcontroller. In order to avoid negative consequences, microcontroller selection procedure should be systematically performed:

a) Physical demands should be correctly defined: target price, physical dimensions, power supply demands, temperature range, etc.
b) Processing demands should be correctly defined: numerical precision in math calculations, maximally allowed time for execution of critical program loops, maximal interrupt response time, etc.
c) Definition of input/output demands should be done: how menu digital channels, what is the maximal frequency on digital channels, analog channels, resolution and bandwidth of analog channels, etc.
d) The correct estimation of required ROM size should be conducted, by writing and compiling of the main parts of microcontroller program.
e) The correct estimation of required amount of RAM should be conducted by calculating the stack size, the size of software buffers and the net size of working variables.
f) It is necessary to check the microcontroller availability on the market, and the availability of development tools.

If the result of systematic decision is more than one microcontroller, the recommendation is to use a device with best development tools.

4. REFERENCES

[1] Jim Turley, "RISCy Business, " *Embedded Systems Design*, May, 2003.
[2] www.wsts.org
[3] John P. Hayes, *Computer Architecture and Organisation*, McGraw-Hill, 3rd ed. 1998.
[4] Chris Nagy, *Embedded Systems Design Using The Ti Msp430 Series*, Elsevier 2003.
[5] *8-Bit Embedded Controllers*, INTEL 1992.
[6] *Keil Cx51 Compiler User's Guide*, Keil Software 2001.
[7] *MSP430 IAR C/C++ Compiler v4.09A*, IAR Systems 2007.
[8] www.microchip.com
[9] "Using the Intel MCS-51 Boolean Processing Capabilities", *Embedded Applications*, INTEL 1980.
[10] Giovanni De Micheli, Rolf Ernst, Wayne Wolf, *Readings In Hardware/Software Co-Design*, Elsevier 2001.
[11] www.pc104.org

DIDACTIC APPLICATIONS OF ALLEN BRADLEY MICROLOGIX 1000 PROGRAMMABLE LOGIC CONTROLLER

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Abstract: *This paper describes a teaching aid suitable for understanding the basic features of the programmable logic controller by enabling students to develop and implement their own programs for Allen Bradley family controller. Two open-board visual impressive application modules, supplied with function switches and LED status indicators, serve for the verification of design results.*

Keywords: *Control engineering education, Sequential control, Programmable logic controller, Rockwell Software*

1. INTRODUCTION

During the seventies last century, with the appearance and rapid development of the programmable logic controllers (PLCs), the sequential control, which until then has traditionally been realized with relay techniques, has been implemented in software. Namely, the PLC was initially developed by a group of engineers from GENERAL MOTORS in 1968, where the initial specification was formulated: it had to be easy programmed and reprogrammed, easily maintained and repaired, significantly smaller dimensions than its relay equivalent, and cost-competitive with the relay panels then in use [1]-[4]. Programmable Logic Controllers caused great interest of engineers from all disciplines, which resulted in using the PLC for industrial control. A microprocessor-based PLC was introduced in 1977 by ALLEN BREDLEY Corporation in USA, using an Intel 8080 microprocessor with the possibility of handle bit logic instructions at high speed. Recall that the early PLCs were designed only for logic-based sequencing jobs (on/off signals). Today there are hundreds of different PLC models on the market. They differ in their memory (from 256 bytes to several kilobytes), I/O capacity (from a few lines to thousands), as well as in the signal processing possiblies they offer. Certainly, the simplest PLCs serve just as relay replacers with added timer and counter capabilities. More complex controllers, in addition to amplified signals, can also perform simple arithmetic calculations as conventional PId controllers. This is the reason way the letter L can be dropped from acronym PLC, but to be avoided confusion with personal computers (PC), it is not done. In the recent literature can be found some descriptions of the successful implementations of the advanced control strategies based on the industrial PLC platform [5].

At a basic level PLCs are programmed in a simple form of assembly code, but each manufacturer has their own standards and definitions for these codes. There are other programming languages, including the IEC 61131-3 standard, Sequential Function Chart or Function Block Diagrams. However, a long established standard programming language called ″Ladder Diagrams″ is universally understood by PLC programmers. Therefore, at this time ladder logic remains the standard way of PLC program describing. In recent years, PLCs have become more sophisticated, and it is sometimes difficult to put all their features into the ladder logic framework, which gives priority to other alternative programming languages.

This paper deals with a teaching aid perfect for explaining the architecture and way of programming the programmable logic controllers in the laboratory conditions. Active participation of students is stimulated by allowing them to critically analyze the existing solutions and come to the original solutions considering traffic signal control or set of events at automatic work of washing machine.

2. DIDACTIC PLC APPLICATION – HARDWARE AND SOFTWARE ENVIRONMENT DESCRIPTION

Fig.1 shows the photograph of an experimental platform that is used for testing the didactic equipment "FEEDBACK PLC Applications 34-400"[6] in the Laboratory for Control Engineering at the Faculty of Electronic Engineering in Niš. The complete purchase of this laboratory equipment was supported by WUS-Austria [7] under the Grant C.E.P. No.115/02.

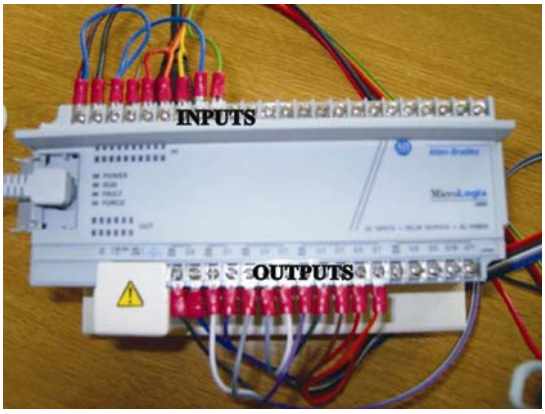
As it is shown in Fig. 1, the experimental setup consists of six functional elements as follows: **1**. Personal computer; **2.** Programmable logic controller; **3.** RS232 communication cable; **4.** Module interface; **5.** Bench-top open-board cross-roads module; **6.** The main window of RSLogix 500 you can expect to see on the monitor immediately after project opening.

Note that to effectively use the necessary software for PLC programming, the personal computer must meet the following hardware and software requirements: Pentium™ or Pentium-compatible microprocessor; 32 MB of RAM and at least 10 MB of available hard disk space; 16-color VGA Graphics Adapter 640×480 or greater resolution (256 color 800×600 optimal); a CD-ROM drive; a 3.5-inch, 1.4 MB disk drive, and any Windows compatible pointing device. The operating system must be one of the following: Microsoft®

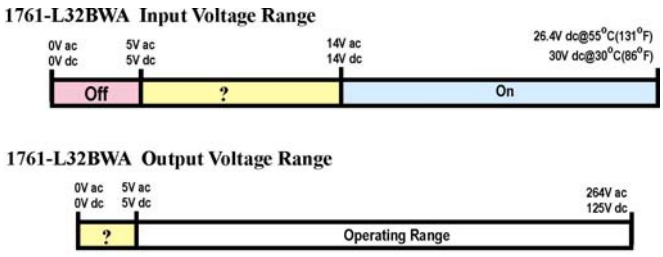
Fig.1. *Photograph of the experimental platform*

Windows® 95/98 or Windows NT 4.0 with Service Pack 4 or greater.

The PLC device Allen Bradley, Micrologix 1000 (part of the platform marked by 2 in Fig.1.) is handily packaged onto a folded metal baseplate, keeping the supply connections safely away from the user. Students are allowed full access to the I/O connections according to the input/output voltage ranges, as is shown in Fig.2 [8].



(a)



(b)

Fig.2. *PLC Allen Bradly, MicroLogix 1000* (type 1761-L32BWA) – *Inputs and outputs* (a) *Wiring example*; (b) *Ranges*

Recall that, after reading status of sensors, the PLC operating system allows controller to perform some arithmetic-logic operations on uploaded data, and in order to implement the control strategy, the processed data are transferred to the output terminals as actuators, indicators etc [9]. This procedure is repeated periodically and any such program passage is one scan cycle. Fig.3 illustrates the scan cycle of five steps: ① Input scan; ② Program scan; ③ Output scan; ④ Communication scan, and ⑤ Maintenance.

During the maintenance operations, various register updates are performed, as well as a number of other tasks that the user does not have to care. During communication scan, the data exchange with other devices connected for PLC is carried out. It is clear that the duration of the program scan depends on the program length and can be calculated easily by addition the instruction times. Typical instruction times and memory usage for Micrologix Controller are given in the Table 1. It is about data related to counter instructions, set on condition and set output instructions, as well as timer instructions. Since it is impossible to change the hardware and software environment, students are able to develop their own programs. After testing logical correctness of the developed program and before uploading program in the memory of the controller, it is suitable to verify whether the available controller meets all memory and real-time requirements.

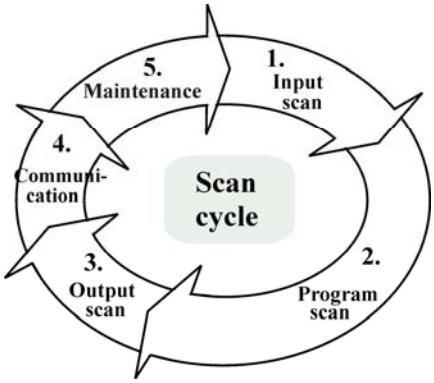


Fig.3. *Scan Cycle* (*Typical values for an Allen-Bradley Micrologix controller: input/output scan time of* $8\,\mu s$; *housekeeping* $180\,\mu s$)

Table 1. *Typical Instruction Times and Memory Usage* [4]

Instruction Type	Time Max[μs]	Time Min[μs]	Memory [words]
CTD - count down	32.19	27.22	1
CTU - count up	29.84	26.67	1
XIC - normally open contact	1.72	1.54	0.75
XIO - normally closed contact	1.72	1.54	0.75
OSR - one shot rising	13.02	11.48	1
OTE - output enable	4.43	4.43	0.75
OTL - output latch	4.97	3.16	0.75
OTU - output unlatch	4.97	3.16	0.75
RES - reset	15.19	4.25	1
RTO - retentive on time	38.34	27.49	1
TOF - off timer	39.42	31.65	1
TON – on timer	38.34	30.38	1

The connection between the computer and programmable logic controller in Fig.1 was achieved with RS232 communication cable. Using interface the prepared ladder program can be uploaded into the memory of the controller, after testing logical correctness of diagram.

The PLC interface (Feedback 34-403) is a box marked by **4** in Fig.1 required to match the voltage levels and to protect some parts of the experimental platform. Namely, the 24V dc line from the PLC is used to provide the +5V dc supply for application module. This module has a connector to accept the ribbon cable from the application module, as well as a group of around thirty screw-in terminals to accept the connection lines from PLC. The interface module between controller and the considered cross-roads module which provides all the required connections to the chosen PLC is shown in Fig.4.

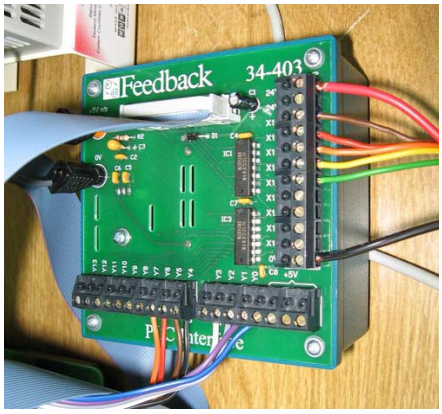
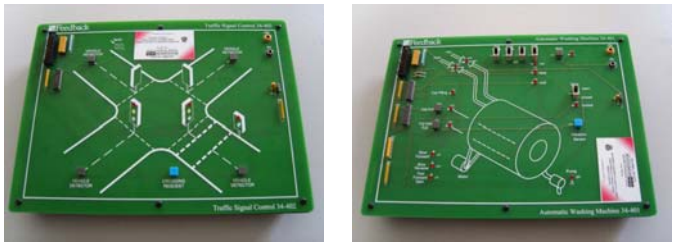


Fig.4. *Module* Feedback 34-403

Both open-board application modules, given in Fig.5, are fiberglass panels with the corresponding mimic diagrams. Each application unit contains function switches and LED status indicators, showing the operation being performed. The practical work associated with these equipments involves the design and implementation of a sequence of PLC programs that exercise all the functions of the module, as follows: demonstration of sequential control, set of the initial process conditions, use of simple interrupts and emergency stop, developing ladder logic programs by programming timers and counters etc. Traffic signal control module (Feedback 34-402) contains traffic and pedestrian control lamp at a crossroads with one pedestrian crossing, in order to allow pedestrians safe crossing as well as quick passage of vehicles in accordance with the detection of their movement direction. Automatic Washing Machine module (Feedback 34-401) is design to be controlled by the chosen PLC for the purpose of providing three wash programs (hot, cool and spin), with the possibility of choice between half and full load [10], [11].

Both units use 5V TTL signals and can be interfaced to a PLC using standard 24V dc logical inputs which implies the use of the interface module.



(a) (b)

Fig.5. *Open-board application modules:*
(a) *Traffic signal control module* Feedback 34-402
(b) *Automatic Washing Machine* Feedback 34-401

A PLC is usually programmed via an external unit; this unit is unnecessary for the PLC operation and may be removed when the PLC is operating. Programming units range from small hand-held portable units, sometimes called "manual programmers", to personal computers. A hand-held PLC programmer (HHP) looks like a large pocket calculator with a number of keys and a simple display. Fig.6 visualizes the connection between programmer and controller. By means of hand-held programmer each logic element of the ladder diagram is entered separately, one at a time, with series or parallel connections achieved by using keys for AND, OR, and NOT. Therefore, it is more convenient for editing the existing, memorized program.

In the case of programming controller via computer, it is necessary to install two ROCKWELL SOFTWARE's [12] programming packages (RSLogix 500 and RSLinx Lite). Note that ROCKWELL SOFTWARE's products are copy-protected. The key is located in an activation file, which is originally located on the Master disk supplied with the RSLogix 500 product. Certainly, it is necessary to look for an alternative solution, because floppy disk is an obsolete data storage medium. Otherwise, the procedure of program installation is not especially different from the usual approach.

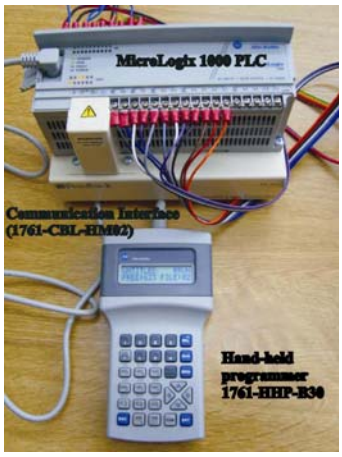


Fig.6. *A hand-held PLC programmer linked with controller*

The RSLogix™ 500 software is a 32-bit Windows® ladder logic programming package for the SLC 500 and MicroLogix processors. It was one of the first PLC® programming software which offers flexibility, reliability, and increased productivity to the industrial controls programming world. This IEC-1131-compliant programming package with easy-to-use editor, diagnostics and troubleshooting tools can help maximize performance, save project development time, and in such a way improve productivity. Programming result is saved as .rss file which contains the corresponding ladder logic diagram.

RSLinx™ is a complete communication server (a set of communication drivers), and can support multiple software applications simultaneously, communicating to a variety of devices on many different networks. RSLinx Lite, which is as a special driver available with RSLogix 500, was used in experiments [13], and some experiences are presented in this paper.

When a project (traf.rss in concrete case) is opened, it can expect to see the result shown in Fig.7. In addition to the usual bars of menu and icon, we can notice a project tree view, which shows all the folders and files contained in the corresponding project. In the part of application window named ladder view it can be shown several program files at the same time, which is useful when editing the ladder logic.

Fig.8 visualize the configuration of system communications, or, in other words, setting RS232 driver, which is a necessary step in establishing a connection between the computer and programmable logic controller. As shown in Fig.8(a), a list of devices available for

connection is displayed in the right (Who Active) pane of the communications window. After the configuration, the driver name appears on the list of drivers (see Fig.8(b)).

RSLinx is available in several versions to meet the cost and functionality requirements of many different applications. It should be noted that the version RSLinx Lite provides only minimum functionality required to support selected software applications from ROCKWELL SOFTWARE and Allen Bradly. This version is not commercially available and does not support Dynamic Data Exchange (DDE).

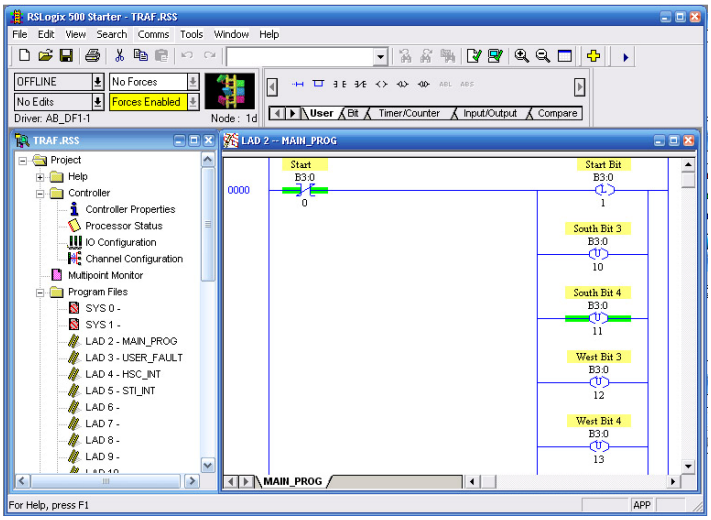


Fig.7. *The main window of RSLogix 500 program*

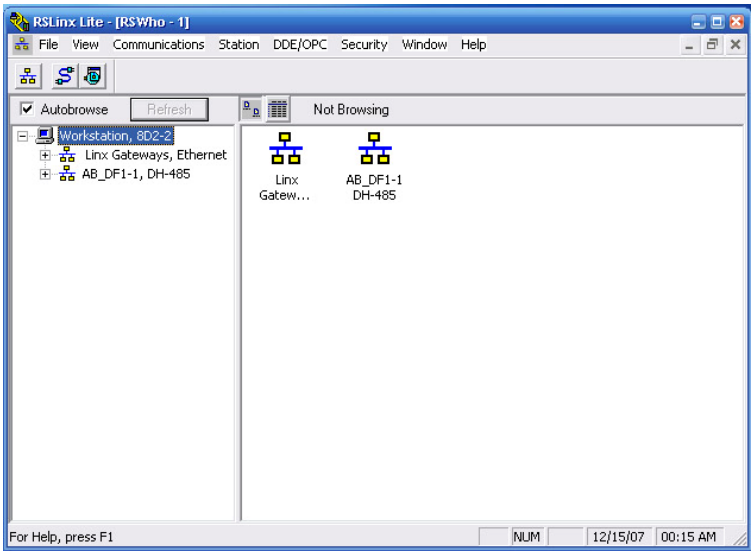


Fig.8. *Configuration of system communications*
(a) Main window;

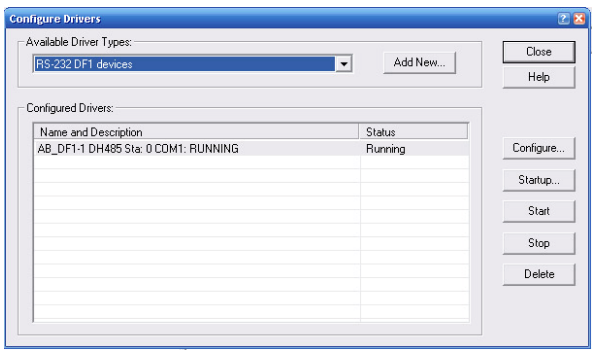


Fig.8. *Configuration of system communications*
(b) Driver configuration

3. CONCLUSION

From an educational viewpoint, "Feedback PLC Applications 34-400" provides opportunities for demonstration of the timed sequence control, allowing the study of basics of PLC programming, the development of ladder logic diagrams by using interrupts, timers, counters etc. Up to now two concrete applications are available: Traffic Signal Control and Automatic Washing Machine. After logic verification of the prepared ladder program and uploading the current offline program into the controller, the user can select the online operating mode in order to verify the validity of whole control system. Because the PLC is designed as a modular system that can connect different input-output modules according of need, it is useful to consider the possibility of enlargement of the list of applications. It is possible to expect the need for advanced control strategies which implementation means the special integration of the starting PLC platform with the additional microprocessor hardware.

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4. REFERENCES

[1] W. S. Levine, *The Control Handbook,* CRC Press, 1996.

[2] W. Bolton, *Mechatronics*, New York: Addison Wesley Longman Publishing, 1995.

[3] N. Matić, *Introduction to Industrial PLC controllers*, MikroElektronika, Beograd, 2001 (in Serbian).

[4] J. Hugh, *Automated Manufacturing Systems*; *PLCs*, http://www.eod.gvsu.edu/~jackh/books/plcs/ (last accessed on October 15th 2008).

[5] S.Gerkšić, G.Dolanc, D.Vrančić, J.Kocijan, S.Strmčnik, S.Blažič, I.Škrjanc, Z.Marinšek, M.Božiček, A.Stathaki, R. King, M.Hadjiski and K.Boshnakov, "Advanced Control Algorithms Embedded in a Programmable Logic Controller", *Control Engineering Practice*, Vol. 14, pp. 935-948, 2006.

[6] Feedback Instruments Limited, http://www.fbk.com/ (last accessed on October 15th 2008).

[7] World University Service (WUS), http://www.wus-austria.org/ (last accessed on October 15th 2008).

[8] MicroLogix™ 1000 Programmable Controllers (Bulletin 1761 Controllers), User Manual, Rockwell International Corporation, USA, 1998.

[9] S. Turajlić, Material from the course "Real-time Control", ETF, Beograd, 2007, http://automatika.etf.bg.ac.yu/files/predmeti/os3urv/materijalipredavanja/plc_komplet_07.pdf (last accessed on October 15th 2008).

[10] *PLC Applications* (*for use with* 34-401 *and* 34-402), Manuel: 34-400, Crowborough: Feedback Instruments Ltd, 2002.

[11] I. Kocić, "Control Applications of PLC Allen Bradly", *Diploma work*, Faculty of Electronic Engineering, Niš, 2004.

[12] *Rockwell Software* http://www.software.rockwell.com (last accessed on October 15th 2008).

[13] A. Arsić, "Traffic Lights System Control with Allen Bradly Micrologix 1000 Programmable Logic Controller", *Diploma work*, Faculty of Electronic Engineering Niš, 2007

DTMF TONE SIGNALIZATION DECODING BASED UPON THE FILTER BANK

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Abstract: *DTMF signalization characteristics are presented in this paper. First, the DTMF signals synthesis, according to ITU-T recommendations Q.23 and Q.24, is described. Synthesis tone frequency signals software implementation is analyzed. Filter bank is used for tone frequency signals decoding. Three filter banks are compared. The first filter bank is composed of second order IIR filters. For IIR cell realization, parallel connection of second order allpass filter and constant equal to minus one, is proposed. The second filter bank is based upon 64th order FIR filter bank realization. The third filter bank uses Goertzel algorithm for quick calculation of DTMF tone signalization discrete Fourier transformation on proposed frequencies.*

Keywords: *DTMF signalization, filter bank, Goertzel algorithm.*

1. INTRODUCTION

DTMF (Dual Tone Multi Frequency) tone signals [1-5] are used for signalization over telephone line in speech frequency range with telephone switchboard. DTMF signalization is the replacement for impulse signalization in telephone networks. DTMF signalization became popular in interactive controling applications such as telephone banking applications or electronic mail systems where a user can select menu options by sending DTMF tones from mobile or fixed telephone device.

In order to detect DTMF tones, IIR and FIR filters are used [5-7] and also algorithms for quick calculation of Fourier transformation, such as Goertzel algorithm [8-9]. New IIR filter bank for DTMF signal detection, based upon parallel connection of allpass filters, is proposed in this paper. This filter bank is compared to FIR filter bank and also to Goertzel algorithm for quick calculation of discrete Fourier transformation.

As first, the technique of DTMF tones synthesis based upon program package MATLAB®, is presented. Then the IIR filter bank cell is described. In order to compare IIR filter bank cell to FIR filter bank cell and Goertzel algorithm, the short description of FIR filter bank cell and Goertzel algorithm is given. Cell comparing is done according to required hardware for realization and detection of DTMF tones corrupted by Gaussian noise. DTMF tones detection in the presence of noise, and also DTMF tones synthesis, are based upon program package MATLAB®. The paper contains MATLAB® program codes for coding, decoding and also the main program for DTMF tones processing.

2. DTMF TONES

DTMF tone is the sum of two singly periodic tones of specific frequency. The frequencies' tones are chosen so that harmonics and intermodulation products will not cause false signals. There is no frequency which is a whole number multiplication of the other frequency, and there is no two frequencies subtraction which is equal to any other frequency. Frequencies can not vary more then $|\Delta f| = 1.5\%$ in regard to its nominal value. Higher frequencies can have the same or greater amplitude then lower frequencies. The amplitude difference beetwen higher and lower frequencies can be up to 3dB.

In DTMF matrix of frequencies, the pair tones are used to represent digits 0-9 and signs #, *, A, B, C and D, as it is shown in Table 1 [10].

Table 1. *Matrix of frequencies.*

Hz	1209	1336	1477	1633
697	1	2	3	A
770	4	5	6	B
852	7	8	9	C
941	*	0	#	D

DTMF tones sampling frequency is $F_s = 8000\,\text{Hz}$. Although there are 16 DTMF signs, telephone devices use only 10 (tones from fourth column and special signs * and # are not used). DTMF standard prescribed that DTMF tone minimal duration is 50ms, and pause between two DTMF tones sending has the same duration.

For tone signal synthesis digital oscillator is used. Singly periodical oscillator implementation is based upon the solution of following difference equation

$$y(n) - 2\cos(2\pi f T_s)y(n-1) + y(n-2) = \sin(2\pi f T_s)x(n-1) \quad (1)$$

where f is digital oscillator frequency. Difference equation (1) solution is obtained using Z-transformation and it has the following format

$$Y(z) = \frac{\sin\left(2\pi\frac{f}{F_s}\right)z^{-1}}{1 - 2\cos\left(2\pi\frac{f}{F_s}\right)z^{-1} + z^{-2}}X(z). \quad (2)$$

Digital oscillator software implementation is very simple using MATLAB® program package.

MATLAB® program code for digital oscillator is:

```
function Y = gensino(f,n,Fs)
% n - must be a vector
% n = 0:dtmf_tonelen-1;
% f = some frequency for the tone to be generated
if nargin < 3, Fs=8000; end
N=length(n);
A = [1 -2*cos(2*pif/Fs) 1];
B = [0 sin(2*pi*f/Fs) 0 ];
Y = impz(B,A,N,Fs);
```

In order to test filter bank, the MATLAB® function for DTMF signal coding is used, which in MATLAB® notation is dtmf_encode(num). Input list num consists of alpha-numerical string which can contain digits, letters A, B, C and D and special signs * and #.

MATLAB® program code for coder is:

```
function EncodedTones = dtmf_encode(num)

 global dtmf_rfreq
 global dtmf_cfreq
 global dtmf_key
 global dtmf_fs
 global dtmf_silencelen
 global dtmf_tonelen

 num = sprintf('%s',num);
 n = 0:dtmf_tonelen -1;
 numcount = length(num);
 tlen = numcount*(dtmf_tonelen + dtmf_silencelen);
 EncodedTones = zeros(1,tlen);

 for i = 1:numcount,
  [row,col] = find(dtmf_key == upper(num(i)));
    if ( isempty(row) )
       disp('One of the Key Pressed')
       disp('is not a valid DTMF Key');
    end
    startpos = (i-1)*(dtmf_tonelen +dtmf_silencelen) + 1;
    endpos =  startpos + dtmf_tonelen - 1;
    EncodedTones(startpos:endpos) = ...
      0.25*gensino(dtmf_cfreq(col),n,dtmf_fs)...
    + 0.25*gensino(dtmf_rfreq(row),n,dtmf_fs);
end
```

DTMF signals time dependence and frequency spectrum, for six digits number 521097, are shown in Fig.1. Tone duration is dtmf_tonelen=2400 samples or 0.30s, and spacing betwwen tones is dtmf_silencelen=1600 samples or 0.20s. Hence, the total DTMF signal duration is 24000 samples or 3s.

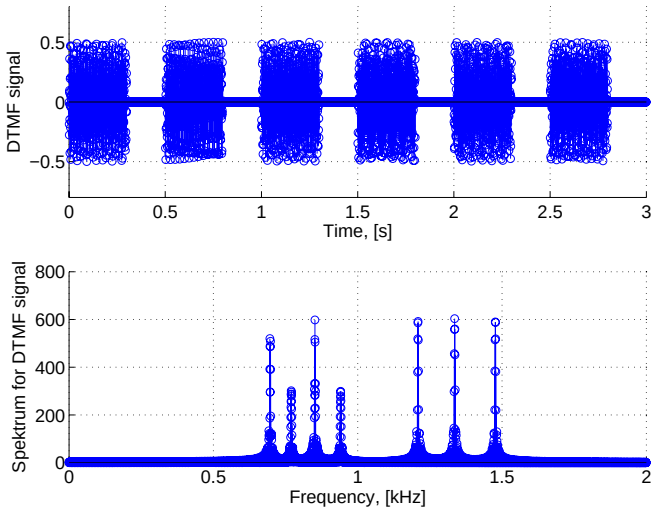

Fig.1. *DTMF signal (Encoded tones), time signal (above) and frequency spectrum (below).*

3. DTMF TONES DECODING

For tone decoding the filter bank is used. Three filter banks are compared. The first filter bank is based upon proposed filter bank realization with infinite impulse response. The second filter bank regards to often applied FIR filter bank [5]. The third filter bank is based upon Goertzel algorithm for discrete Fourier transformation of DTMF tone signalization.

3.1. IIR filter bank

IIR filter bank cell presents modification of stopband filter which is described in [11]. Cell is composed of two allpass filters parallel connection. By replacing one allpass filter with constant $C=-1$, and by adjustment of second allpass filter phase in such a way that, at DTMF tone frequency, phase is $\varphi=180^\circ$, passband filter is obtained. Therefore, filter bank IIR cell consists of allpass filter and constant equal to $C=-1$ parallel connection.

$$H(z)=\frac{1}{2}\left[H_{ap}(z)-1\right] \tag{3}$$

where $H_{ap}(z)$ is allpass filter second order transfer function,

$$H_{ap}(z)=\frac{r^2-2r\cos\theta_1 z^{-1}+z^{-2}}{1-2r\cos\theta_1 z^{-1}+r^2 z^{-2}}, \tag{4}$$

where $z_p=r_1\exp(\pm\theta_1)$ are allpass filter poles.

$$\varphi=\varphi_{num}-\varphi_{den} \tag{5}$$

where

$$\varphi_{num}=\arctan\frac{2r_1\cos\theta_1\sin\theta-\sin 2\theta}{r_1^2-2r_1\cos\theta_1\cos\theta+\cos 2\theta}$$

$$\varphi_{den}=\arctan\frac{2r_1\cos\theta_1\sin\theta-r_1^2\sin 2\theta}{1-2r_1\cos\theta_1\cos\theta+r_1^2\cos 2\theta}.$$

At DTMF signal frequency, $\theta=2\pi f_{dtmf}/F_s$, allpass filter phase displacement need to be equal to $\varphi=180^\circ$. This can be achieved by phase angle θ_1 adjusment, after adopting pole modulus r_1.

Allpass filter discrete realization is shown in Fig.2. Filter coefficients are: $a_1=-2r_1\cos\theta_1$ and $a_2=r^2$.

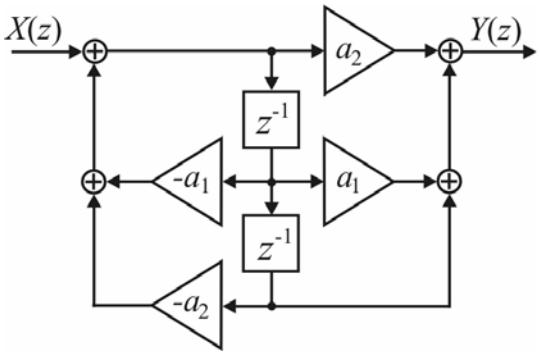

Fig.2. *Second order allpass filter.*

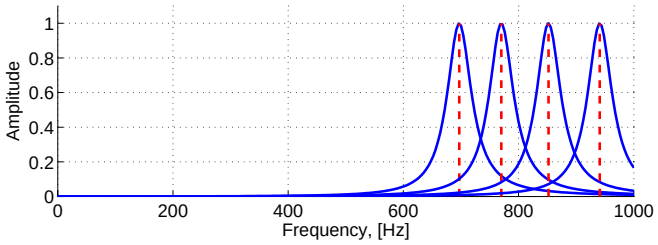

Fig.3. *Second order IIR filter bank.*

Filter bank cell is formed as parallel connection of constant $C=-1$ and second order allpass filter. Required condition for detection is that DTMF tone average power of

the filter output is greater then one fifth of DTMF tone power of the filter input, which can be written in MATLAB® as: mean(encstr_frag2.^2) > mean(encstr_frag.^2)/5. In that way, influence of the DTMF tone amplitude to DTMF signalization decoding, is removed.

3.2. FIR filter bank

It is known that FIR filter transfer function is polynomial (6)

$$H(z)=\sum_{n=0}^{L-1} b_n z^{-n}. \tag{6}$$

Coefficients are determined using following expression

$$b(n)=\frac{2}{L}\cos\left(\frac{2\pi f_p n}{F_s}\right), \text{ for } n=0,1,\ldots,L-1 \tag{7}$$

where L is filter length, f_p is tone signal frequency and F_s is sampling frequency. In order to decode tone frequency signal, filter length $L=64$ is adopted, although for value $L=128$ better results are obtained. Filter impulse response is shown in Fig.4, apropos, FIR filter coefficients are shown. Filter bank amplitude characteristics for tone signals, corresponding to matrix of frequencies columns, are shown in Fig.5.

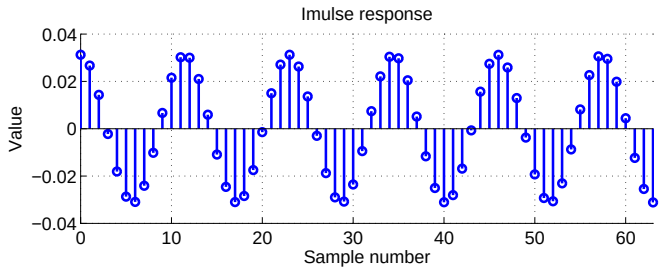

Fig.4. *64th order FIR filter impulse response.*

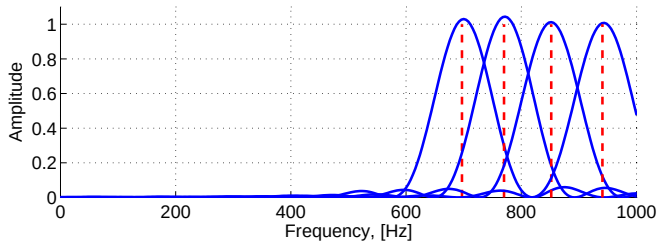

Fig.5. *64th order FIR filter bank.*

3.3. Goertzel filter bank

Goertzel filter bank is based upon second order special discrete cell application, which as a result of samples processing of input signal, $x(n)$, gives Fourier transformation at the output, $y_k(n)=X(k)$ [12, 13]. Difference equation which describes second order Goertzel section can be written as

$$\begin{aligned} y_k(n) &= 2\cos\left(\frac{2\pi k}{N}\right)y_k(n-1)-y_k(n-2) \\ &+x(n)-\mathrm{e}^{\frac{2\pi f_i}{F_s}}x(n-1) \end{aligned} \tag{8}$$

where N is the number of samples needed for one telephone number coding.

By introducing the auxiliary variable, $w_k(n)$, equation (8) is separated into recursive and nonrecursive part

$$\begin{aligned} w_k(n) &= 2\cos\left(\frac{2\pi k}{N}\right)w_k(n-1)-w_k(n-2)+x(n) \\ y_k(n) &= w_k(n)-\mathrm{e}^{\frac{2\pi f_i}{F_s}}w(n-1) \end{aligned} \tag{9}$$

where initial conditions for variable $w_k(n)$ are equal to zero. The advantage of this kind of expressioning is that nonrecursive part is calculated at N times lower sampling frequency because

$$X(\theta_k)=y_k(n)\big|_{n=N}=y_k(N). \tag{10}$$

Therefore, for discrete Fourier transformation calculation there are $N+2$ real multiplications and $2N$ real summings.

Second order Goertzel cell transfer function is given by expression

$$H_{f_i}(z)=\frac{1-\mathrm{e}^{\frac{2\pi f_i}{F_s}}z^{-1}}{1-2\cos\frac{2\pi f_i}{F_s}+z^{-2}}. \tag{11}$$

Goertzel algorithm scheme is shown in Fig.6.

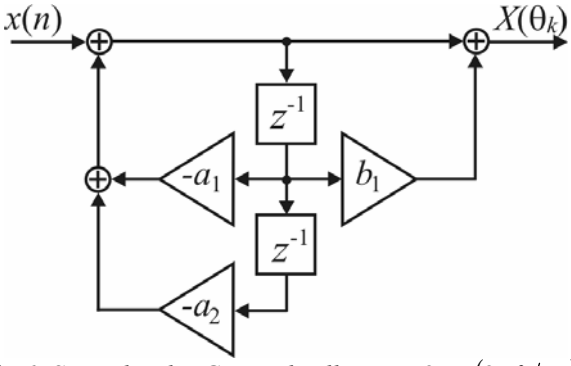

Fig.6. *Second order Goertzel cell:* $a_1=-2\cos(2\pi f_i/F_s)$, $a_2=1$, $b_1=\mathrm{e}^{-2\pi f_i/F_s}$.

In general case, DTMF signal discrete frequencies $\theta_k=2\pi f_k=2\pi kF_s/N$ do not coincide to frequencies in which Fourier transformation is calculated. Lower absolute difference, bigger number N of samples which have to be processed. Frequency indexes, absolute and relative error for all DTMF signals, when one DTMF signal minimal duration is 30ms or $N_{\min}=2400$, are given in Table 2.

For DTMF signals decoding MATLAB® function Y =goertzel(x,k+1) is used. Calculation is done only at one point which corresponds to DTMF signal frequency index. Frequency index values, k, for all DTMF signals when number of samples is $N=2400$ and sampling frequency is $F_s=8\,\mathrm{Hz}$, are given in Table 2. Beside the whole number value of frequency index, k, Table 2 contains its accurate value, $\tilde{k}$, absolute error, Δk, and relative error, ε.

DTMF signal and frequency spectrum for digit one are shown in Fig.7. Signals of frequencies $f_1=697\,\mathrm{Hz}$ and $f_5=1209\,\mathrm{Hz}$ are used for digit one, which means, according to Table 2, that frequency indexes for those

frequencies are 209 and 363. DTMF tone contains 2400 samples. Frequency spectrum is calculated only for two frequency components which correspond to frequency indexes of DTMF tone.

Table 2. *Frequency indexes of DTMF signals for* $F_s = 8\,\text{Hz}$ *and* $N = 2400$.

f_k[Hz]	$\tilde{k}$	k	Δk	ε[%]
697	209.1	209	0.100	0.0478
770	231.0	231	0	0
852	255.6	256	0.400	0.1565
941	282.3	282	0.300	0.1063
1209	362.7	363	0.300	0.0827
1336	400.8	401	0.200	0.0499
1477	443.1	443	0.100	0.0226
1633	489.9	490	0.100	0.0204

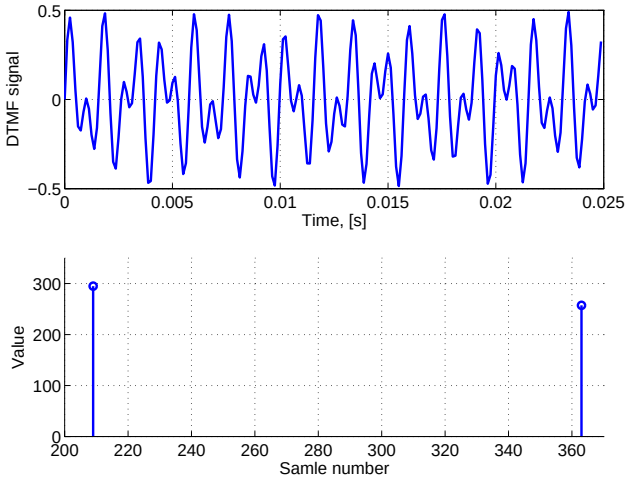

Fig.7. *DTMF signal at the Goertzel cell input (above) and DTMF signal frequency spectrum (below).*

Fig.7 shows that signals can be simply decoded by investigating if the amplitude of spectral component of DTMF tone of output Goertzel cell, is larger then proposed value.

Since calculation is done only for one frequency, spectrum leakage does not influence the detected signal. MATLAB® script of decoder for tone frequency signals is written for IIR filter bank. By replacing IIR filter bank with FIR filter bank or by Goertzel cell for Fourier transformation DTMF signal, MATLAB® program can be simply rearranged for detection of DTMF signals using described filter banks.

MATLAB® program code for decoder is:

```
function digitstr = dtmf_decode(encstr)
 global dtmf_rfreq
 global dtmf_cfreq
 global dtmf_fs
 global tmf_silencelen
 global dtmf_tonelen
 global dtmf_key
 r=0.98;
 dtmf_digilen = length(encstr)/...
   (dtmf_tonelen+dtmf_silencelen);
 for deco_seq = 1:dtmf_digilen
    startpos = (deco_seq - 1)*(dtmf_tonelen ...
       + dtmf_silencelen) + 1;
    endpos = startpos + dtmf_tonelen - 1;
    encstr_frag = encstr(startpos:endpos);
    for i = 1:4;
       [B,A]=IIRbank(dtmf_rfreq(i),r,dtmf_fs);
       encstr_frag2=filter(B,A,encstr_frag);
       ss = mean(encstr_frag2.^2) > ...
          mean(encstr_frag.^2)/5;
                if (ss)
          row = i;
          break
       end
    end
    for i = 1:4;
       [B,A]=IIRbank(dtmf_cfreq(i),r,dtmf_fs);
       encstr_frag2=filter(B,A,encstr_frag);
       ss = mean(encstr_frag2.^2) > ...
          mean(encstr_frag.^2)/5;
       if (ss)
          col = i;
          break
       end
    end

 numstr(1,deco_seq) = dtmf_key(row,col);
 end
 digitstr = numstr;
```

4. NOISE INFLUENCE TO TONE SIGNALIZATION DECODING

For analysis of noise influence to DTMF signals detection, the Gaussian noise is adopted, and then tone signalization for decoding is

$$x_n(n) = x(n) + \sigma\, g(n), \tag{12}$$

where $g(n)$ is Gaussian possibility density which average value is equal to zero and standard deviation equal to one, σ is standard deviation and $x(n)$ is DTMF signal corrupted by Gaussian noise. MATLAB® function used for calculation Gaussian possibility density is randn(1,N). This corrupted DTMF signal is processed by DTMF signal decoder. All three types of filter banks are compared.

The main program includes subprogram for DTMF signal coding and decoding.

```
clear all; close all;
 global dtmf_rfreq
 global dtmf_cfreq
 global dtmf_key
 global dtmf_fs
 global dtmf_silencelen
 global dtmf_tonelen
 dtmf_rfreq = [ 697 770 852  941];
 dtmf_cfreq = [1209 1336 1477 1633];
 dtmf_key = [ '1' '2' '3' 'A';
              '4' '5' '6' 'B';
              '7' '8' '9' 'C';
              '*' '0' '#' 'D' ];
 dtmf_fs = 8000;
 disp(['DTMF samplerate set to  ' num2str(dtmf_fs) ' Hz']);
 dtmf_tonelen = round(dtmf_fs * 0.30);
 disp(['DTMF tone length set to ...
       ' num2str(dtmf_tonelen) 'samples']);
 dtmf_silencelen = round(dtmf_fs * 0.20);
 disp(['DTMF break length set to ...
       ' num2str(dtmf_silencelen) ' samples']);
 num='531097';
 EncodedTones = dtmf_encode(num);

 N = length(EncodedTones);
 sigma=0.4;
```

```
g=randn(1,N);
EncodedTones=EncodedTones+sigma*g;
digitstr = dtmf_decode(EncodedTones)
```

5. CONCLUSION

Three filter banks are analyzed for DTMF signal detection: IIR filter bank, FIR filter bank and Goertzel filter bank. The following conclusions can be obtained:

1) If hardware is considered, FIR filter bank requires the biggest number of multipliers and adders. Satisfactory selectivity is achieved with 64^{th} order cell. IIR filter cell and Goertzel cell are of the second order and therefore they require less hardware.
2) FIR and IIR cell coefficients are the real numbers while coefficient in Goertzel cell numerator is a complex number. Signal processing using Goertzel cell is more complicated in regard to IIR cell.
3) With Gaussian noise standard deviation increasing, decoders with FIR and IIR filter banks have more similar characteristics. For value $\sigma > 0.3$ decoders are not able to detect DTMF signal, but Goertzel cell decodes DTMF signal precisely for $\sigma = 0.5$. It is used 500 DTMF numbers for simulation.
4) Noise influence to DTMF signal decoding in Goertzel cell can be controlled by detection step selection. The bigger the detection step, the lower the noise influence to decoding.

6. REFERENCES

[1] International Telecommunication Union, ITU-T Recommendation Q.23, "Technical features of push-button telephone sets", Fascicle VI.1, Blue Book, 1993.

[2] International Telecommunication Union, ITU-T Recommendation Q.24, "Multifrequency push-button signal detection", Fascicle VI.1, Blue Book, 1993.

[3] International Telecommunication Union, ITU-T Recommendation Q.454, "The sending part of the multifrequency signaling equipment", Fascicle VI.4, Blue Book, 1993.

[4] International Telecommunication Union, ITU-T Recommendation Q.454, "The receiving part of the multifrequency equipment", Fascicle VI.4, Blue Book, 1993.

[5] Kikuchi and H. Kitano and J. Matsuda, "A study on digital pushbutton signaling receiver", Review of Electr. Commun. Lab., vol. 27, no. 7-8, August 1979, pp.630-641.

[6] F. Braun, "Nonrecursive digital filters for detecting multifrequency coded signals", IEEE Trans. Acoust. Speech, Signal Process., vol. 23, no. 3, June 1975, pp.250-256.

[7] Thyssens and L. Verbist, "Digital multifrequency receivers and senders", Electr. Commun., vol. 54, no. 4, 1979, pp.319-325.

[8] I. Koval and G. Gara, "Digital MF receiver using Discrete Fourier transform", IEEE Trans. Commun., vol. 21, no. 12, December 1973, pp.1331-1335.

[9] P. Mock, "Add DTMF generation and decoding to DSP μP designs", EDN, vol. 30, March 1985, pp.205-220.

[10] M. Popović, "Efficient decoding of digital DTMF and R2 tone signalization", Facta Universitatis, Ser.: Elec. and Energ., vol. 16, no. 3, 2003, Available: http://factaee.elfak.ni.ac.yu/fu2k33/9mp.pdf

[11] Goran Stančić, Darko Ilić and Vlastimir Pavlović, "Uskopojasni rekurzivni digitalni filtar nepropusnik frekvencija", Proc. 14th Telecommunications forum TELFOR 2006, Serbia, Belgrade, November 21-23, 2006, pp.337-340.

[12] S.Gay, J. Hartung and G. Smith, "Algorithms for multichannel DTMF detection for the WE® DSP32family", Proc. IEEE Int. Conf. Acoust. Speech, Signal Processing, vol. 2, Glasgow, UK, May 1989, pp.1134-1137.

[13] A. Dabrowski, "Modified Goertzel algorithm for detection of DTMF signals", Proc. Int. Conf. on Signal and Systems, Algiers, Algeria, September 1994, IV.1-IV.3.

DESIGN AND SIMULATIONS OF FRACTAL HIGH-IMPEDANCE SURFACES FOR MODERN WIRELESS COMMUNICATION SYSTEMS

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Abstract: *Unlike the conventional conductive surfaces, high-impedance surfaces (HIS) exhibit reflection coefficient $\Gamma \approx +1$, i.e. they do not change the phase of the reflected wave. Such structures are used in modern wireless communication systems, especially in the antenna design. HIS comprises of a great number of unit cells with sub-wavelength dimensions. Due to this fact, the concept of artificial effective media can be applied and HIS can be described using one parameter, the effective surface impedance. Unit cells are basically resonant LC circuits, whose parameters determine the operating frequency of HIS. Conventional HIS geometries, such as so called mushroom structures do not offer wide range of values of the inductance and the capacitance of the unit cell. This can be overcome by the application of fractal geometries, which allow much greater freedom in the choice of the unit cell parameters. In this paper, HIS that uses Hilbert fractal curves are analyzed. Advanced simulation techniques of HIS are presented, based on the usage of modern commercially available EM simulation tools.*

Keywords: *High impedance surface, mushroom structure, fractal curves, Hilbert curve.*

1. INTRODUCTION

Conductive surfaces are useful as reflectors, but they reverse the phase of reflected waves, [1]. A flat metal sheet, which is used in many antennas as a reflector or ground plane, redirects half of the radiation into the opposite direction, improving the antenna gain. However, if the antenna is too close to the conductive surface, the phase of the impinging wave is reversed upon reflection, resulting in destructive interference with the wave emitted in the other direction, shown in Fig.1.

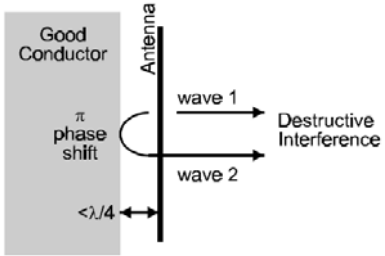


Fig.1. *Destructive interference of reflected and emitted waves*

Another property of metals is that they support surface waves that are nothing more than AC currents at microwave frequencies. By applying special structures these problems could be efficiently solved.

2. HIGH IMPEDANCE SURFACES

High-impedance surfaces (HIS), also known as artificial magnetic conductors, are structures which exhibit reflection coefficient $\Gamma \approx +1$ (expression 1), i.e. they do not change the phase of the reflected wave, [2]. Such structure is comprised of a great number of unit cells with sub-wavelength dimensions. Due to this fact, the concept of artificial effective media can be applied and HIS can be described using one parameter, the effective surface impedance. Unit cells are basically resonant LC circuits, whose parameters determine the operating frequency of HIS. In the vicinity of the resonant frequency, HIS is characterized by having very high impedance, shown in Fig.2, which results in reflection coefficient of $\Gamma \approx +1$ and zero degree reflection phase, depicted in Fig.3. Also, in a forbidden frequency band, HIS does not support freely propagating surface currents.

$$\Gamma = \frac{Z_2 - Z_1}{Z_2 + Z_1} \tag{1}$$

Since materials that exhibit very high impedance do not exist in nature, HIS has been realized artificially and there are different design approaches of them.

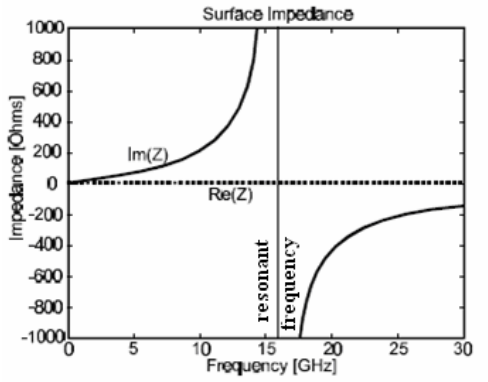


Fig.2. *Impedance of HIS*

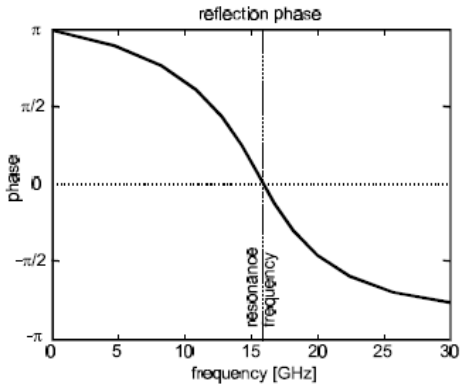


Fig.3. *Reflection phase*

3.HIGH IMPEDANCE SURFACES WITH MUSHROOM-TYPE UNIT CELLS

So-called mushroom structure, described and analyzed in [1], is based on mushroom-type unit cells and nowadays it presents conventional structure of HIS. Mushroom-type unit cell consists of metal patch connected to the ground plane by a via through a dielectric slab. Fig.4 shows an example of a mushroom structure in which metal patches have hexagonal shape.

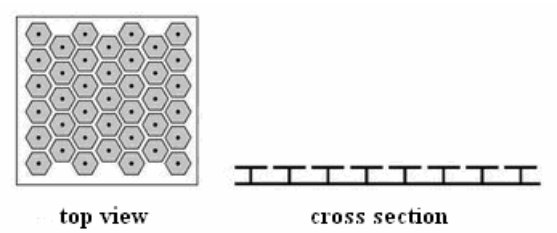


Fig.4. *A mushroom structure with hexagonal metal plates*

When the structure interacts with electromagnetic waves, currents are induced in the metal plates. Associated with these currents is a magnetic field, and thus an inductance. Also, charge is built up on the ends of the plates which can be described as a capacitance. Therefore, every unit cell represent resonant circuit and the behavior of the structure can be reduced to parallel LC circuit, where L and C stands for total inductance and capacitance, respectively, of the structure.

The edge capacitance between two plates, which are surrounded by ε_1 on one side and ε_2 on the other, could be expressed as

$$C = \frac{w(\varepsilon_1 + \varepsilon_2)}{\pi} \cosh^{-1}\left(\frac{a}{g}\right), \qquad (2)$$

where w is plate width, g is separation of the plates and a is separation between their vias.

Sheet inductance is given by inductance of solenoid whose length to width ratio is taken as unity, thus it depends only on the thickness of the structure and the permeability.

$$L_s = \mu t. \qquad (3)$$

Resonant frequency is given by the following expression:

$$\omega_0 = \frac{1}{\sqrt{LC}}. \qquad (4)$$

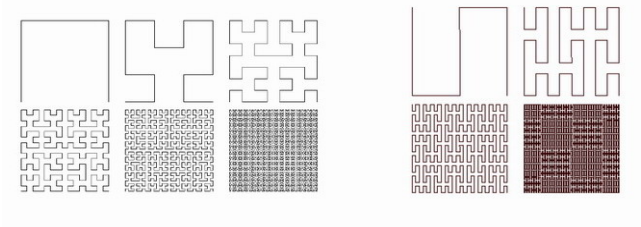
It can be seen from (4) that the resonant frequency can be lowered by increasing either the inductance or the capacitance. Since high-permeability materials do not currently exist at microwave frequencies, the inductance cannot be significantly increased without significant change in the dimensions of the structure. As the capacitance depends on the dimensions of the unit cell, value cannot either be particularly increased since it would undermine the concept of this structure, that is much smaller period of the surface texture than the wavelength of the propagating waves.

We can conclude that the drawback of the mushroom structure is that it does not offer a wide range of values of the inductance and the capacitance of the unit cell, and thus it does not offer a wide range of operating frequency.

In [1] the roles of the ground plane and conducting vias in HIS were also reviewed. If there were not the vias and the ground plane, currents that are responsible for existence of inductance would not propagate. Hence, there would not be the impedance which corresponds to parallel resonant circuit.

4. UNIT CELLS WITH FRACTAL CURVE GEOMETRY

Fractal curves are infinitely long lines which, at the same time, fit into the finite area, [3]. That means that width of a fractal line has to be infinitely small. Since it is not possible to physically realize such a line, in practice we use pre-fractals – fractal curves that are built with finite number of iterations (that are obtained after finite number of iterations), i.e. fractal curves of finite order. Such lines do not occupy the whole area and their width is not infinite. Fig.5. shows several first iterations of some of well-known fractals.



First six fractal iterations for the Hilbert-curve geometry

First four fractal iterations for the Peano-curve geometry

Fig.5. *Hilbert and Peano fractal curves*

In comparison with homogenous metal plates, the main advantage of unit cells that have pre-fractal geometry lies in the fact that finite order fractal curve which has the same footprint size as metal plate has a considerable higher inductance, while its capacitance to ground plane remains practically unchanged. As the iteration order of these curves increases, they maintain their footprint size which implies that the length of fractal curve can vary within the same area. The higher the order of a fractal curve is, the greater the length of the fractal curve is as well as its inductance. By increasing the order of a fractal curve it becomes more and more similar to a homogenous metal plate, and thus has greater capacitance.

It can be concluded that by varying the length of a fractal curve we can change the unit cell parameters and preserve the area that it occupies.

5. HIGH IMPEDANCE SURFACES WITH THE THIRD ORDER HILBERT FRACTAL CURVES

In [4] the structure which is based on the third order Hilbert fractal curves, is described and analyzed, shown in Fig.6. The structure consists of Hilbert curve inclusions which are arranged in a 2D periodic array whose dimensions are 7 x 3. Dimensions of the Hilbert curve footprint are 12 x 12 mm. 2D periodic arrangement is designed on FR-4 substrate with $\varepsilon_r = 4.4$, $h = 1.575$ mm and $tg\delta = 0.02$.

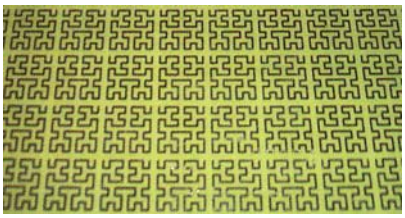


Fig.6. *The high impedance surface with the third order Hilbert curve inclusions*

In order to analyze this structure, electromagnetic simulations were performed and for that purpose the structure was placed in the waveguide WR-430, 5 mm from the short circuited end of the waveguide, as Fig.7. depicts. Since the high impedance surface is placed on substrate whose thickness is 1.575 mm, the 2D periodic arrangement is 6.575 mm from the short circuited end.

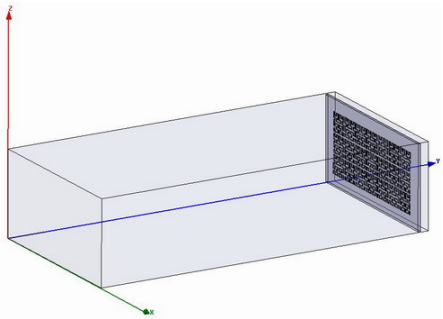


Fig.7. *The simulation model of the high-impedance surface with the third order Hilbert curve inclusion*

Fig.8 shows the magnitude and phase of the reflection coefficient as a function of the frequency, for this structure.

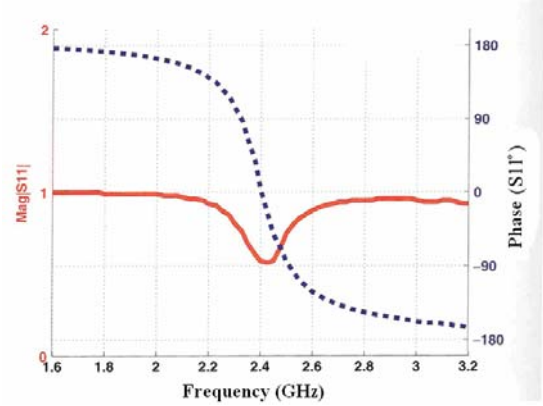


Fig.8. *Simulated results of the structure from [4]*

We can see from the simulation results that the value of the frequency at which the reflection phase crosses through zero is 2.4 GHz. At the same frequency attenuation of the magnitude of the reflection coefficient occurs. In [4] the attenuation is considered to be due to the losses in the substrate.

Apart from the results, it should be noted that the structure from [4], unlike the structure from [1], does not have a ground layer nor vias that would connect the unit cells with the ground plane. Furthermore, in [4] it is not discussed whether vias and a ground layer are necessary in HIS, nor why the structure comprised of the lattice of the unit cells and the dielectric substrate only was chosen to analyze. However, it is important to notice that although the structure itself does not have a ground layer, there is such layer in the analyzed model – the short circuited end of the waveguide.

6. SIMULATION RESULTS

The structure described in the previous section was used as a basis for the research carried out in this paper.

In order to prove the results from [4] and analyze influences of different parameters, electromagnetic simulations were performed by using HFSS (High Frequency Structure Simulator). Also, the same dimensions as those from [4] were used.

The basic model, which is shown in Fig.7, is comprised of: a two-dimensional lattice of unit cells, the substrate on which the lattice is designed, and a waveguide. The shape of the unit cell is the third order Hilbert fractal curve and the dimensions of the unit cell footprint are 12 x 12 mm. The line width is 0.55 mm, and the separation between lines is twice as wide as the line width. In the simulations the boundary condition "*perfect E*" was applied to the unit cells, i.e. the unit cells were assumed to be made of perfect conductor. The two-dimensional lattice of unit cells consists of Hilbert curve inclusions which are arranged in a 2D periodic array whose dimensions are 7 x 3. The separation between the unit cells is 1 mm and they are not galvanic coupled. Dimensions of the substrate are 108.22 x 53.61 x 1.575 mm, where 1.575 mm presents the substrate thickness. Dielectric constant and loss tangent of substrate are 4.4 and 0.02, respectively. The dimensions of the waveguide are 109.22 x 54.61 mm, while its length is 220 mm. The substrate with the lattice is positioned 5 mm from the short circuited end of the waveguide, and 0.5 mm from the each side of the waveguide, which means that the lattice is placed 6.575 mm from the end of the waveguide.

The frequency range from 1.6 GHz to 3.2 GHz was analyzed. Fig.9 shows the magnitude of the reflection coefficient as a function of the frequency.

It can be seen that the magnitude of the reflection coefficient dependence is very similar to those from [4] – in the vicinity of 2.5 GHz the magnitude of the reflection coefficient is evidently smaller than maximum.

The aim of the next step was to analyze the influence of the position of the substrate in the waveguide on the reflection coefficient.

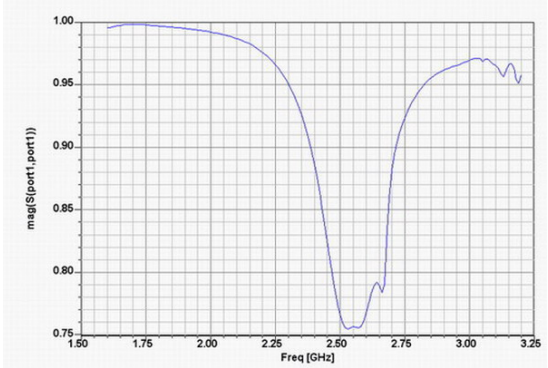


Fig.9. *Magnitude of the reflection coefficient*

Three models which differ in the distance of the substrate from the short circuited end of the waveguide were simulated. In the first case the distance was 5 mm, in the second 2 mm, while in the third case the substrate coincides with the end of the waveguide. The magnitude of the reflection coefficient dependences on frequency for all three cases are depicted in Fig.10, 11 and 12.

In the first case the magnitude is slightly different from the magnitude of the basic model. However, when the separation between the substrate and the short circuited end is 2 mm, the frequency band in which the magnitude attenuates becomes narrower. At the same time, that attenuation is significant, even twice greater than in the first case. Also, the resonant frequency does not change. In the third case, when the lattice and the short circuited end of the waveguide are separated only by the substrate, the resonant frequency shifts to lower frequencies. The frequency band in which the magnitude attenuates, is narrower than in the first case, while attenuation is greater althoug not as much as in the second situation.

In the first case, space between the Hilbert curve inclusions and the short circuited end of the waveguide consists of the dielectric layer and the part between the substrate and the short circuited end of the waveguide which

is filled with air, and which length is 5 mm. Effective permittivity of the space between the unit cells and the ground layer is less than permittivity of substrate. In the second case the layer filed with air is smaller and effective permittivity is slightly greater than it is in the previous case. This model exhibit significant increasing in attenuation in the stopband. In the third case, effective permitivitty is equal to permitivitty of the substrate, and thus greatly differs from those in the previous two cases, which explains the variation in the resonant frequency.

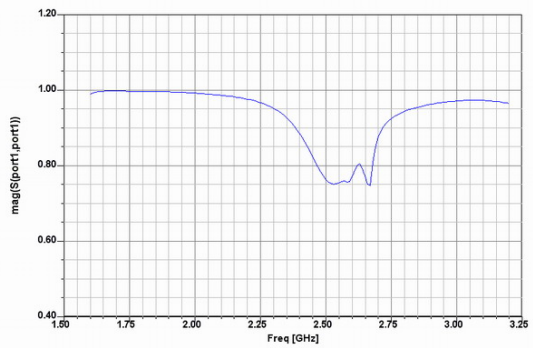


Fig.10. *Magnitude of the refl. coeff. in case the separation between the substrate and the end of the waveguide is 5 mm*

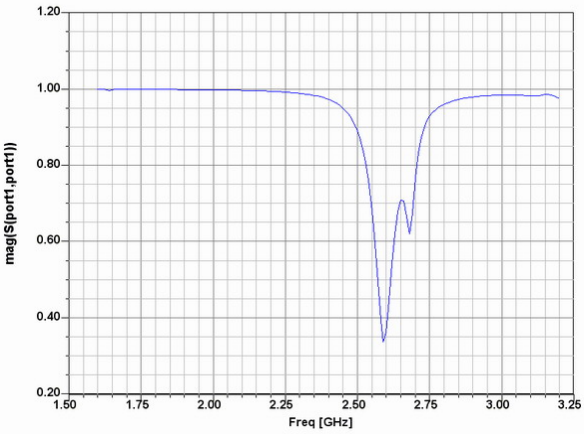


Fig.11. *Magnitude of the refl. coeff. in case the separation between the substrate and the end of the waveguide is 2 mm*

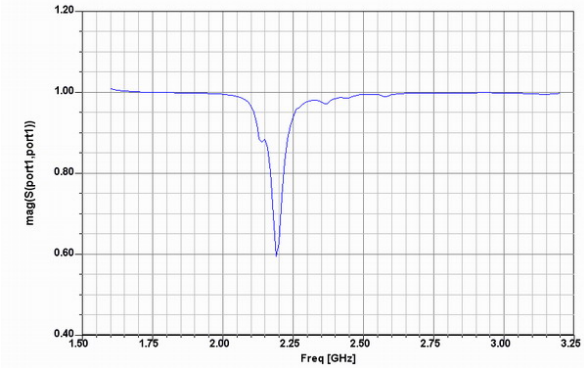


Fig.12. *Magnitude of the refl. coeff. when there is no distance between the substrate and the end of the waveguide*

7. INFLUENCE OF THE GROUNDING OF THE UNIT CELLS

For the purpose of the analysis of the influence of adding vias between the unit cells and the ground layer, the third model from previous section with vias between the Hilbert curve inclusions and the ground plane, was simulated. Fig.13 shows this structure, while Fig.14 depicts the simulation results for it.

One can see that adding vias does not change the nature of the circuit in essence, that is the reflection coefficient still has minimum at the resonant frequency. Though, due to change in total inductance and capacitance, the resonant frequency has shifted, and it has value of 2.75 GHz. By the grounding of the unit cell, parallel inductance in the equivalent circuit of the structure occurs. By suitable choice of the values of circuit elements the structure can perform *left-handed* behavior.

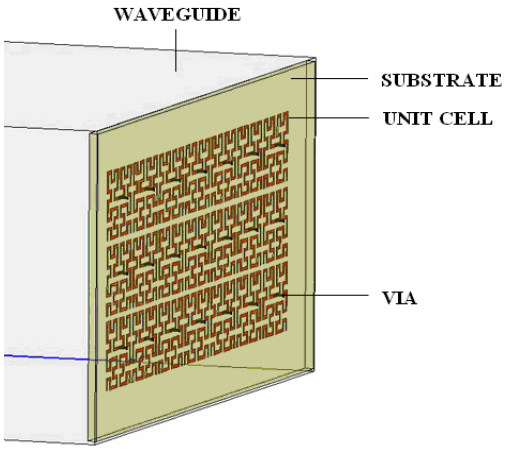


Fig.13. *The structure with vias between the unit cells and the ground layer*

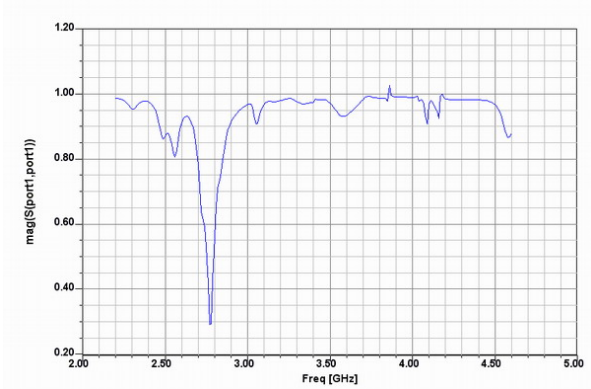


Fig.14. *Simulated results of the structure with vias between the unit cells and the ground layer*

8. CONCLUSION

In this work, high impedance surfaces with conventional and Hilbert fractal unit cells have been analyzed. Owing to its specific features HIS can offer interesting applications in the compact antenna with high directivity design.

It has been shown that changes in position of the substrate with 2D lattice of unit cells in relation to short circuited end of the waveguide, causes significant attenuation of the magnitude of the reflection coefficient in the vicinity of the resonant frequency as well as change in resonant frequency, which contradicts the statement from [4] that these structures can operate without ground layer.

Also, it has been shown that adding vias between unit cells and short circuited end does not change the nature of the circuit in essence, i.e. the reflection coefficient still has minimum at the resonant frequency. Though, due to change of total inductance and capacitance, the resonant frequency

has shifted. By suitable choice of the values of circuit elements the structure which would perform *left-handed* behavior can be designed.

9. REFERENCES

[1] Daniel Frederic Sievenpiper, "High-Impedance Electromagnetic Surfaces", *PhD Thesis in Electrical Engineering, University of California*, Los Angeles, 1999.

[2] John McVay, Nader Engheta, Ahmad Hoorfar, "High-impedance metamaterial surfaces using Hilbert-curve inclusions," *IEEE Microwave and Wireless Components Letters*, Vol. 14, pp. 130-132, March 2004

[3] Vesna Crnojević-Bengin, "Novel configurations of fractal and LH microstrip resonators", *PhD Thesis, Faculty of Technical Sciences*, Novi Sad, february 2006

[4] Nader Engheta, Richard W Ziolkowski, "Metamaterials: Physics and Engineering Explorations," IEEE Press, Wiley-Interscience, 2006.

OPTIMAL AND ROBUST TUNING OF THE PI CONTROLLER BASED ON THE MAXIMIZATION OF THE CRITERION J_C DEFINED BY THE LINEAR COMBINATION OF THE INTEGRAL GAIN AND THE CLOSED-LOOP SYSTEM BANDWIDTH

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Abstract: *This paper presents a new, simple and effective, optimization of the PI controller under constraints on the robustness. The optimization is based on the maximization of the combined performance criterion $J_C=\beta k_i+(1-\beta)\omega$, where k_i is the integral gain, $0\leq\omega<\infty$ is the frequency and β is a free parameter in the range $0<\beta\leq 1$. Constraint is defined by the maximum sensitivity M_s, as a tuning parameter in the range $1.4\leq M_s\leq 2$. For $\beta=1$ and $J_C=k_i$ one obtains Åström, Panagopoulos, Hägglund's (APH) design of PI controller based on non-convex optimization. On a large test batch representing stable, integrating and oscillating processes, including dead-time, it is demonstrated that the method proposed here guarantees better tradeoff between performance and robustness than the APH method, the best one proposed until now.*

Keywords: PI controller, Optimization, Robustness

1. INTRODUCTION

The PID controllers, in single and cascade loops, or combined with the Smith predictor, are still mostly used control systems. Even more than 94% regulatory controllers have the PID structure [1,2,3]. Because of such widespread use of PI/PID controllers, development of simple and effective tuning rules is still in progress [3,4,5]. However, during the last ten years, considerable efforts have been oriented towards the optimization of the PI/PID controllers [6-12], in order to minimize *IAE* (Integrated Absolute Error) under constraints on the robustness. The reason for this choice of the performance index is the fact that most of the PI/PID controllers operate as regulators and the step load disturbance-rejection performance index *IAE* is of primary importance to evaluate performance of the industrial controllers [13]. Recently, fractional-order PI/PID controllers are also investigated [14-18] as a way to find a better tradeoff between performance and robustness.

The choice of studying, in this paper, optimization of the PI controllers evolves from the fact that the derivative action is turned off in the large percent of industrial applications. The control system structure from [6], presented in Fig.1, is used here. In [6-9] the constrained optimization of the PI/PID controllers is based on the maximization of the integral gain k_i, starting from the fact that, if the error $e(t)=y_{sp}(t)-y(t)\geq 0$, then

$$IAE = IE = \int_0^\infty e(t)dt = 1/k_i\,. \tag{1}$$

According to (1) maximization of the integral gain k_i is equivalent to the minimization of *IAE*= *IE*.

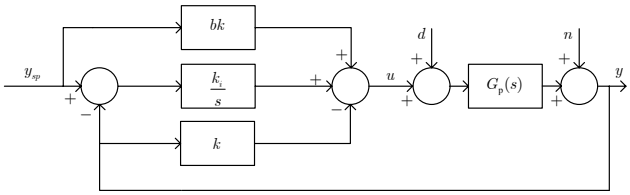

Fig.1. *Plant* $G_p(s)$ *with PI controller*

In the present paper, for the same maximum sensitivity M_s, an improvement of the tradeoff between the performance, small *IAE*, and robustness, small maximum complementary sensitivity M_p, is obtained by applying the combined performance criterion J_C defined by the relation

$$J_C = \beta k_i + (1-\beta)\omega\,, \tag{2}$$

where $0\leq\omega<\infty$ is the frequency and β is a free parameter in the range $0<\beta\leq 1$. Constraint is defined by the desired value of the maximum sensitivity M_s, which is a tuning parameter in the range $1.4\leq M_s\leq 2$, as in [6,7].

2. OPTIMAL AND ROBUST TUNING BASED ON THE MAXIMIZATION OF THE CRITERION J_C

The loop transfer function $L(s)$ is given by the relation

$$L(s) = \gamma\frac{ks+k_i}{s}G_p(s) = C(s)G_p(s)\,. \tag{3}$$

where $k>0$, $k_i>0$ and $\gamma=1$ when the process gain is greater than zero or $\gamma=-1$ when the process gain is less than zero. Parameter b describes the feed forward from the set point y_{sp} to control signal u and will not be considered here. When k and k_i are determined, b can be tuned as in [6].

The tuning parameter M_s defines the maximum sensitivity, given by the relation

$$M_s = \max_\omega |S(j\omega)| = \max_\omega |1/(1+L(j\omega))|\,, \tag{4}$$

where $S(s)$ is the sensitivity function, which shows the effect of feedback. Denoting by $y_{OL}(t)$ the response of the open-loop system in Fig.1, the closed-loop response $y(t)$ in Fig.1 is given by

$$Y(s) = S(s)Y_{OL}(s)\,. \tag{5}$$

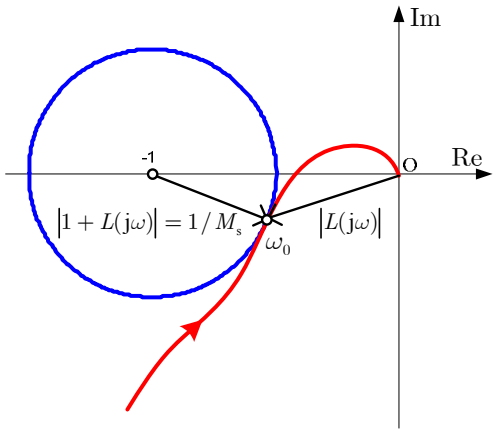

Fig.2. *M_s circle and Nyquist curve $L(j\omega)$ of the optimally tuned closed-loop system. At the frequency ω_0 the sensitivity has its largest value $|S(j\omega_0)|=M_s$.*

According to (5), disturbances d and n in Fig. 1 are attenuated if their frequencies are such that $|S(j\omega)|<1$. At $\omega=\omega_0$ $|S(j\omega_0)|=M_s$, where $M_s>1$.For given value of the tuning parameter M_s in the range $1.4\le M_s\le 2$, Nyquist curve of the loop transfer $L(s)$ of the optimally tuned closed-loop system is presented in Fig.2.

Let us define the function

$$F(\omega,k,k_i)=|1+L(j\omega)|^2-1/M_s^2 \qquad (6)$$

and the performance criterion (2). For β=1 one obtains performance criterion $J_C = k_i$ applied in [6]. Increasing the closed-loop bandwidth ω_B, defined by $|S(j\omega)|<1/\sqrt{2}$ for $\omega<\omega_B$, implies more effective disturbance rejection and faster response. On the other hand, increase of the frequency ω_0 results into the increase of ω_B. Accordingly, the maximization of the combined criterion $J_C=\beta k_i+(1-\beta)\omega$, for $0<\beta\le 1$ guaranteeing $\min_{\beta}(IAE)$, results into improvement of the closed-loop system performance. However, to obtain an adequate tradeoff between performance and robustness, optimal solution must satisfy some robustness constraint. In the present paper, as in [6,7], the robustness constraint is defined by requiring the maximum sensitivity to be equal to the desired value M_s. This is satisfied by requiring that $F(\omega,k,k_i)=0$. In order to avoid the intersection of the Nyquist curve with the M_s circle, as presented in Fig.2, the condition $\partial F(\omega,k,k_i)/\partial\omega=0$ must be satisfied.

According to the previous analysis, the constrained optimization of the PI controller is defined by the following relations

$$\max_{ki,\omega} J_c=\max_{ki,\omega}(\beta k_i+(1-\beta)\omega), \qquad (7)$$

$$F(\omega,k,k_i)=0, \qquad (8)$$

$$\frac{\partial F(\omega,k,k_i)}{\partial\omega}=0. \qquad (9)$$

Calculations are repeated for a few values of the parameter β, from the range $0<\beta\le 1$, in order to find β_0 corresponding to the minimum of *IAE*. Thus, optimal solution is defined by k, k_i, ω_0 and β_0. As for β=1 one obtains the procedure from [6] initial guesses for k, k_i and ω_0 are obtained as defined in [6].

3. SIMULATION RESULTS

Test batch is defined as in [6,11]. Comparison of the proposed method (ŠEMA) with the best PI optimization method, proposed until now by Åström, Panagopoulos and Hägglund (APH) in [6], is presented in Fig.3-14. Improvement of both the performance and robustness is evident. Smaller *IAE* and smaller maximum complementary sensitivity $M_p=\max_{\omega}|L(i\omega)/(1+L(i\omega))|$ are obtained.

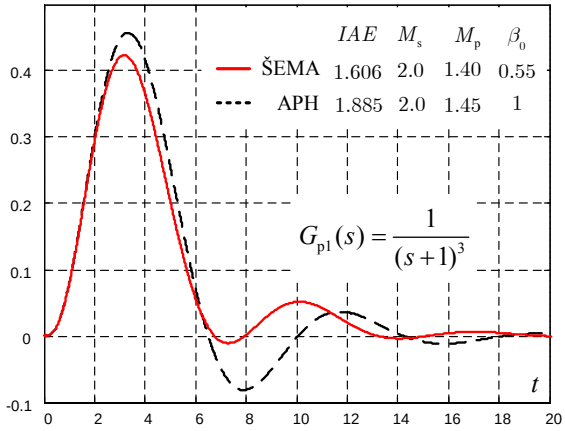

Fig.3. *Load disturbance response for* $G_{p1}(s)$

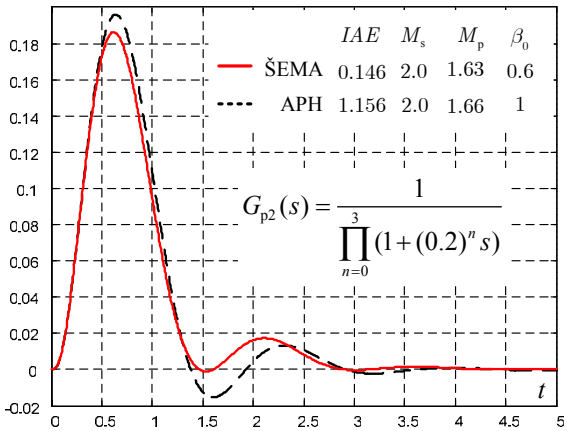

Fig.4. *Load disturbance response for* $G_{p2}(s)$

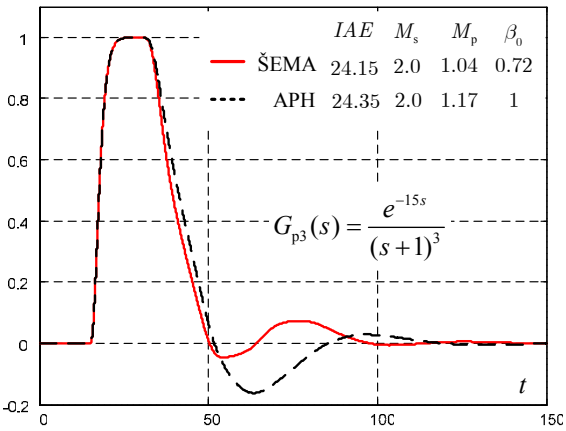

Fig.5. *Load disturbance response for* $G_{p3}(s)$

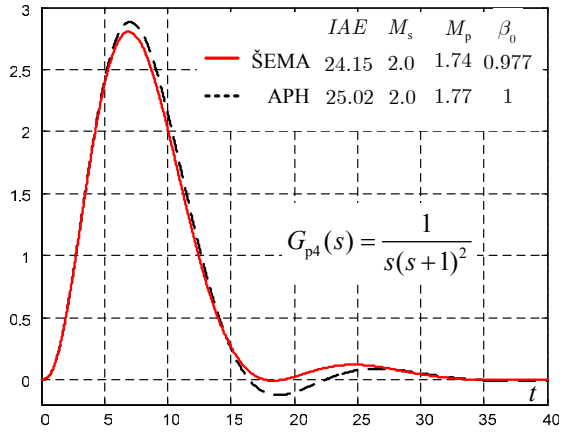

Fig.6. *Load disturbance response for* $G_{p4}(s)$

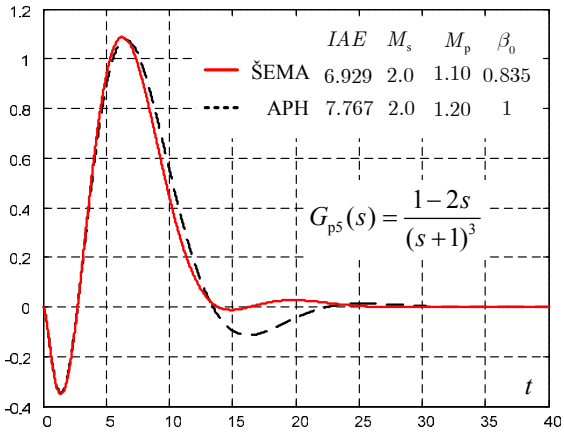

Fig.7. *Load disturbance response for* $G_{p5}(s)$

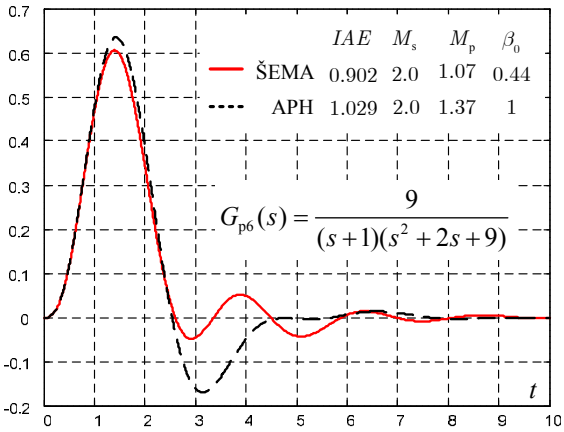

Fig.8. *Load disturbance response for* $G_{p6}(s)$

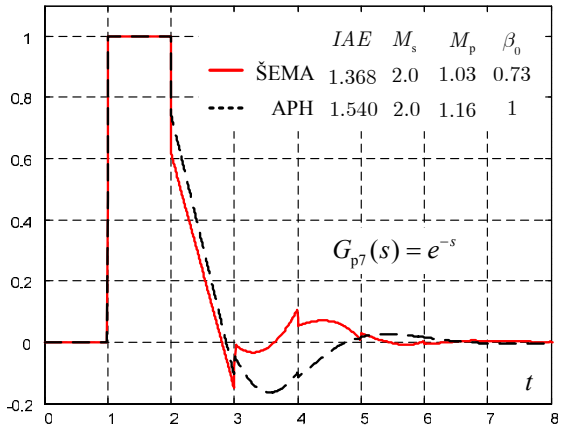

Fig.9. *Load disturbance response for* $G_{p7}(s)$

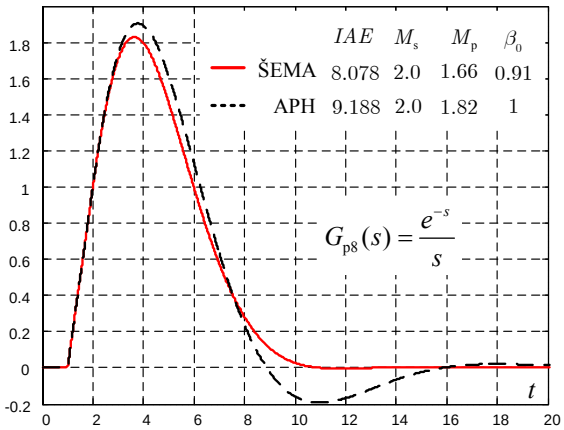

Fig.10. *Load disturbance response for* $G_{p8}(s)$

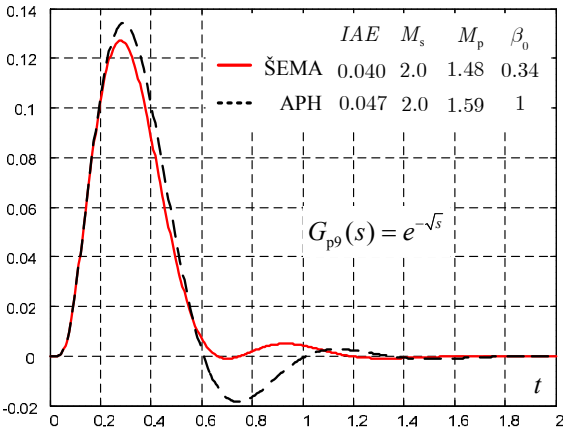

Fig.11. *Load disturbance response for* $G_{p9}(s)$

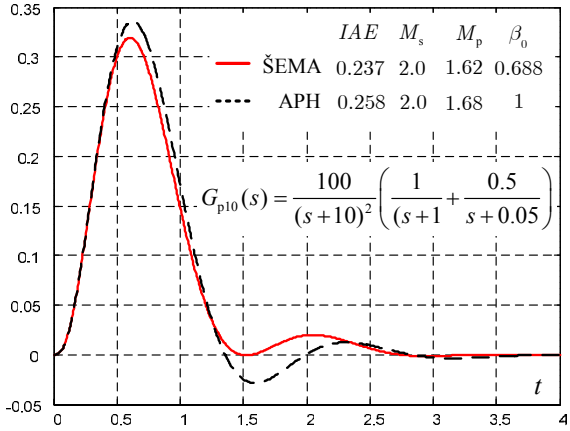

Fig.12. *Load disturbance response for* $G_{p10}(s)$

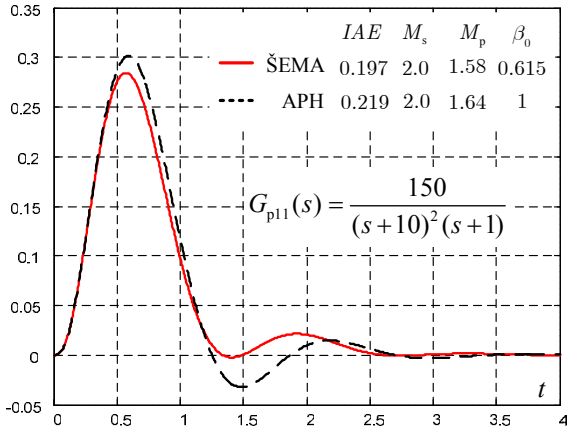

Fig.13. *Load disturbance response for* $G_{p11}(s)$

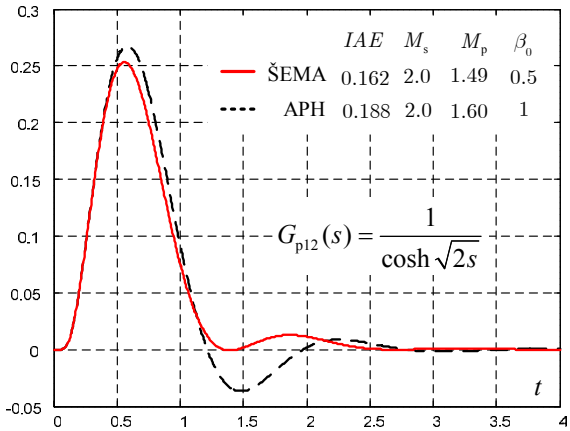

Fig.14. *Load disturbance response for* $G_{p12}(s)$

Table 1. *Parameters of the optimally tuned PI controller obtained by applying the combined criterion* J_c, *for* G_{pn}, n=1,2,..,12.

G_{pn}	M_s	k	$T_i=k/k_i$	ω_0	IAE	M_p	β_0
	1.8	1.330	2.402	0.934	1.813	1.20	0.660
G_{p1}	2.0	1.634	2.579	0.997	1.606	1.40	0.555
	1.8	3.715	0.671	4.368	0.181	1.44	0.770
G_{p2}	2.0	4.650	0.676	4.826	0.146	1.63	0.600
	1.8	0.311	7.582	0.117	24.595	1.00	0.850
G_{p3}	2.0	0.398	9.202	0.129	24.151	1.04	0.720
	1.8	0.292	9.194	0.386	31.530	1.60	0.993
G_{p4}	2.0	0.352	8.490	0.428	24.148	1.74	0.977
	1.8	0.311	1.946	0.458	7.399	1.00	0.920
G_{p5}	2.0	0.389	2.230	0.512	6.929	1.10	0.835
	1.8	0.624	0.510	2.495	0.926	1.07	0.545
G_{p6}	2.0	0.752	0.573	2.580	0.902	1.07	0.440
	1.8	0.297	0.407	2.081	1.387	1.00	0.860
G_{p7}	2.0	0.382	0.497	2.308	1.368	1.03	0.730
	1.8	0.481	4.914	0.820	10.348	1.55	0.932
G_{p8}	2.0	0.546	4.405	0.870	8.078	1.66	0.910
	1.8	5.383	0.249	10.468	0.048	1.33	0.450
G_{p9}	2.0	6.371	0.250	11.247	0.040	1.48	0.340
	1.8	2.280	0.651	4.552	0.296	1.46	0.830
G_{p10}	2.0	2.795	0.645	5.021	0.237	1.62	0.688
	1.8	2.449	0.587	4.885	0.240	1.41	0.754
G_{p11}	2.0	3.004	0.591	5.347	0.197	1.58	0.615
	1.8	2.700	0.515	5.201	0.191	1.34	0.630
G_{p12}	2.0	3.228	0.523	5.641	0.162	1.49	0.500

Finally, in the proposed optimization procedure a noise filter can be easily included in two ways. Firstly, as a time constant T_f defined by the relation [6,7]

$$T_f = 1/(N\omega_0),\ N \in [2,10]. \tag{10}$$

Secondly, by using the maximum sensitivity to measurement noise M_n, given by the relation [6,7]

$$M_n = \max_{\omega} |G_{un}(j\omega)|,\quad G_{un}(s) = -C(s)/(1+L(s)), \tag{11}$$

as an additional constraint for a given value of M_n. In that case the controller $C(s)$ in (3) is given by the relation

$$C(s) = \gamma(sk + k_i)/(s(T_f s + 1)). \tag{12}$$

Optimal parameters are k, k_i, ω_0, β_0 and T_f. Additional constraint (11), for a desired value of M_n, is added to (7)-(9).

4. CONCLUSION

The proposed optimal and robust tuning of the PI controller for $M_s \geq 1.7$ besides smaller IAE and M_p guarantees smaller over shoot and under shoot. For $M_s < 1.7$ practically the same tuning is obtained as for maximizing k_i, i.e. for β=1.

5. REFERENCES

[1] S. Yamamoto and I. Hashimoto, "Present status and future needs: the view from Japanese industry", In Arkun and Ray, Eds., *Chemical Process Control-CPCIV. Proc. 4th Inter. Conf. on Chemical Process Control,* TX, 1991.

[2] L. Desbourough, R. Miller, "Increasing customer value of industrial control performance monitoring—Honeywell's experience", in: *Sixth International Conference on Chemical Process Control, AIChE Symposium* Series Number 326, Vol.. 98, 2002.

[3] K. J. Åström, T. Hägglund, "Revisiting the Ziegler–Nichols step response method for PID control", *Journal of Process Control,* Vol. 14, pp. 635–650, 2004.

[4] M. R. Matausek, G. S. Kvaščev, "A unified step response procedure for autotuning of PI controller and Smith predictor for stable processes", *Journal of Process Control*, Vol. 13, pp. 787-800, 2003.

[5] S. Skogestad, "Simple analytic rules for model reduction and PID controller tuning", *Journal of Process Control*, Vol. 13, pp. 291–309, 2003.

[6] K. J. Åström, H. Panagopoulos and T. Hägglund, "Design of PI controllers based on non-convex optimization", *Automatica*, Vol. 34, pp. 585-601, 1998.

[7] H. Panagopoulos, K. J. Åström and T. Hägglund, "Design of PID controllers based on constrained optimization", *IEE Proc-Control Theory Appl.*, Vol. 149, pp. 32-40, 2002.

[8] B. Kristiansson, B. Lennartson, "Evaluation and simple tuning of PID controllers with high-frequency robustness", *Journal of Process Control* Vol. 16, pp. 91-102, 2006.

[9] A. Karimi, M. Kunze, R. Longchamp, "Robust controller design by linear programming with application to a double-axis positioning system", *Control Engineering Practice,* Vol. 15, pp. 197-208, 2007.

[10] T. B. Šekara, M. R. Mataušek, "A simple effective method to obtain a well-tuned PID controller", Zbornik radova 51 Konf. ETRAN, Vol. 1, 2007.

[11] T.B. Šekara, M.R. Mataušek, "Optimalno podešavanje PI/PID regulatora za procese definisane racionalnom funkcijom prenosa", INFOTEH Vol. 6, Ref. A-2, p. 6-9, Jahorina Mart 2007.

[12] T.B. Šekara, M.R. Mataušek, "Optimization of PID controller based on maximization of the proportional gain under constraints on robustness and sensitivity to measurement noise", to appear in *IEEE Trans. AC* (in December 2008).

[13] F. G. Shinskey, "How good are our controllers in absolute performance and robustness?", *Measurement and Control,* Vol. 23, pp. 114–121, 1990.

[14] T. B. Šekara, *Frakcione transformacije sa primjenom u sistemima automatike i električnim kolima,* Doktorska disertacija, Elektrotehnički fakultet Univerziteta u Beogradu, 2006.

[15] I. Podlubny, "Fractional-Order Systems and $PI^{\lambda}D^{\mu}$ controllers", *IEEE Trans. AC*, Vol. 44, pp. 208-214, 1999.

[16] H. F. Raynaud and A. Zergaïnoh, "State-space representation for6fractional order controllers", *Automatica*, Vol. 36, pp. 1017-1021, 2000.

[17] C. A. Monje, A. J. Calderon, B. M. Vinagre, Y. Q. Chen and V. Feliu, "On Fractional PI^{λ} Controllers: Some Tuning Rules for Robustness to Plant Uncertainties", *Nonlinear Dynamics*, Vol.38,pp. 369-381, 2004.

[18] T. B. Šekara, M. R. Mataušek, "Frakciono dinamičko proporcionalno dejstvo PI/PID regulatora", Zbornik radova L Konf. ETRAN, Vol. 1, pp. 252-255, 2006.

A HIGH PRECISION POSITIONAL SYSTEM BASED ON REFERENCE MODEL AND VARIABLE STRUCTURE CONTROL

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Abstract: *The paper presents the design of a high precision positional system. The system uses the reference model disturbance estimator based on variable structure control with discrete-time sliding mode. The resulting control provides the system robustness to parametric and external disturbances and suppresses non-modeled dynamics excitation. The approximate, but still very good, invariance of the system output to the disturbances is demonstrated using a simulation example.*
Keywords: *Variable structure systems, positional servo-systems, discrete-time sliding mode control, active disturbance estimator.*

1. INTRODUCTION

The prevailing positional systems in industry are based on PID controllers. The great advantage of such systems is their simple design and easy tuning based on the input-output model. However, the system output is sensitive to the parameter changes of controlled system. Also, the step system response shows an overshoot, and their external disturbance rejection is not very good.

An alternative approach is to apply variable structure control (VSC) with sliding modes (SM). This type of control offers an excellent response robust to the large parameter variations in the controlled system. Besides, VSC with SM have an excellent rejection capability of the external disturbances.

Unfortunately, a full system state is needed for VSC. In addition, the controller output is not smooth as it shows step-like changes from one value to the other. Such jumps in the control may excite un-modeled high frequency dynamics. This results in a high frequency parasitic motion that can not be tolerated in electromechanical systems.

This paper presents a discrete-time VSC system with a disturbance estimator, based on the reference model and a supplemental integral action in the controller. An interesting feature of the presented approach is that the disturbance estimator subsystem and the main control subsystem use the same type of SM controller. This is a significant advantage from the application point of the view. The proposed control structure makes positional systems practically invariant, and positional servo systems significantly robust.

The paper is organized as follows. The second section of the paper presents the general mathematical model of the controlled system (plant). The third section describes the disturbance estimator based on the reference model. Tracking SM controller, embedded as the main element of disturbance estimator and position controller, is designed in the fourth section. The illustrative example is given in the fifth section, and the conclusion ends the paper.

2. MATHEMATICAL MODEL OF THE CONTROLLED SYSTEM

The model is given in its canonical controllable form as follows:

$$\begin{aligned}\dot{\mathbf{x}}(t) &= (\mathbf{A}+\Delta\mathbf{A})\mathbf{x}(t)+\mathbf{b}u(t)+\mathbf{p}(t),\\ y(t) &= x_1(t),\end{aligned} \tag{1}$$

where $\mathbf{x}\in\Re^n$ is the state vector, $\mathbf{A},\Delta\mathbf{A}\in\Re^{n\times n}$ are the constant and perturbation part of the system matrix, respectively; $\mathbf{b}\in\Re^n$ is the input vector; $u\in\Re$ is the input, defined further as *control*; $\mathbf{p}\in\Re^n$ is the vector of external disturbances; $y\in\Re$ is the system output or *controlled variable*.

Assumption 2.1.. *The system* (*1*) *is fully controllable and observable.*

Assumption 2.2. *Parametric and external disturbances and their derivatives are piecewise continuous and bounded functions.*

The system model given by (1) may be also represented in the following form.

$$\begin{aligned}\dot{\mathbf{x}}(t) &= \mathbf{A}\mathbf{x}(t)+\mathbf{b}u(t)+\mathbf{d}(t),\\ \mathbf{y}(t) &= x_1(t),\end{aligned} \tag{2}$$

where

$$\mathbf{d}(t)=\Delta\mathbf{A}\mathbf{x}(t)+\mathbf{p}(t)$$

is the *equivalent disturbances vector.*

Remark 2.1: *If the equation* (*1*) *is a linear first-order Taylor approximation of a nonlinear system model, then the equivalent disturbances vector includes also neglected higher derivatives.*

The system model (2) in the complex domain is given as:

$$Y(s)=G_o(s)U(s)+D(s)\,, \tag{3}$$

where

$$G_o(s)=[1\,0\,...0][s\mathbf{I}-\mathbf{A}]^{-1}\mathbf{b};$$

$$D(s)=[1\,0\,...0][s\mathbf{I}-\mathbf{A}]^{-1}\mathbf{d}(s).$$

As it may be seen in (3), the vector of equivalent disturbances is simply added to the system output.

The main control problem of the high precision systems is the suppression of the disturbances. The traditional approach to this problem is to place in the control loop a high gain component just before the entrance point of the external disturbances. The classic PID controllers are mostly used as such a component. But, they reach a high gain only in steady-state, and therefore they are adequate for a restricted class of reference inputs and disturbances only.

Another approach is to estimate the disturbances and apply feed-forward technique to compensate their effect on the output. The design of the adequate disturbance estimators is the topic of numerous papers. In Section 3 the estimator described in [1] and [2] will be shortly presented, since it is used in the proposed design in this paper.

3. REFERENCE MODEL-BASED DISTURBANCE ESTIMATOR

Consider the system shown in the fig. 1. It will be first shown that under some conditions the disturbances D do not influence the output Y.

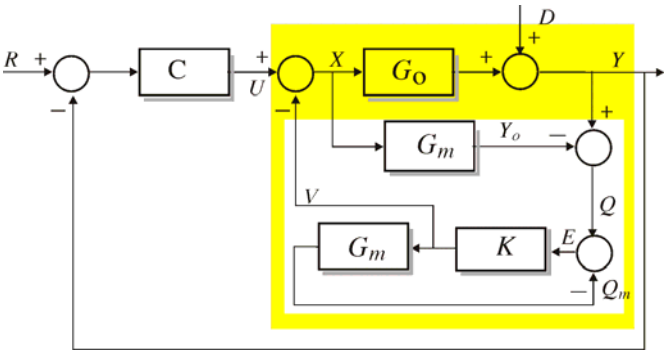

Fig.1. *The disturbance estimator* [2].

Assumption 3.1: *The nominal controlled system G_o is stable. The model of the controlled system G_m has the same transfer function as the nominal controlled system.*

Corollary 3.1. *Based on the Assumption 3.1, Q=D.*

Assumption 3.2: *In the closed loop subsystem consisting of the controller K and the controlled system model G_m, denoted as KG_m, the following equation is valid: E=0.*

Corollary 3.2. *From Assumption 3.1, and 3.2 it follows:*

$Q_m=Q=D$.

It is obvious then that $V = G_m^{-1}Q_m$. From the assumption and corollary 3.2 it follows $V = G_m^{-1}D = G_o^{-1}D$. Therefore:

$$Y = G_o(U - V) + D = G_m(U - G_m^{-1}D) + D = G_oU \qquad (4)$$

Hence the output Y is not affected by the disturbance D.

Remark 3.1: *The estimator given in Fig. 1 may be realized in discrete- or continuous-time (digital or analog).*

The implementation of the Assumption 3.1 is not a problem. However, the realization of the Assumption 3.2 is not possible in general, since it requires a system which could ideally track every possible signal representing any equivalent disturbance vector **d**(t). This vector depends on too many factors such as parameter changes in the controlled system, external disturbances and perhaps even neglected higher derivatives. Hence equivalent disturbance vector may take many mathematical forms.

However, the approximate realization is possible for some classes of signals. If it is possible to realize the subsystem KG_m in Fig. 1 able to track input signals up to r-th order, then the proposed system will compensate the same class of external disturbances. Since the parameter changes are much slower than external disturbance, they can be tracked as well.

In this paper the controlled systems of the second-order will be considered only. This is not a significant loss in generality. It is common in positional systems to neglect small inertial time constant resulting in second-order models, which is adequate for the control design. The following section presents the design of the controller K embedded in the subsystem KG_m given in Fig. 1, which is capable to follow signals up to the 3rd order [3].

4. CONTROL SYSTEM DESIGN

4.1. Control synthesis

In this section a synthesis method of the controller K, Fig.1, which produce control signal $v(t)$ will be considered.

The component G_m in the subsystem KG_m, Fig. 1, is the nominal model of the controlled plant G_o. Its parameters are constant, and its state is fully available. It is not influenced by any external disturbances, thus its output depends only on the control $v(t)$. This control will be synthesized using discrete-time SM approach.

The nominal plant model, G_m,of an electro-mechanical, electro-hydraulic or electro-pneumatic positional system may be identified with transfer function:

$$G_m(s) = \frac{b}{s(s+a)} = \frac{Q_m(s)}{V(s)}. \qquad (5)$$

The state-space model of this system is:

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix} = \begin{bmatrix}0 & 1\\ 0 & -a\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} + \begin{bmatrix}0\\ b\end{bmatrix}v \Rightarrow \dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{b}u, \qquad (6)$$

$q_m = x_1$.

The system error is defined as:

$$e(t) = q(t) - q_m = q(t) - x_1(t). \qquad (7)$$

The model in the error space of the same system is:

$$\dot{\mathbf{e}} = \mathbf{A}\mathbf{e} - \mathbf{b}v + \mathbf{p};\ \mathbf{e} = \begin{bmatrix}e_1\\ e_2\end{bmatrix};\mathbf{p} = \begin{bmatrix}0\\ a\dot{q} + \ddot{q}\end{bmatrix}. \qquad (8)$$

Here vector **p** depends on the reference q in the subsystem KG_m, and plays the role as the *disturbance caused by the reference*. The component $a\dot{q}$ may be relatively easily estimated and compensated by the feed-forward technique. The second component, $\ddot{q}$, cannot be estimated using the second-order differentiator due to high content of the noise. Since the influence of the first component may be dealt with, only the second component will be seen as real disturbance. Therefore the vector **p** will be considered as $\mathbf{p} = [0\ \ \ddot{q}]^{\mathrm{T}}$.

Remark 4.1: *Positional systems have a constant reference, and therefore* **p**=0. *This is not valid for tracking systems.*

If a discrete-time controller with a sampling-time, T, and zero-order hold controls the plant (8), then it is necessary to consider the discrete-time equivalent of the analog system (8):

$$\mathbf{e}(k+1) = \mathbf{A}_d\mathbf{e}(k) - \mathbf{b}_d v(k) + \mathbf{d}_d(k), \qquad (9)$$

where

$$\mathbf{A}_d = \exp(\mathbf{A}T); \mathbf{b}_d = (\int_0^T \mathbf{e}^{\mathbf{A}t}\mathrm{d}t)\mathbf{b};$$

$$\mathbf{d}_d = \int_0^T \mathbf{e}^{\mathbf{A}t}\mathbf{p}(kT + T\text{-}t)\mathrm{d}t.$$

Another discrete-time equivalent model may be obtained if the error derivative is replaced with its Euler approximation:

$$\mathbf{e}(k+1) = \mathbf{e}(k) + T\mathbf{A}_\delta\mathbf{e}(k) - T\mathbf{b}_\delta v(k) + T\mathbf{d}_\delta(k). \qquad (10)$$

The models (9) and (10) are identical if $\mathbf{A}_\delta, \mathbf{b}_\delta$ satisfy the following equations:

$$\mathbf{A}_d = \mathbf{I} + T\mathbf{A}_\delta; \mathbf{b}_d = T\mathbf{b}_\delta; \mathbf{d}_d = T\mathbf{d}_\delta. \qquad (11)$$

In the sequel, the model (10) will be used.

A VSC with SM design is based on the notion of the *switching function*. The switching function, $s(k)$, is linear in state, and it is defined as:

$$s(k) = \mathbf{c}_\delta^T \mathbf{e}(k); \mathbf{c}_\delta^T = [c_{\delta 1} \;\; c_{\delta 2}]. \quad (12)$$

Consider the line in the error space where switching function is zero, named *switching line*:

$$s(k) = c_{\delta 1} e_1(k) + c_{\delta 2} e_2(k) = 0. \quad (13)$$

This line passes through the origin. The control $v(k)$ is then chosen so that two conditions are satisfied. First, the system state, starting from an arbitrary initial point where $s(k) \neq 0$, is driven to the switching line where $s(k) = 0$. This part of the motion is named *reaching mode*. Second, once the state is at the switching line it should stay on it regardless of system disturbances. This part of the motion is named *discrete-time SM*. The choice of the switching function must provide an asymptotically stable motion in the SM. In this way the error vector, $\mathbf{e}(k)$, will always reach origin, and the output will ideally follow the reference. In the considered case, the asymptotic stability is realized by a suitable choice of the slope of the vector $\mathbf{c}_\delta^{\mathrm{T}}$. The resulting dynamics should be defined by an eigenvalue, that is located within the unit circle, which defines the line slope.

To find a suitable control $v(k)$, the above conditions will be expressed in the terms of the switching function dynamics. Suppose that the value of the switching function satisfies the following condition [4]:

$$s(k+1) - s(k) = -\min\{|s(k)|; \sigma T\}\operatorname{sgn}(s(k)); \sigma > 0. \quad (14)$$

Consider first the case $|s(k)| > \sigma T$:

$$s(k+1) - s(k) = -\sigma T \operatorname{sgn}(s(k)). \quad (15)$$

The following condition [5],[6]:

$$|s(k+1) - s(k)|\, s(k) < 0 \quad (16)$$

must be fulfilled for the system to reach (or cross) the switching line.

Multiplying the equation (15) by $s(k)$ and taking into account that $\sigma T > 0$ and $s(k)\operatorname{sgn}(s(k)) = |s(k)| > 0$, it is obvious that (16) is a consequence of (15). Therefore the state will be closer to the switching line and the absolute value of the switching function, $s(k)$, will decrease. In a moment $k=k_o$-1 it will drop bellow σT, i.e. $0 < |s(k_o - 1)| < \sigma T$. Then the dynamics (14) will be equal to

$$s(k+1) - s(k) = -s(k) \Rightarrow s(k+1) = s(k_0) = 0. \quad (17)$$

Thus, in the moment k_o the system state will be on the switching line, and the reaching mode will end. In all the future moments it holds $|s(k > k_o)| = 0 < \sigma T$. The system state stays on the switching line, and the discrete-time SM begins and continues until the state reaches the origin. The control $v(k)$ needs to be defined.

First, the control in the reaching mode, named *reaching control*, will be determined. In the first part of the reaching phase, system motion is defined by (15). If (10) is inserted into (12) and then into (15), the following equation is obtained:

$$\mathbf{c}_\delta^{\mathrm{T}} \mathbf{A}_\delta \mathbf{e}(k) - \mathbf{c}_\delta^{\mathrm{T}} \mathbf{b}_\delta v(k) + \mathbf{c}_\delta^{\mathrm{T}} \mathbf{d}_\delta(k) = -\sigma \operatorname{sgn}(s(k)).$$

To solve this equation for $v(k)$, the term $\mathbf{c}_\delta^{\mathrm{T}} \mathbf{b}_\delta$ must be nonzero. Since the linear transformation of the switching function and the control does not affect the system dynamics [7], it may be taken that $\mathbf{c}_\delta^{\mathrm{T}} \mathbf{b} = 1$. The previous equation is solved for $v(k)$ to get the first component of the reaching control, $v_{r1}(k)$:

$$v(k) = v_{r1}(k) = \sigma \operatorname{sgn}(s(k)) + \mathbf{c}_\delta^{\mathrm{T}} \mathbf{A}_\delta \mathbf{e}(k) + \mathbf{c}_\delta^{\mathrm{T}} \mathbf{d}_\delta(k). \quad (18)$$

After that, the control, which brings the state onto the $s(k)$=0, must be determined. In this case, system motion satisfies (17). By the same procedure, (10) is put into (12), and then into (17). The obtained equation is then solved for $v(k)$ to get second reaching control component $v_{r2}(k)$:

$$v(k) = v_{r2}(k) = T^{-1} s(k) + \mathbf{c}_\delta^{\mathrm{T}} \mathbf{A}_\delta \mathbf{e}(k) + \mathbf{c}_\delta^{\mathrm{T}} \mathbf{d}_\delta(k). \quad (19)$$

Taking into account that in the SM the switching function is zero, the discrete-time equivalent control $v_{eq}(k)$ is computed from (19) as

$$v_{eq}(k) = \mathbf{c}_\delta^{\mathrm{T}} \mathbf{A}_\delta \mathbf{e}(k) + \mathbf{c}_\delta^{\mathrm{T}} \mathbf{d}_\delta(k). \quad (20)$$

Observe that the reaching control component (19) and the discrete-time equivalent control (20) can be defined by the same expression (19). This is a particular property of the discrete-time SM, and it does not apply to the continuous-time SM.

The above reaching control (19) and discrete equivalent control (20) require the knowledge of disturbance $\mathbf{d}_\delta(k)$ for their realization. If the disturbance term is dropped in (19), the general expression for the second reaching control component as well as the equivalent control will be

$$v_{eq}(k) = T^{-1} s(k) + \mathbf{c}_\delta^{\mathrm{T}} \mathbf{A}_\delta \mathbf{e}(k). \quad (21)$$

Thus, the obtained VSC will be given as:

$$v(k) = \begin{cases} \sigma \operatorname{sgn}(s(k)) + \mathbf{c}_\delta^{\mathrm{T}} \mathbf{A}_\delta \mathbf{e}(k), & |s(k)| > \sigma, \\ T^{-1} s(k) + \mathbf{c}_\delta^{\mathrm{T}} \mathbf{A}_\delta \mathbf{e}(k), & |s(k)| \leq \sigma. \end{cases} \quad (22)$$

It is also convenient from practical reasons to introduce the saturation function in the expression for the control, in order to obtain the so called *saturation control* $u_{sat}(k)$, which is given by the expression [8]:

$$v_{sat}(k) = sat(v_{eq}(k)) = \begin{cases} \sigma \dfrac{v_{eq}(k)}{|v_{eq}(k)|}, & |v_{eq}(k)| > \sigma, \\ v_{eq}(k), & |v_{eq}(k)| \leq \sigma. \end{cases} \quad (23)$$

Remark 4.2: *The last term in (20) is* $Tc_2 \ddot{d}(k)$. *This term is zero for all step and ramp disturbances. For other types of disturbances its magnitude will decrease with the sampling- time, T, i.e.* $\lim_{T \to 0} \mathbf{d}_\delta(k) \to 0$.

4.2. The enhancement of the control with an supplemental integral action

The steady-state error in a closed-loop system may be annihilated or reduced if the integral action is present in the controller. In the case of the VSC SM control, the integral action, $u_I(k)$, is in use only when the error is small, that is in the final stage of the sliding mode, when the error, $\mathbf{e}(k)$, becomes sufficiently small. Integral action is not necessary in

the first part of the reaching mode, as well as when the state is far from the origin, because it may provokes an unwelcome overshoot.

This idea is implemented by the next expression:

$$u_I(k)=\begin{cases} 0 & \|\mathbf{e}(k)\|>\rho>0; \\ hs(k)+u_I(k-1) \text{ if } & \|\mathbf{e}(k)\|\le\rho. \end{cases} \quad (24)$$

where ρ is an arbitrary small positive constant, and $\|e(k)\|$ is a suitably chosen norm. Then the general expression for the control, $v(k)$, which is valid both in the reaching and the sliding mode may be written as:

$$v(k)=\begin{cases} v_{r1}(k), & |s(k)|>\sigma T, \\ v_{eq}(k), & |s(k)|\le\sigma T, \\ v_{eq}(k)+u_I(k), & |s(k)|<\sigma T \text{ and } \|\mathbf{e}(k)\|<\rho. \end{cases} \quad (25)$$

Remark 4.3 *Note that the supplemental integral action does not suppress the disturbances that are dependent on the reference signal, since it is placed in the control loop in rear of the disturbance input. Nevertheless, if the closed loop is stable, it upgrades the system type for one, and increase the possibility to better track the reference.*

Remark 4.4. *If the main controller, C, is designed as the considered controller K, constant disturbances, acting on the controlled plant input, as depicted on Fig. 2, are fully suppressed by* $u_I(k)$*, since the integral action is placed in front of their input to the system.*

In the next paragraphs the system stability and the steady-state error for typical reference signals and disturbances will be analyzed.

4.3. The stability analysis

The control defined by (22) was proposed and discussed in [4]. The stability of the closed-loop system with bounded but not estimated/compensated disturbances was established. Starting from this point, it has to be proven that the inclusion of the integral action in the last phase of the sliding motion does not jeopardize the system stability.

Analyzing first the switching function dynamics, it will be shown that, if the integral gain *h,* satisfies the condition $0\le h<1/T$, then its difference equation defines a stable system.

To prove this, left-multiply first (10) by $\mathbf{c}_\delta^{\mathrm{T}}$, and put in it the value of the discrete-time control given by:

$$v(k)=v_{eq}(k)+u_I(k)=T^{-1}s(k)+\mathbf{c}_\delta^{\mathrm{T}}\mathbf{A}_\delta\mathbf{e}(k)+u_I(k)$$

thus one obtains the switching function difference equation:

$$s(k+1)=-Tu_I(k)+T\mathbf{c}_\delta^{\mathrm{T}}\mathbf{d}_\delta(k),$$
$$u_I(k)-u_I(k-1)=hs(k).$$

Applying *Z*-transformation to the previous relations, and solving them with respect to *s*(*z*), one obtains:

$$s(z)=\frac{z-1}{z[z-(1-hT)]}T\mathbf{c}_\delta^{\mathrm{T}}\mathbf{d}_\delta. \quad (26)$$

It is obvious that $0\le h<T^{-1}$ guarantees that poles are inside of the unit circle, and therefore the system is stable.

4.4. The steady state error

Consider the closed-loop linear system structure given in Fig.2. It represents the proposed control system in linear mode.

From Fig.2 one obtains the open loop transfer function:

$$W(z)=\frac{Q_m(z)}{E(z)}=\left\{\left[(c_{\delta1}+\frac{z-1}{zT}c_{\delta2})\right](\frac{zh}{z-1}+\frac{1}{T})+p_1\frac{z-1}{Tz}\right\}\times$$
$$\times\frac{z-1}{z}\frac{b}{a}\left[\frac{Tz}{(z-1)^2}-\frac{z(1-e^{-aT})}{a(z-1)(z-e^{-aT})}\right]. \quad (27)$$

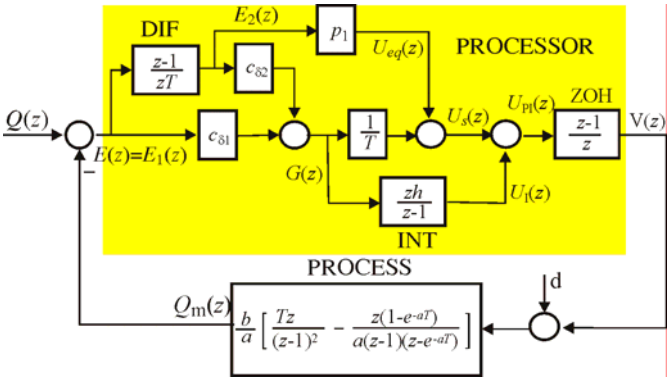

Fig.2. *The closed-loop system structure,* $p_1=\mathbf{c}_\delta^{\mathrm{T}}\mathbf{A}_\delta$.

Let the reference signal be

$$q(t)=\frac{q_0}{r!}t^r,$$

where q_0 is a positive constant. Step reference is for *r*=0, ramp for *r*=1 and parabola for *r*=2. The steady-state error can be obtained from conventional definition of error constants: K_p, K_v and K_a, defined as:

$$K_e=\begin{cases} K_p & \text{for } r=0 \\ K_v & \text{for } r=1 \\ K_a & \text{for } r=2 \end{cases}=\lim_{z\to1}(z-1)^rW(z). \quad (28)$$

The position and velocity constants for the open-loop transfer function (27) are $K_p=K_v=\infty$. Therefore the step and ramp inputs will be tracked with a zero steady-state error. If there is no compensation of the reference-dependent disturbance term, the value of the acceleration constant K_a is equal to:

$$K_a=bTc_{\delta1}\frac{h}{a}. \quad (29)$$

The steady state error for the input parabola $q(t)=0{,}5q_0t^2$ is equal to

$$e_1(\infty)=\frac{q_0T}{bc_{\delta1}}\frac{a}{h}. \quad (30)$$

Remark 4.3: *If the disturbance term* $a\dot{q}$ *is feed-forward compensated, then just one term,* $\ddot{q}$ *remains in the disturbance caused by reference. The parabolic signal will be completely suppressed by the additional integrator since its second derivative is a constant. The cubic parabola signal will have a steady state error equal to*

$$e_1(\infty) = \frac{q_0 T}{b c_{\delta 1}}. \quad (31)$$

It is easy to show that constant disturbance acting on the controlled system input will be completely suppressed due to the integral action. A unit ramp disturbance will result in steady state error equal to

$$e_1(\infty) = \frac{d_0 T}{K_A h c_{\delta_1}}. \quad (32)$$

where d_0 is the slope of the disturbance, and K_A is the gain of power amplifier which supplies controlled positional system.

4.5. Controller parameters determination

The first controller parameter to be determined is the sampling time, T. According to the above steady-state accuracy analysis, this parameter should be as small as possible. The choice of the sampling time will be influenced by controlled system parameters b and a, and also the desired open- and closed-loop dynamics.

Once the sampling time is determined, parameters of the switching function, $c_{\delta 1}$ and $c_{\delta 2}$, defining the system performance in the SM should be set. This is a crucial step since the rise-time in the reaching mode is relatively brief compared to one in the SM.

Taking into account that $\mathbf{c}_\delta^{\mathrm{T}} \mathbf{b}_\delta = 1$, the only parameter to be determined for a second-order controlled system is the switching line slope $(c_{\delta 1} / c_{\delta 2}) = \alpha$, as seen in the following equation:

$$[c_{\delta 1} \;\; c_{\delta 2}]\mathbf{b} = 1 \Rightarrow c_{\delta 2} = [b_{\delta 2} + (c_{\delta 1} / c_{\delta 2}) b_{\delta 1}]^{-1}. \quad (33)$$

The switching function parameter calculation for higher-order systems is discussed in [1], [3], [4], [6], and [9]. The following example implements this procedure to a real system.

5. DESIGN EXAMPLE

The considered positional system is driven by a permanent magnet dc motor. The armature is supplied by a power module based on pulse-width modulation. The angular position is measured by an incremental encoder. The considered controlled plant contains a series connection of the amplifier, the power module, motor and encoder. Its second-order model (5) parameters are a=26,5 s^{-1} and b=654 rad/Vs.

The sampling time is set to T=0,4 ms. The matrices defining discrete-time equivalent system are:

$$\mathbf{A}_\delta = \begin{bmatrix} 1 & 0.98687 \\ 0 & -26.152 \end{bmatrix}; \mathbf{b}_\delta = \begin{bmatrix} -0.32413 \\ -645.41 \end{bmatrix}.$$

The switching line slope is chosen as $\alpha = 50$. Further design steps are given bellow:

$$c_{\delta 2} = (-645.41 - 50 \cdot 0.32413)^{-1} = -0.00151449,$$

$$c_{\delta 1} = 50 c_{\delta 2} = -0.07557248,$$

$$\mathbf{c}_\delta^{\mathrm{T}} \mathbf{A}_\delta = [0 \quad -0.035572].$$

The discrete-time equivalent control is

$$u_{eq}(k) = 2500\, s(k) - 0.035572\, e_2(k).$$

The value of σ is set to 10.

The second component of the error vector, $e_2(k)$, representing the error derivative in the sampling instants, is approximated using the Euler's formula:

$$e_2(k) = T^{-1}[e_1(k) - e_1(k-1)].$$

The system model is then augmented by the feed-forward compensation of the disturbance term $a\dot{q}$. The final version of the model is given as

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 0 & -a \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ b \end{bmatrix} u + \begin{bmatrix} 0 \\ a \end{bmatrix} \dot{q} \Rightarrow \dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{b}u,$$

$$q_m = x_1.$$

The supplemental integral action (23) is defined by h=1000, ρ=0,01 and $\|\mathbf{e}(k)\| = |e_2(k)|$.

Fig.3 shows the response of the KG_m control subsystem to the reference:

$$q(t) = 5\cos(t) - 2\cos(2{,}5t). \quad (34)$$

The maximal absolute value of the tracking error, excluding the starting moment, is $4 \cdot 10^{-7}$. As it may be seen from Fig.3, the subsystem having the task to generate signal $v(t)$ that compensates the disturbance (see Fig.1), tracks its input signals with a high precision, and thus fully satisfies design requirements.

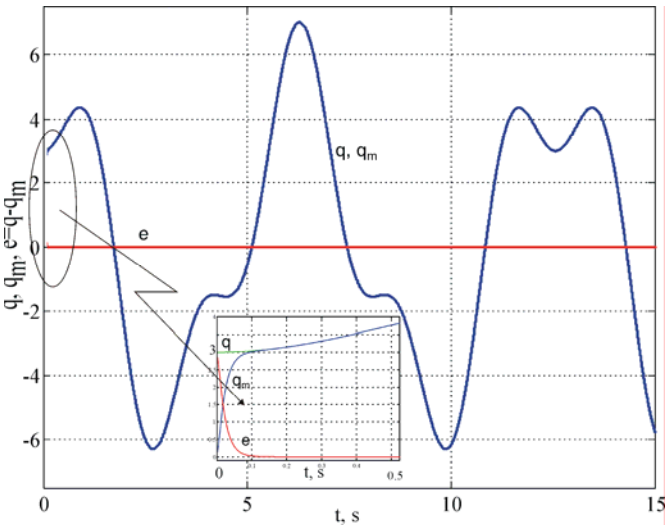

Fig.3. *The response of the KG_m subsystem to reference q, (34), with integral action parameter h=1000.*

The next step is to design the main positioning controller which generates the control $u(t)$. This controller is depicted as block C in the Fig. 1. One possibility is to apply a P, PD or PID controller. In the proposed positional system, this controller is basically the same as controller K. The main difference is that the derivative of the output, $\dot{y}(kT)$, is used, instead of the derivative of the error signal, in order to prevent the output overshoots. It is assumed that $\dot{y}(kT)$ may be either measured or estimated by a suitable observer.

Fig.4 shows the output of the overall system with a step reference of 0.001 rad. The pulse disturbance, acting at the plant input, was set as

$$\mathbf{p}(t) = [0 \quad -100\,[h(t\text{-}0{,}4)\text{-}h(t\text{-}0{,}7)]]^{\mathrm{T}}.$$

The integral action with h=1000 was permanently on in the controller K. As seen in the Fig.4, the introduction of the estimator in the control system results in almost total

rejection of the pulse disturbance, even if there is no integral action in the main controller C. Yet, this action is still needed to suppress the uncompensated portion of disturbances, which cannot be dealt by the disturbance estimator. Indeed, according to trace 3 in Fig.4, the given disturbance estimator overcompensates disturbance. The used integral action in the main controller avoids this overcompensation (trace 4 in Fig.4).

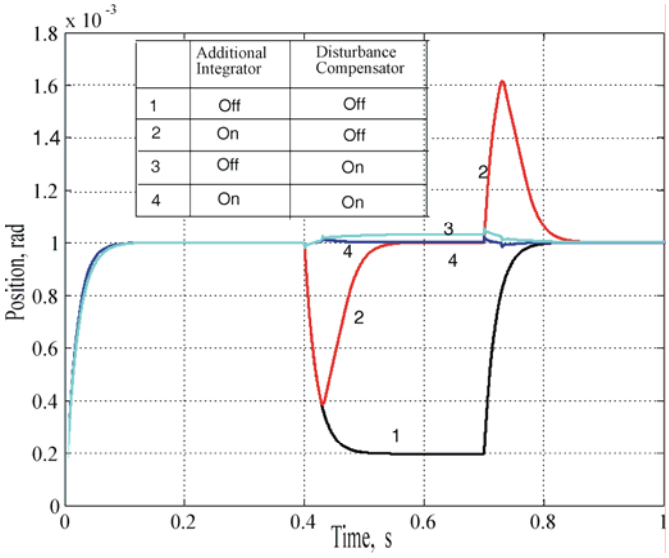

Fig.4. *Step response of the proposed positional system for different conditions. Integral gain h: in the main controller (C) h=100: in the controller K within the disturbance estimator h=1000.*

The presented positional system design has been experimentally tested using two real systems. In the first test the positional system described in the design example was used, and the results are published in [3]. In the second test the positional system was driven by a three-phase vector controlled induction motor with a squirrel-cage rotor. The results were presented in [10]. The positioning precision in both cases was maximal possible; that is one encoder quantum.

7. CONCLUSION

This paper introduces a new approach to the design of high-precision positional robust systems using discrete sliding mode motion. The positional system robustness is significantly enhanced by two particular features: use of a disturbance estimator based on discrete sliding mode motion, and inclusion of an additional integral action effectuated in the final stage of the motion. Due to these features a positioning system of the type three can be made using relatively cheap and simple components. That cannot be done using conventional approach in the design. The simulation of the response to a pulse disturbance confirmed the theoretical prediction.

8. REFERENCES

[1] B. Veselić, "*Application of discrete-time sliding mode control in robust servo-systems synthesis for coordinated tracking of complex trajectories*", (in Serbian) Doctoral dissertation, Faculty of Electronic Engineering, University of Niš, 2005.

[2] B. Veselić, Č. Milosavljević, B. Peruničić-Draženović, D. Mitić, "Digitally controlled sliding mode based servo-system with active disturbance estimator," in *Proc. of 9th IEEE Int. Workshop on Variable Structure Systems*, Alghero, Italy, June 5-7, 2006, pp. 51-56. CD.

[3] Č. Milosavljević, B. Peruničić-Draženović, B. Veselić, D. Mitić, "A new design of servomechanisms with digital sliding mode", *Electrical Engineering*, **89** (2007), 233-244.

[4] G. Golo, Č. Milosavljević: "Robust discrete-time chattering-free sliding mode control", *Systems and Control Letters*, 2000, **41**, pp.19-28.

[5] Č. Milosavljević: "General conditions for the existence of a quasi-sliding mode on the switching hyperplane in discrete variable structure systems," *Automatic Remote Control*, vol. 46, pp. 307-314, 1985.

[6] Č. Milosavljević: "Discrete-ime VSS", Chapter V in *Variable Structure Systems: from Principles to Implementation,* ed. by A. Sabanovic, L. M. Fridman and S. Spurgeon, The IEE Press, 2004., ISBN 0 86341 350 1.

[7] V. I. Utkin: *Sliding modes in control and optimization,* Springer-Verlag, 1982.

[8] G. Bartolini, A. Ferrara, V. I. Utkin: "Adaptive sliding mode control in discrete-time systems", *Automatica,* 1995, **31**(5), 769-773.

[9] Č. Milosavljević, B. Peruničić-Draženović, B. Veselić,, D. Mitić: "Sampled-data quasi-sliding mode control strategies", *IEEE International Conference on Industrial Electronics ICIT* 2006, Bobay, Indija. CD.

[10] Č. Milosavljević, Veselić, B.: "Digital sliding mode based induction motor shaft position controller synthesis", *XIV Int. Symposium on Power Electronics Ee2007*, Novi Sad, 7-9 Nov. 2007, CD.

PARAMETAR ESTIMATION OF DYNAMICS SYSTEMS USING MATLAB SPE TOOLBOX

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Abstract: *This paper defines a methodology of parameter estimation in a complex dynamics system. All phases of estimation are realized in MATLAB/SIMULINK. SIMULINK RTWT (Real-Time Windows Target) with multifunctional PCI I/O card is used in data acquisition during experiments, while the other steps of acquisition are performed in SIMULINK-y i SPE (SIMULINK PARAMETR ESTIMATION) toolbox.*

Keywords: *parameter estimation, MATLAB/SPE, I/O data acquisition card, apparatus for motor control of human arm in ballistic tasks*

1. INTRODUCTION

Dynamics systems identification is to determine the models of dynamics system based on experimental data measured at input/output of the object. Each real dynamics system (control plant) can be, in general, adjoined to various types of models that describe its operating under different operating conditions. Dynamic models of the objects are realized based on the laws of physics to bring a valid insight into model's behavior that can be used in simulations when designing a control system. Models obtained in such a matter can generally be very complex thus not suited for a practical implementation. Therefore we strive towards simpler models based on a set of parameters to sustain pertinent dynamic link between inputs and outputs of control plant. Nonetheless, we can ask what the minimum set of parameters that a model needs to contain is, as well as the influence of each individual parameter on dynamic behavior of real object. Answers to these questions are the main reason for uses of different methodologies for dynamic systems models direct identification based on experimental data. Dynamic systems identification and estimation of parameters as experimental procedure can be divided, in general, into four phases: (1) data activation at identification object input/output following appropriate experimental protocols, (2) evaluation or choice of model structure, (3) model parameters estimate, (4) model validation and verification (of the suggested structure and parameters). Complete identification and estimation procedure implies implementation of the above mentioned phases. What identification methods will be used in individual phases is determined by the type of model we wish to acquire (parameter model, non-parameter model, continuous or discrete model etc.) as well as executing conditions of the experiment (noise, identification in open/closed loop etc.). It is important to mention that validation phase is mandatory step that reveals how the suggested model and estimated model parameters present dynamic behavior of the controlled plant. There is no universal algorithm of estimation of model parameters or the experimental protocol that would always pass the validation phase. It is often necessary to fine tune the parameter estimation algorithm, model complexity or the experimental protocol that would in result give a valid model, and therefore identification of dynamic systems (objects) can be observed as iterative process (Fig.1).

Above mentioned parameter estimation procedure that is described in this paper is fully conducted in MATLAB/SIMULINK environment. Dynamic system whose parameters are subjected to estimation is an apparatus for motor control of the human arm in ballistics tasks of target hitting exercise (Fig.2).

2. BASIC PHASES OF DYNAMIC SYSTEMS PARAMETER ESTIMATES IN MATLAB ENVIRONMENT

MATLAB/SIMULINK environment embodies all the necessary dynamic system parameter estimation tools to handle experimental data. For the first phase of data acquiring and generating of appropriate stimulus signals RTWT (RT Windows – Target) environment can be used together with multifunctional I/O cards.

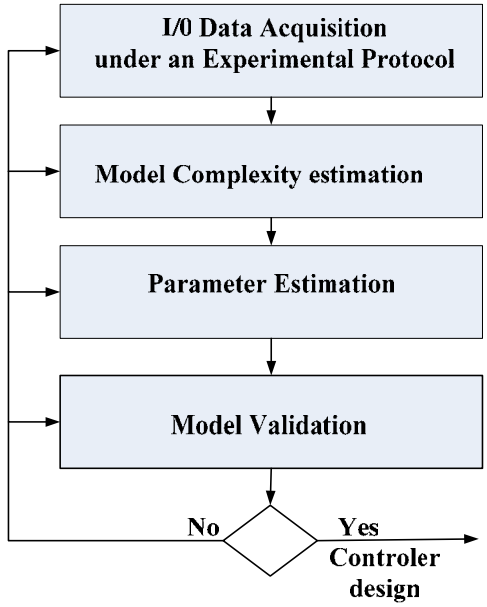

Fig.1. *Iterative dynamic systems identification process and parameters estimation*

HUMUSOFT PCI multifunctional I/O card MF624 was used for conducting experimental parameter estimation. The same I7O card was at the same time used for generating test signals and acquisition of input/output data from the apparatus. Acquisition data is easily imported into MATLAB workspace through Scope blocks and it is additionally archived at PC for additional processing. Second estimation phase and choice of model structure is realized directly in the SIT (System Identification Toolbox), supported by SIMULINK. Third and fourth model parameters and validation estimation phase is performed in the SPE toolbox. It was possible to acquire all the relevant indicators of quality of the performed apparatus parameters estimate (target function, experimental and simulated value, estimation parameters sensitivity etc.) from SPE toolbox.

3. MODEL OF APARATUS FOR MOTOR CONTROL OF HUMAN ARM IN BALLISTIC TASKS OF TARGET HITTING

Apparatus consists of DC motor with permanent magnet on whose axis is a catapult for throwing small balls as shown in Fig.2.

Mathematical model of the apparatus can be described with the following equation:

$$J\ddot{\theta} + m_{KAT} cg_{KAT} g \sin\theta + f(\dot{\theta}) = \tau_{EM}, \quad (1)$$

where **J** is total moment of system inertia around the rotation axis; $\mathbf{m_{KAT}}$ is catapult mass; $\mathbf{cg_{KAT}}$ is catapult center of gravity;

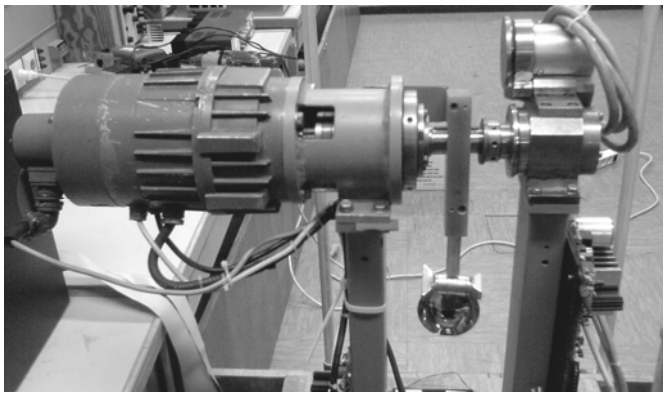

Fig.2. *Apparatus for motor control of human arm in ballistic tasks of target hitting exercise*

Total moment of system inertia J consists of two components: $J=J_O+J_{KAT}$, where J_O is motor rotor moment of inertia, J_{KAT}- is catapult moment of inertia over the rotation axis. Motor rotor moment of inertia J_O is available from catalogue. As the catapult consists of many components made of different materials and with different geometry, it is not simple to determine its parameters. For that reason the catapult moment J_{KAT} and its position of center of gravity cg_{KAT} were the estimation subject. It is possible to model all the components that the catapult is made of by CAD software application and n that manner estimate values of the moment of inertia and center of gravity of al the components individually and therefore entire catapult as a complex model. Instead of modeling in CAD software it is also possible to make a geometrical simplification of the catapult components and in that manner observe the catapult as a pendulum with $_{mKAT}$ mass and cg_{KAT} center of gravity and then do the parameter estimation of the above mentioned parameters.

In general, the problem is also the friction modeling and determination of non-linear friction function f(ω).

Many models that would describe the friction phenomenon were suggested and they are mostly based on experimental results [7]. They give relationship of the friction moment, τ_F, as the function of speed, ω, i.e. $\tau_F = f(\omega)$. The classical "static + kinematic + viscose" friction model is most commonly used and it consists of three components:

- Constant Coulomb friction τ_C that depends solely on the sign of speed ω,
- Viscose component B_T that is proportional to the catapult axis rotation speed ω and
- Static component τ_C that represents moment that is necessary to generate in order to initiate activation of catapult axis.

Model can be described by the following equation:

$$\tau_F = T_s \eta(\dot{\theta}) + T_c \operatorname{sgn}(\dot{\theta}) + B_T \dot{\theta},$$

$$\eta(\dot{\theta}) = \begin{cases} 0 & \dot{\theta} = 0 \\ 1 & \dot{\theta} \neq 0 \end{cases}, \qquad T_c = \begin{cases} 0 & \dot{\theta} = 0 \\ T_c^+ & \dot{\theta} > 0 \\ T_c^- & \dot{\theta} < 0 \end{cases} \quad (2)$$

Which components of the equation (2) will be used in the model description depends on the concrete dynamic system as well as the frequency range of interest in which the model parameters are being estimated. So, with low drive frequencies, in other words low speeds, it is possible to leave out the viscose component of friction. In this case satisfactory results were obtained by model described by Coulomb friction τ_C.

3.1 Apparatus modeling in SimMechanics Environment

Unlike the classic SIMULINK blocks that represent appropriate mathematical operations, SimMechanics is GUI environment for physical modeling of mechanical systems, machines, their kinematics and dynamics using classic Newton laws of mechanics. Physical components of mechanical systems such as solid bodies, joints, kinematical limitations etc. are represented with corresponding blocks. Through sensors and actuators that are integral part of Simmechanics toolbox models from SimMechanics can be connected to other MATLAB/SIMULINK components. This toolbox was used for apparatus modeling and block diagram is shown on Fig.3.

4. PARAMETER ESTIMATION IN SIMULINK PARAMETER ESTIMATION SPE TOOLBOX

SPE toolbox is GUI (graphic user interface) for estimation and calibration of model parameters based on experimental data taken from real object. SPE supports the following estimation types:

- Transient Estimation — model parameters estimation based on comparison of model outputs with experimental data under given input signal.
- Initial Condition Estimation — estimation of initial conditions based on experimental data.
- Adaptive Lookup Tables — Estimation of values in tables for points determined in advance according to test values from physical model.

Regardless of the estimation type, entire estimation process is performed in Control and Estimation Tools Manager. Basic steps of the estimation process are:

1. Input/output entry of data acquired in the experimental phase
2. Data pre-processing
3. Choice of parameters and initial conditions for estimation
4. Configuration of estimation process

5. Parameters estimation
6. Graphic presentation of relevant indicators of estimation quality
7. Validation of estimated parameters

4.1. Apparatus parameters estimation procedure

MATLAB RTWTGT environment with PCI I/O multifunctional card MF624 was used to conduct experimental procedure of data acquisition from the apparatus. Block diagram of RTWTGT environment is shown in Fig.4. Different kinds of sinus test signals were generated through signal generator and they were used to stimulate DC motor through square amplifiers [4]. Encoder (1000 imp/o) mounted at motor axis simultaneously provided information about position of motor axis through encoding input of I/O card. In order to estimate all the parameters of the motor described by the equation (1) it is necessary to know speed and acceleration as well as the position. Speed and acceleration estimator was used to that purpose (real differentiator) and on its output were acquired all the necessary measurements.

After conducting experimental protocol the following phase in the estimation procedure is starting SPE toolbox and entry of acquired data or sets of acquired data. SPE toolbox has an option of data pre-processing before the onset of the estimation procedure that is performed through the following activities: removal of peaks, glitches from signal, detrending -removal of arithmetic mean or linear growth, filtering data with desired filter etc.

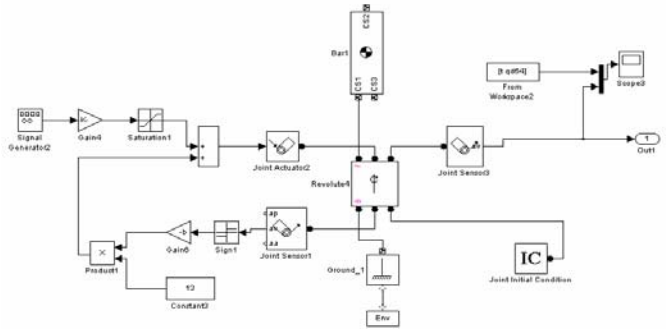

Fig.3. *Apparatus model in SimMechanics toolbox*

After pre-processing there follows a choice of parameters/initial conditions, configuration and execution of estimation process. All the above mentioned phases are performed in Control and Estimation Tools Manager which is shown in Fig.5.

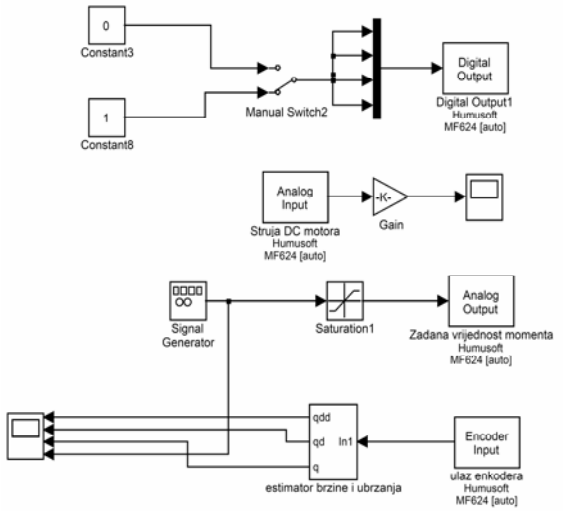

Fig.4. *RTWTGT environment for data acquisition from the apparatus*

Table 1. *Estimated apparatus parameters*

Parameter	Estimated valus of parameters - before	Estimated values of parameters - after
Catapult mass	0.35kg	0.467kg
Catapult length	0.18m	0.18m
Friction coefficient	0.01Nm	0.014Nm
Position of center of gravity	0,09m	0.1066m
Kt of DC motor	0.167A/Nm	0.167A/Nm
Moment of inertia with regard to individual axis	0.0017kgm2	0.0017kgm2
	9.45e-004 kgm2	9.45e-004 kgm2
	0.0017 kgm2	0.0027 kgm2

Values of apparatus parameters before and after the estimation procedure are provided in Table 1.

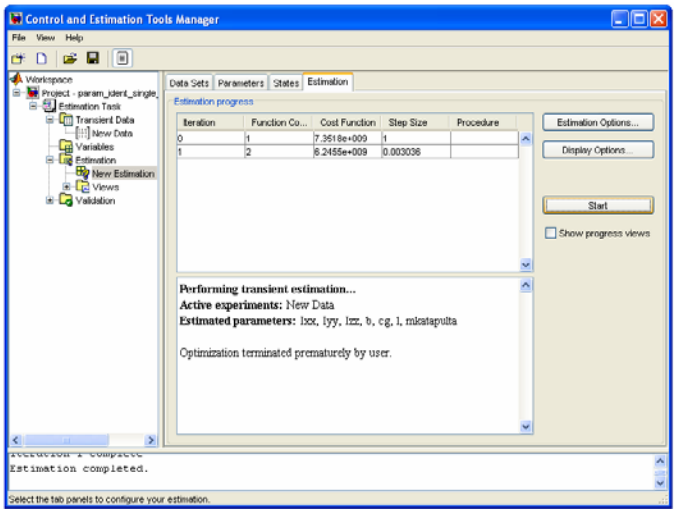

Fig.5. *Control and Estimation Tools Manager*

After the conducted estimation procedure follows the overview of relevant estimation quality indicators which are:

- Measured and simulated value
- Goal function as sum of squares of error that was subject to minimizing in the estimation procedure
- Estimation parameters sensitivity
- Parameters trajectory
- Residuals

All the above mentioned indicators of quality of estimation process are shown in Fig.6, 7, 8 and 9.

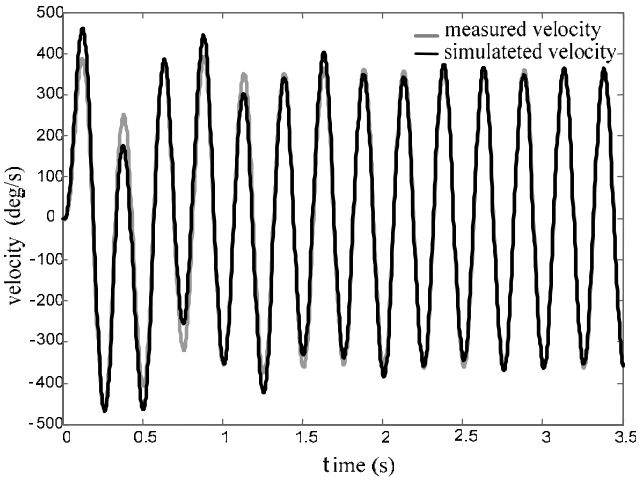

Fig.6. *Measured and simulated apparatus speed*

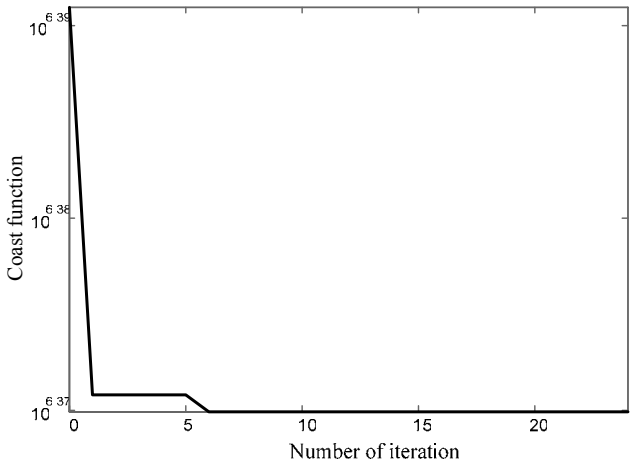

Fig.7. *Convergence of goal function*

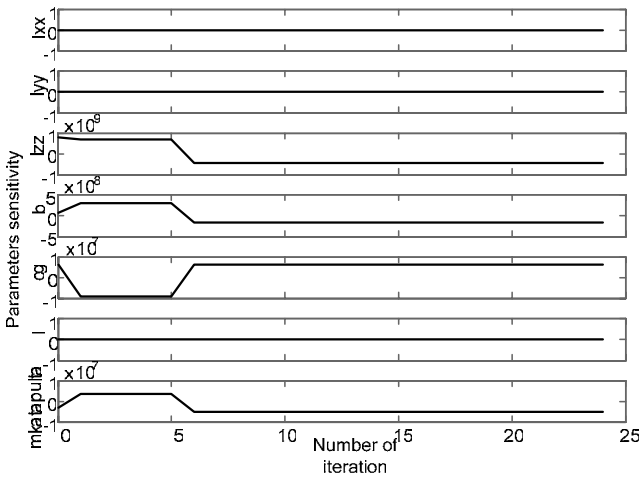

Fig.8. *Estimation parameters sensitivity*

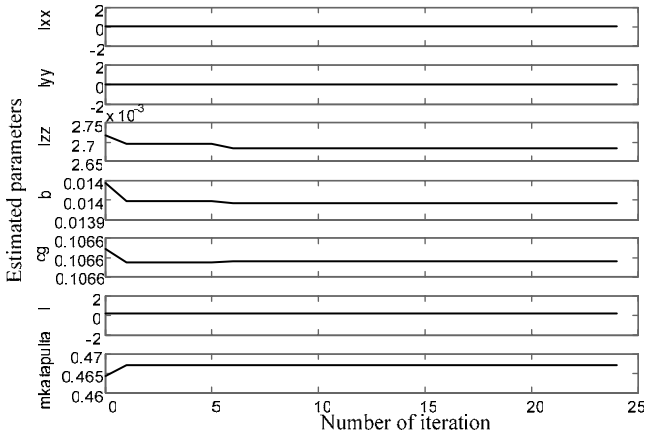

Fig.10. *Values of estimated parameters*

5. CONCLUSION

We gave an practical example of parameter estimation procedure for a mechatronic setup. All results point out the quality of performed estimation. Convergence speed of goal function (sum of error squares) certainly depends on complexity and precision of proposed model of dynamic system. In this specific case, parameters estimation process is completed in less than ten iterations. On the basis of the conducted procedures of parameter estimation followed by estimation of apparatus for motor control of human arm in ballistic tasks of target practice we stand at the pint that the MATLAB/SIMULINK have all the necessary tools for fast, simple and reliable estimation procedure. RTWINTGT toolbox has special benefit here because it provides flexible environment in experimental phase of data acquisition from the aspect of versatility of generated test signals and data archives. Also, identification of dynamic systems and estimation of their parameters is just an initial phase in projecting control structures in general. All further design steps can be performed in MATLAB/SIMULINK (Model Based Predictive Control Toolbox, Control toolbox) form a comprehensive environment, that can handle both, the identification and the estimation processes.

6. REFERENCES

[1] Ioan D. Landau and Gianluca Zito, "Digital Control Systems, Design, Identification and Implementation", Springer-Verlag London Limited 2006

[2] Adnan Salihbegović, "Metode identifikacije procesa", ETF Sarajevo 2004

[3] F. van der Heijden, R.P.W. Duin, D. de Ridder, "Classification, Parameter Estimation and State Estimation An Engineering Approach using MATLAB"

[4] Slobodan Lubura, Milomir Šoja: "Četverokvadrantni pojačavač snage za upravljanje DC motorima", ETRAN, Beograd 2006.godine,

[5] MATLAB SImmechanics toolbox User Gude R2006a

[6] MATLAB Parametar Estimation toolbox User Guide R2006a

[7] H. Olsson, K.J. Åström, C. Canudas de Wit, M. Gäfvert, P. Lischinsky, *Friction Models and Friction Compensation*, Department of Automatic Control, Lund Institute of Technology, Lund University, 1997.

INFLUENCE OF MEASUREMENTS FROM THE DEPTH OF THE DISTRIBUTION NETWORK ON STATE ESTIMATION

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Abstract: *Distribution State Estimation is the essential function of the DMS Analytical Functions System. It is based on both historical data describing loads and real-time telemetered state data. Real-time data consist of switchgear statuses data, tap position of under load tap-changing transformers and telemetered currents and voltages magnitudes. In distribution networks automated in the usual way, only supply substations are covered by SCADA systems. Thus, the redundancy of data necessary for state estimation performance is significantly bad, regarding transmission networks. The quality of distribution state estimation (and consequently of all other analytical functions) could be significantly increased if state data from the depth of the medium voltage network (RTU located at medium voltage substations, reclosers, ...) are taken into account in the state estimation algorithm. The analysis of the impact of these data on the distribution state estimation is the main goal of this paper. It is done for Distribution Utility Elektrovojvodina, "Elektrodistribucija Sombor", Serbia. In this analysis, the results provided with following data are specially stressed: 1) only historical data, 2) historical data and real-time data telemetered from supply substations and 3) historical data, real-time data telemetered from supply substations and data telemetered from the depth of the medium voltage network.*

1. INTRODUCTION

Distribution State Estimation (DSE) represents the essential analytical function for management and planning of distribution network (DN) operation. The evaluation of actual or chosen state of DN is based on off-line data (historical data) and real-time data. Historical data consist of quality and quantity load indicators. Real-time data consist of data about switchgear statuses, tap changer positions, and measurements that are telemetered and stored in the technical database by using SCADA system. Usually, SCADA system covers only supply substations and a few medium voltage (MV) points. Therefore, the redundancy of telemetered real-time data in DN is significantly less than 1,0 (values are approximately 0,2 – 0,3 [2]). Because of that, in the last ten years specialized algorithms for distribution state estimation [2, 3, and 4] have been developed. However, small numbers of papers [5] offer the results of the application of the real-life state estimators. One of the main reasons for that is the fact that the practical application of state estimation in DN requires its integration with the functions for analysis, management, and DN planning: Load Forecast, Load Flow, etc. In fact, it requires its integration in DMS Software (DMS – Distribution Management System). The practical application of DMS Software started with the project realization [1], and verification and analysis of the State Estimation function in *"Elektrodistribucija Sombor"* [6]. At the beginning, only usually available values of real time are used – data about supply substations that are monitored by using SCADA system. The results of such application of DSE function are shown in [7,8,9]. Generally, the results of the state estimation proved to be useful for the estimation of values between the observable parts of DN, but not within them. The verification and analysis of DSE function, that is based not only on data that are telemetered from supply substations by using SCADA system, but on data from the depth of the MV network as well, are shown in this paper. After the introduction, the second part shows mathematical model for distribution state estimation. In the third part, the results of the application of DSE function in *"Elektrodistribucija Sombor"* and the influence of measurements from the depth of the MV network on their quality are shown. After conclusion, bibliography used in this paper is given.

2. METHODOLOGY OF STATE ESTIMATION

The DSE algorithm consists of state estimation of DN on the basis of real-time telemetered data [data about state (measurements) and topology (switchgear statuses)], quantity and quality historical data about DN load. In addition, measurements could be: magnitudes of currents and voltages, active and reactive power on any location in the network. Historical data consist of: (*i*) normalized daily chronological diagram (NDCD) of load for magnitudes of current, active and reactive power and daily chronological diagram of power factor and (*ii*) weight factor – maximal values of load (kW, kVAR, A), load flow (kWh, kVARh) and rated powers of equipment (kVA). If NDCDs of load (currents or powers) are multiplied with appropriate maximal values of load, daily chronological diagrams (DCDs) of currents or powers are obtained in appropriate units.

The developed DSE algorithm consists of 7 steps: 1 – *Preestimation*, 2 – *Verification of topology*, 3 – *Verification of telemetered measurements*, 4 – *Load calibration*, 5 – *Load flow calculation,* 6 – *Verification of telemetered voltage measurements* and 7 – *Load flow calculation*.

2.1. Preestimation

The preestimation consists of load flow calculation of the considered DN [10], for specified root voltage, based only on load historical data. The values calculated in this step are called *preestimated values.* If the network is not remotely monitored, this step is the last step of the estimation algorithm.

2.2. Verification of topology

The verification of topology represents the identification and elimination of errors made during the update on the changes in switchgear statuses made by using SCADA system and manually in the field. Since the redundancy of telemetered data in DN is very humble, the possibilities of topology verification are also very humble. However, heuristic rules can be used, e.g.: in DN where state estimation is always performed (e.g. in every 10 seconds), every sudden change in telemetered magnitudes of measurements and their great difference compared to "good" historical data represents the change of network topology or the error of telemetered measurements.

2.3. Verification of Measurements

The verification of measurements means acknowledging, correction of errors or elimination of "bad" telemetered measurements. Also, due to small redundancy of data, it is based on the artificially obtained redundancy of data obtained on the basis of the results of preestimation. The verification of measurements consists of 5 sub-steps.

2.3.1. Measurements preparation. It represents the conversion of all measurements of various types (powers, currents, power factors) into unique measurements: 1 – currents and power factors or 2 – active and reactive powers.

2.3.2. Elimination of obviously bad measurements. The term *obviously bad measurements* represents the measurements that are: 1 – beyond limits imposed by limitations of relay protection functioning; 2 – zero, but there are loads below them and 3 – over differences between measured and preestimated values of measurements defined in advance. These measurements are rejected from the following algorithm steps.

2.3.3. Network reduction. By making equivalents of all unobserved parts (DN areas), the dimensions of the network are being reduced. The areas consist of electrically connected elements (lines, transformers...) without telemetered measurements of currents and powers. They are mutually connected solely through branches with telemetered measurements. Thus, the unobservable areas are not known in detail, but their total load is. In this way, after the application of very simple procedure of establishing equivalence, mainly unobservable network with N nodes (Figure 1a) is reduced to equivalent network with N_0 nodes that can be entirely observed (areas are highlighted with dashed line).

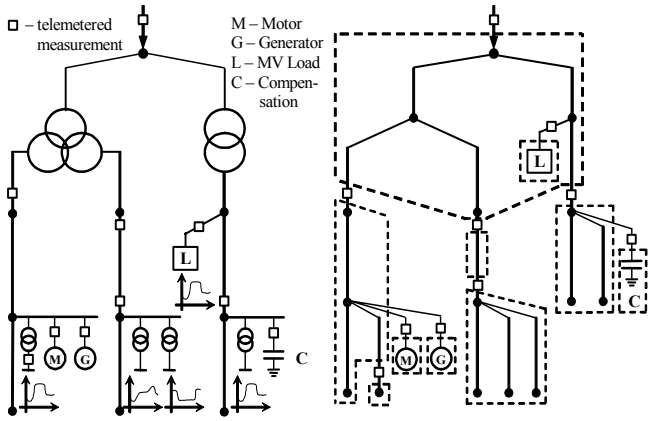

Fig.1. *Network (a) divided in unobservable areas (b)*

2.3.4. Verification procedure. The constrained optimization procedure for measurement verification, applied to reduced model of the network is radically faster than its application to the model of the entire network. This procedure consists of minimization of the following objective function: sum of square of deviations from measured (m) and preestimated (p) from estimated values (e) for N_m telemetered measurements x_j and N_o total loads of the area x_n:

$$\Phi = \sum_{j=1}^{N_m} [w_j^m (x_j^m - x_j^e)^2 + w_j^p (x_j^p - x_j^e)^2] W_j + \sum_{n=1}^{N_o} [w_n^p (x_n^p - x_n^e)^2] W_n \,, \tag{1}$$

with a constraint for every area.

$$f_n = x_n^e + \Delta x_n^p - \sum_{j=1}^{N_m} k_{nj} x_j^e = 0 \,, \qquad n=1, ..., N_o \,. \tag{2}$$

The relative weights of telemetered and preestimated values are marked with w; the relative weights of state of variables and areas are marked with W; k_{nj} represents the sign mark of measured values x_j (it is positive when measured value is directed in the area); x_n represents total active and reactive losses of the area, when (1) active and reactive power are unknown variables x_j or the real and imaginary part of total shunt current, when currents are unknown variables.

Load flows are the essential constraints of the considered optimization procedure. They are implicitly included in the procedures in the preestimation step and also in the fifth and seventh step (load flow calculation).

The result of the optimization procedure consists of *estimated measurements* and *total loads of areas*. The quality of those values is considered in the following sub-step.

2.3.5. Detection of bad data and elimination. The measurement with maximal deviations from the estimated value previously obtained, that surpasses the threshold specified in advance, represents bad measurements and is eliminated from the further procedure of the estimation. After eliminating bad measurements, substeps 2.3.3 and 2.3.4 are repeated, as long as there are bad measurements in sub-step 2.3.5.

2.4. Load calibration

All the loads (active and reactive power or magnitudes of currents with power factor) directly (remotely) monitored are estimated in the previous step. Other belongs to the monitored areas. The load estimation of the node i, in the area n from N nodes is:

$$x_{ni}^e = \frac{x_n^e}{x_n^p} x_i^p \,, \qquad i=1, ... N_n \,, \qquad n=1, ... N_o \,. \tag{3}$$

2.5. Load flow calculation

Finally, state estimation of the original network is obtained on the basis of load flow calculations, for the loads estimated in the previous step and for specific voltage phasors of the roots of DN.

3. INFLUENCE OF MEASUREMENTS FROM THE DEPTH OF THE NETWORK

The verification and analysis of the application of DSE is done in the part of DN *"Elektrodistribucija Sombor"* which is supplied with electric power through supply transformer 110/20 kV/kV (transformer 1) with rated power 31,5 MVA, in supply substation "Sombor 2". The transformer 1 supplies the network of the total length of 130 km, with 127 distribution substations 20/0,4 kV/kV of total rated power 40,29 MVA. The consumption of the considered network (part of the area of the city of Sombor and villages Bezdan, Kolut, Bački Monoštor, Bački Breg, and Kupusina) amounts to 8,975 MW. The considered network is described in [7] and shown in figure 2. Three feeders with the schedule of control measurements are pointed out to. The measurements with the values monitored by using SCADA system for supply substation 110/20 kV/kV are highlighted with yellow; measurements from the depth of the network controlled by using SCADA system for distribution substations 20/0,4 kV/kV are highlighted with green, and control measurements with grey rectangle.

The analysis of the influence of measurements of currents from the depth of the network on the quality of the results of state estimation is done for the period of 64 days. The verification is done on the basis of automatically written results of the DSE function (that used to be permanently done for every change: measurement values, switchgear statuses, tap changer positions, and so on) and simultaneously, the registered values of measurements in chosen control points (20 kV and 0,4 kV values of measurements of magnitudes of currents and voltage in distribution substations 20/0,4 kV/kV). The paper shows the results when state estimation is done in the following five variants:

1. Only by using historical data.
2. By using historical data and the values of telemetered 20 kV currents from supply substation ″Sombor 2″.
3. By using historical data and the values of telemetered 20 kV currents from supply substation ″Sombor 2″ and the values of chosen measurement of 20 kV current on feeder "Pariska" from distribution substation "Kosovska".
4. By using historical data and the values of telemetered 20 kV currents from supply substation ″Sombor 2″ and the values of chosen measurement of 20 kV current from distribution substations "V. Nazor", "Kosovska" and "Elektrovojvodina".
5. By using historical data and the values of telemetered 20 kV currents from supply substation ″Sombor 2″ and the values of chosen measurement of 0,4 kV current of loads supplied from distribution substations ″V. Nazor″, ″Kosovska″ and ″Blok 273″.

The results shown in table 1 are in accordance with the formulated variants of state estimation. Thus, grey fields in the columns Variant/error [%] mark the values used when calculating state estimation and white fields represent measurements used as the control of the result of state estimation.

The quantification of the results quality of state estimation is based on the comparison of the estimated and simultaneously measured values of magnitudes of currents. For that purposes, the following values are used as quantitative indicators: the average absolute and medium percentage deviation of measured and preestimated values (α=P), or measured and estimated values of magnitudes of currents (α=E) (these indicators in the sequel are marked with B and D, respectively), for m moments of measurements:

$$\Delta X_{sr}^{M\alpha} = \frac{1}{m}\sum_{j=1}^{m}\left|X_j^M - X_j^\alpha\right|, \quad \Delta X_{sr\,\%}^{M\alpha} = \frac{100}{m}\sum_{j=1}^{m}\frac{\left|X_j^M - X_j^\alpha\right|}{X_j^\alpha} \quad (4)$$

In the sequel the results of five variants of the application of state estimation for Friday 18.03.2005, working day, are given in detail. In figures (3, 4 and 5) measured values are marked with blue dotted line, DCD of preestimated value with red dotted line (variant 1) and variants of estimated values with full line (variant 2 red, 3 green, 4 black and 5 blue color). Regarding the quality, in all the examples the ratio of weight factors of measured and historical data are the same: T_{meas}:T_{hist} = 100:5.

The review of the quality of state estimation results done for considered variants is given in table 1. The evaluation based only on historical data, variant 1, has the greatest deviation from the measured value; taking into account only control measurements, this deviations averagely amounts to 16,1%. If measurements monitored by using SCADA system are used, the average deviation of estimated from measured values is 13,8%. If the values obtained by using SCADA system are associated with measurements of 20 kV currents, the average deviation of estimated from measured values can be additionally reduced. Even though the increase in number of measurements from the depth of the MV network increases the correctness of the results, it should be pointed out that the choice of measurements locations in the depth of the MV network is of the crucial importance. By adding only one measurement in the depth of the MV network with solidly chosen location, variant 3, the error of the state estimation is reduced in comparison with variant 2 for 1,2% (from 13,8 to 12,6%), and by adding three measurements in the depth of the MV network, variant 4, for 1,7% (from 13,8 to 12,1%). If in DN with 127 distribution transformers for state estimation, except for measurements monitored by using SCADA system, the measurements of 0,4 kV currents of three distribution transformers are used: the quality of the estimated state on those transformers will significantly improve, but this does not apply to the quality of the estimation of the entire area. For the considered example, variant 5, the average deviation from the measured value is 13,5%, which is for 0,3% better than the deviation in the variant containing only SCADA measurements.

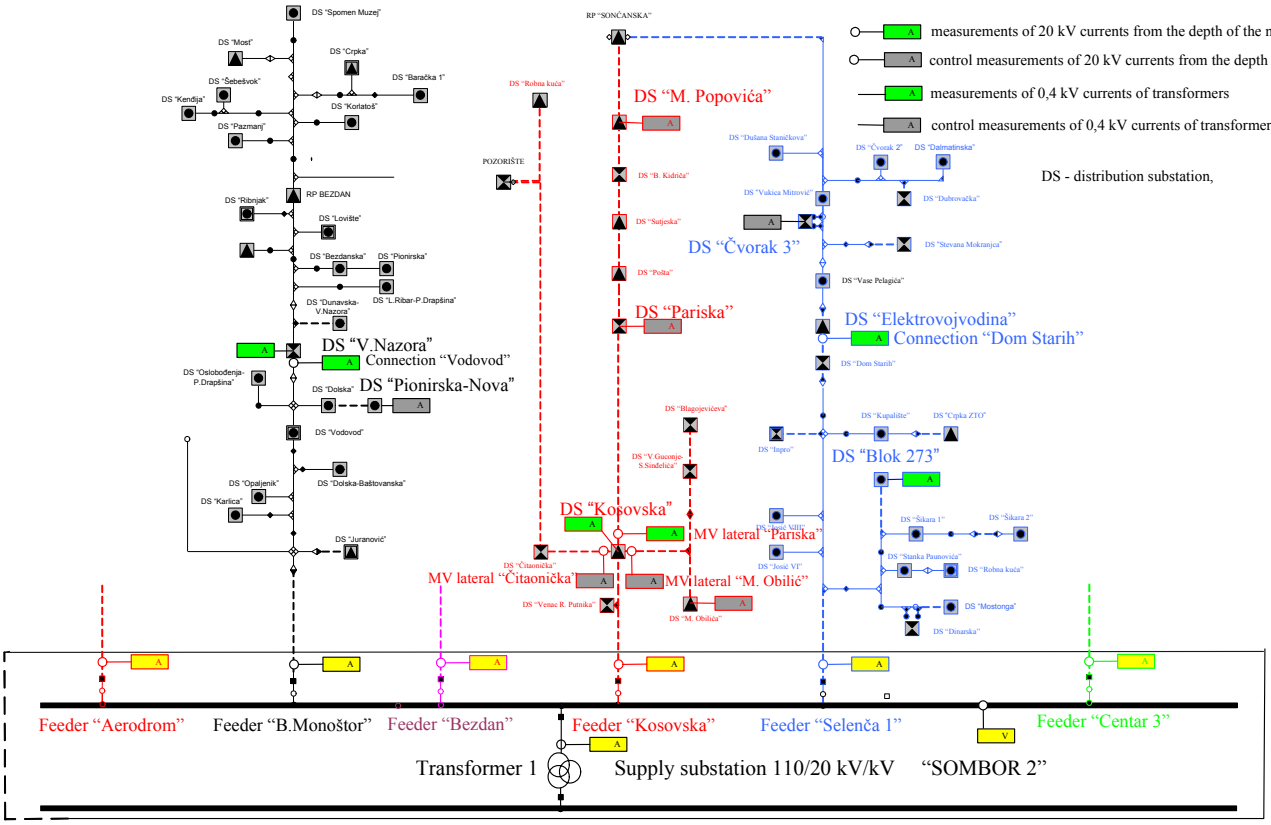

Fig.2. *Schedule of measured equipment in winter period of the experiment*

Table 1. *Quantification of variants of state estimation*

Measurement	Name of power object		Measured current		Variant/error [%]				
			Voltage	Measurement point	1/*B*	2/*C*	3/*C*	4/*C*	5/*C*
SCADA	supply substation 110/20 kV/kV "Sombor 2"	Transformer 1	20 kV	Feeder root	8,3	1,9	1,9	1,9	1,9
		Feeder "Aerodrom"	20 kV	Feeder root	15,1	2,3	2,2	2,2	2,3
		Feeder "B. Monoštor"	20 kV	Feeder root	15,1	2,1	2,1	2,1	2,1
		Feeder "Bezdan"	20 kV	Feeder root	8,3	1,7	1,6	1,6	1,7
		Feeder "Kosovska"	20 kV	Feeder root	12,5	1,4	1,5	1,5	1,4
		Feeder "Centar III"	20 kV	Feeder root	13,2	2,4	2,4	2,4	2,4
		Feeder "Selenča 1"	20 kV	Feeder root	10,4	1,5	1,5	1,5	1,5
		Average of SCADA measurements :			11,9	1,9	1,9	1,9	1,9
Measurements in the depth of the MV network	Feeder B. Monoštor	DS "V. Nazora"	20 kV	Connection "Vodovod"	14,8	12,7	11,5	2,3	11,9
			0,4 kV	Transformer	10,6	10,7	13,1	10,6	0,8
	Feeder Kosovska	DS "Kosovska"	20 kV	MV lateral "Pariska"	30,9	12,5	5,0	5,7	12,0
			0,4 kV	Transformer	10,2	14,3	20,7	21,1	3,7
	Feeder Selenča 1	DS "Elektrovojvod."	20 kV	Connection "Dom Starih"	16,1	9,9	9,7	1,9	9,1
		DS "Blok 273"	0,4 kV	Transformer	24,6	14,4	14,4	12,0	5,1
Control measurements in the depth of the MV network	Feeder B. Monoštor	DS "Pionir. – Nova"	0,4 kV	Transformer	13,2	9,9	10,1	15,2	13,0
	Feeder Kosovska	DS "Kosovska"	20 kV	MV lateral "M. Obilića"	18,0	7,6	11,7	9,9	8,0
		DS "Kosovska"	20 kV	MV lateral "Čitaonička"	12,5	15,9	9,3	10,9	14,0
		DS "Pariska"	0,4 kV	Transformer	32,5	23,5	13,2	13,1	24,2
		DS "M. Popovića"	0,4 kV	Transformer	14,7	14,1	22,4	15,6	12,3
		DS "M. Obilića"	0,4 kV	Transformer	14,2	9,6	7,2	7,2	9,0
	Feeder Selenča 1	DS "Čvorak 3"	0,4 kV	Transformer	7,3	14,0	14,0	21,4	13,9
		Average of control measurements :			16,1	13,8	12,6	12,1	13,6

Fig.3, 4, and 5 present preestimated, measured and estimated values, depending on the variant of application of measurements from the depth of the network. The values shown in figure 3 refer to 20kV current on the feeder "Kosovska". The influence of measurements from the depth of the network on the quality of estimation of 20kV current at the beginning on feeder (values monitored by using SCADA system) is insignificantly small. The values shown in figure 4 refer to 20kV current on MV lateral "Čitaonica" in distribution substation "Kosovska". There are also "worse" historical data on that feeder (preestimated values

in comparison with measured values), but 20 kV measurements from the depth of the network reduce the errors of estimation. The values shown in Fig.5 refer to 0,4 kV current of transformer in distribution substation "M. Obilić" where estimated values are close to measured values and measurements from the depth of the network reduce the estimation errors.

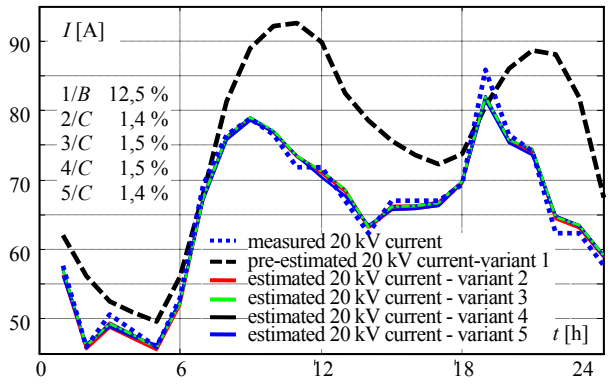

Fig.3. *Estimated 20 kV currents on feeder "Kosovska"*

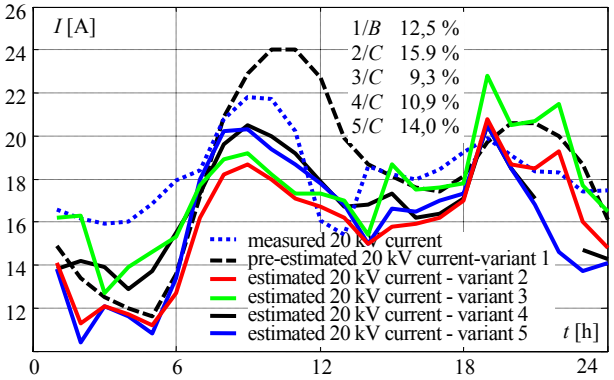

Fig.4. *Estimated 20 kV currents on MV lateral "Čitaonička"*

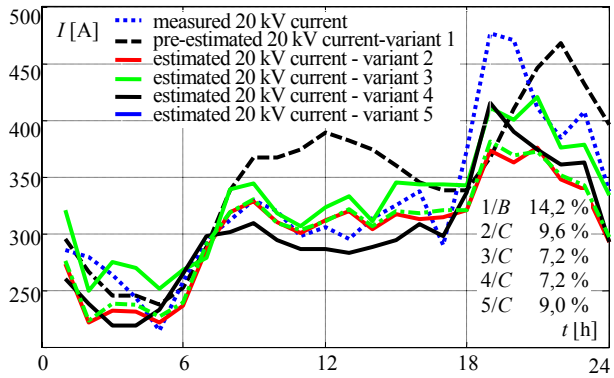

Fig.5. *Estimated 0,4 kV currents of distribution substation "M. Obilić"*

5. CONCLUSION

Distribution state estimation is the basic and most important analytical function for DN calculation. It is used for estimation and analysis of past, current or future states of DN. This paper briefly describes the idea of a simple, fast and robust state estimator. Its power is reflected in the fact that it can be adapted to any DN – from those for which only historical data are available to those that are entirely remotely controlled. The main aspect of this paper is the confirmation of the need to introduce measurements from the depth of the network in the state estimation procedure. Only one small, but representative part of the results obtained by comparison of the values of very complex measurements and application of state estimation in real time, done in the last couple of years is represented here. The paper points out to the main conclusions: 1 – the importance of historical and telemetered data; 2 – the quality of the results of the state estimation increases with the increase in number of consumers supplied by element whose magnitude is being estimated; 3 – measurements from the MV network increase the quality of state estimation. It will not influence the estimation of magnitudes monitored by using SCADA systems, but they will significantly influence their distribution along the points monitored by SCADA systems; 4 – measurements from the depth of the network should be set along feeder so that its location divides the feeder in areas with the same values of their loads, for the great consumers whose value and dynamics of load cannot be predicted at the places where there is the possibility of remote change of switchgear statuses. Finally, the paper shows that the real-time state estimation gains more quality by introducing measurements from the depth of the network, so that it is more reliable and more precise for the analysis of DN state in on-line mode, and, therefore, for its management in real time.

5. REFERENCES

[1] V.Strezoski, D.Popović, D.Bekut, G.Švenda, Z.Gorečan; *DMS Power Applications for Control and Operation Planning,* Project for J.P. Elektrovojvodina, Faculty for Technical Sciences, Novi Sad, 1995-2005.

[2] M.K.Celik, W.-H.E.Liu: *A Practical Distribution State Calculation Algorithm*, Proceedings of IEEE Winter Meeting '99", pp. 442-447, 1999.

[3] A.K.Ghosh, D.L.Lubkeman, R.H.Jones: *Load Modeling for Distribution Circuit State Estimation*; IEEE Trans. on PWRD, Vol.12, No.2, pp. 999-1005, April 1997.

[4] I.Roytelman, S.M.Shahidehpour: *State Estimation for Electric Power Distribution Systems in Quasi Real-Time Conditions*, IEEE Trans. on PWRD, Vol.8, No.4, pp. 2009-2015, October 1993.

[5] D.L.Lubkeman, J.Zhang, A.K.Ghosh, R.H.Jones: *Field Results for a Distribution Circuit State Estimator Implementation*; IEEE Trans. on PWRD, Vol.15, No.1, pp. 399-406, January 2000.

[6] Z.J.Simendić: *Real-Time State Estimation of Distribution Networks*, master thesis (in Serbian). Faculty for Technical Sciences, Novi Sad, 2006.

[7] Z.J.Simendić, V.C.Strezoski, G.S.Švenda: *In-Field Verification of the Real-Time Distribution State Estimation*, 18-th International Conference on electricity Distribution, Turin, Session No.3, 6-9 June 2005.

[8] Z.J.SimendIć, G.S.Švenda, V.C.Strezoski, V.Mijatović: *Verification of the Distribution State Estimation in "Elektrodistribucija Sombor"* (in Serbian), JUKO CIRED, Zlatibor, Serbia & Montenegro, 17-20. Oktober 2006.

[9] Z.J.Simendić, G.S.Švenda, V.C.Strezoski, V.Mijatović: *Application of the Distribution State Estimator in "Elektrodistribucija Sombor"*, Journal Elektroprivreda (in Serbian), No. 4, pp. 81-91, 2006.

ANALYSIS OF POWER TRANSFORMER ON LOAD TAP CHANGER (OLTC)

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Abstract: *This paper presents a concept of the analysis of power transformer On Load Tap Changer (OLTC) operating conditions. Tap Changer failures represent over 40% of total failures of power transformers. Analysis of power transformer OLTC operating conditions encourages a big interest at utilities and industry. Reasons for increased interest in this analysis are at first big desire for good utilization of transformers, then increase of transformer reliability caused by prevention of failures and at the end improvement of operator safety and environment conditions. Results of analysis are ilustrated on a power transformer. PC software RMOWin-T5 together with winding resistance ohmmeter RMO50T is used for calculation and drawing of the graphs.*

Keywords: *power transformers, analysis, tap changer, software*

1. INTRODUCTION

Power transformers are critical, capital-intensive assets for utilities as well as for industry. Transformers are extremely reliable devices. However, many of the transformers in use today have already exceeded their design life. Today transformers are not automatically replaced, if they have reached their life span, but left in service as long as possible. In contradiction to the past, power transformers are operated nowadays at or above rated power.

Transformers are subject to vibration. Problems or faults occur due to poor design, assembly, handing, poor environments, overloading or poor maintenance. Failures are appeared on all transformer parts with a certain frequency (Fig.1). In an international analysis there are statically presented data on a sample of 47000 transformer-years. The failures are systematized by the part of the transformer for which is believed that is initially started the failure. The tap changer failures represent more than 40 % of all failures on power transformers.

Measuring the resistance of the windings assures that the connections are correct and the resistance measurement indicates that there are no severe mismatches or opens. Many transformers have taps built into them. These taps allow ratio to be increased or decreased by fractions of a percent. Any of the ratio changes involve a mechanical movement of a contact from one position to another. These tap changes will also be checked during a winding resistance test.

The OLTC are consisted of two parts. Those two parts are diverter switch, which carry the load, and tap selector which chooses the tap positions. Both of these two parts are placed in transformer oil. Fig.2 shows the scheme of the OLTC.

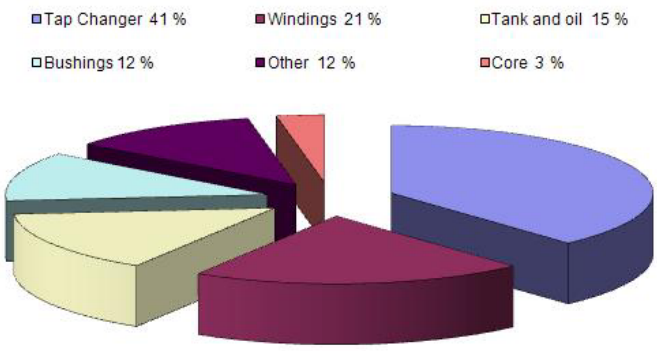

Fig.1. *Allocation of failures through the parts of power transformers with the OLTC*

The tap changer is intended to regulate the voltage of the transformer by increasing or decreasing the certain number of turns. At the European type of transformers the OLTC is placed on primary side.

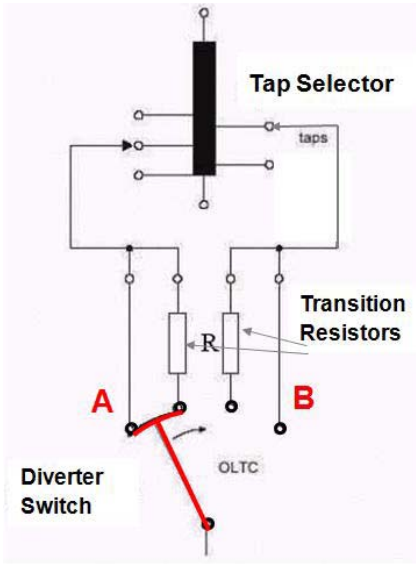

Fig.2. *OLTC scheme*

2. TRANSFORMER STATIC WINDING RESISTANCE MEASUREMENT

Static winding resistance consists of all internal contact resistances increased by the resistance of the windings in certain tap position. The result calculated using Ohm's law: voltage drop divided by the test current R=U/I.

Winding resistance measurements in transformers are of fundamental importance for the following purposes:

- Calculations of the I^2R component of conductor losses,
- Calculation of winding temperature at the end of a temperature test cycle,
- As a base for assessing possible damage in the field.

Regardless of the configuration, either star or delta, the measurements are made phase to phase and comparisons are made to determine if the readings are comparable. If all readings are within one percent of each other, then they are acceptable. Keep in mind that the purpose of the test is to check for gross differences between the windings and for opens in the connections. The tests are not made to duplicate the readings of the manufactured device which was tested in the factory under controlled conditions and perhaps at other temperatures. The scheme of measuring method is shown on Fig.3.

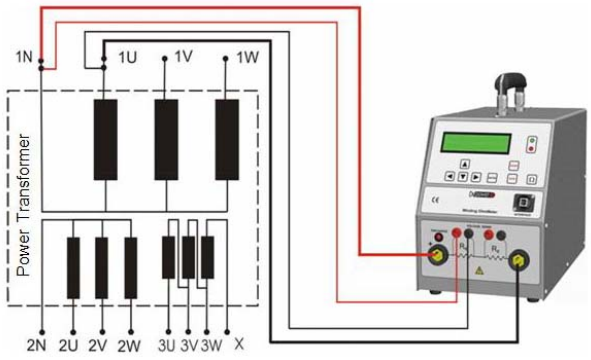

Fig.3. *Method for winding resistance measurement of power transformer*

Fig.4 shows damaged tap selector contacts of power transformer's OLTC.

Figu.4. Damaged tap selector contacts

3. TRANSFORMER DYNAMIC RESISTANCE MEASUREMENT

Up to date, only the static behavior of the contact resistances has been taken into account in maintenance testing and diagnosis of power transformers.

Dynamic resistance here mentioned is actually test current change, which could be detected with RMO50T device in combination with the RMOWin-T5 software, during the change from one tap changer position to the next one. That current is in an inverse proportion with the total resistance of the circuit. The scheme of measuring method for the dynamic resistance measurement is shown on Fig.5.

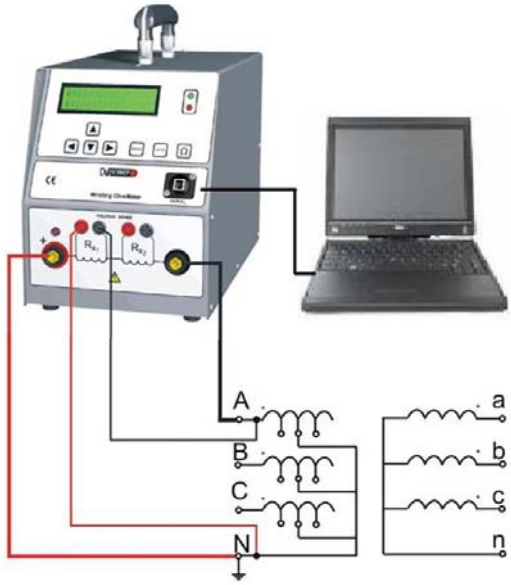

Fig.5. *Method for the OLTC analysis of power transformers*

Switching problems of the diverter switch of the OLTC can be found through dynamic resistance measurements method which is shown on the Fig.6.

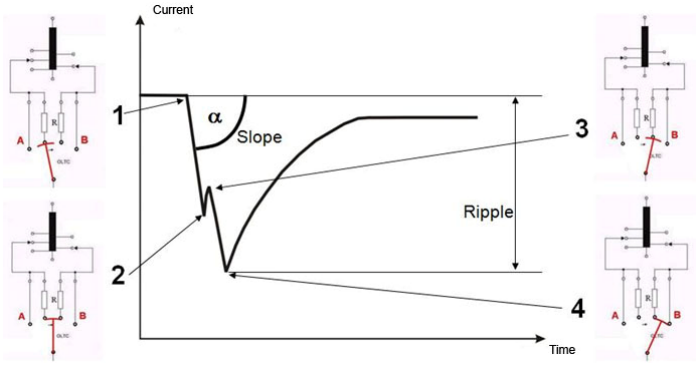

Fig.6. *Dynamic behavior of the diverter switch*

For the dynamic resistance measurement the test current should be as low as possible, otherwise short interruptions or bouncing of the diverter switch contacts cannot be detected. In this case the initiated arc has the effect of shortening the open contacts internally.

During the test of the OLTC, the test instrument should stay in operation all the time when the positions of the OLTC are changed. It enables for the measurement to be performed very fast without necessity to discharge the transformer and then to charge it again for all the tap changes. The test instrument will stabilize the test current after each tap position change.

If the tap changer is faulty (opened) or if there is a short period of time when the circuit is opened, the winding resistance ohmmeter will continue to generate the current, the operator can chose either to continue the test with changing the tap changer to the next position or to stop the test. If the operator stops the test, the instrument will automatically discharge the energy stored into the transformer.

The case of the opened circuit in the tap changer is clearly indicated to the user of the device by message „Discontinuity“ on the display of the instrument. If the circuit is opened, measuring instrument will not damage the transformer at all.

Fig.7 shows aged diverter switch contacts of the OLTC.

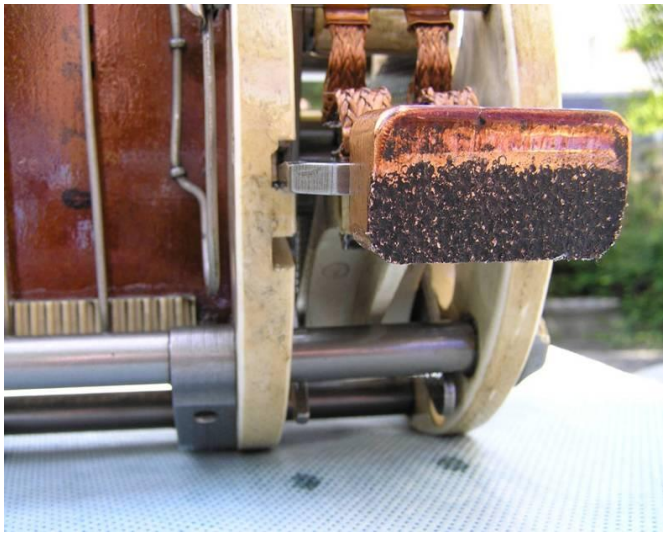

Fig.7. *Aged contacts of the diverter switch*

4. COMPUTER SUPPORT

Specialized PC software RMOWin-T5 is used for data aquisition and storing results of transformer static and dynamic resistance measurements. The software operates on a standard PC configuration using Windows operating system. Connection between PC and test instrument is accomplished using USB interface. The software enables controling the test instrument during measurement and downloading measuring results stored in the internal instrument memory. Static resistance measurements are saved in standard file formats like XLS, CSV and TXT. Fig.8 and 9 show static resistance measurements on two different transformers T1 and T2, while changing the OLTC position from minimum to maximum position. Figure 8 shows good condition of OLTC on transformer T1, while Fig.9 shows bad condition of OLTC on transformer T2.

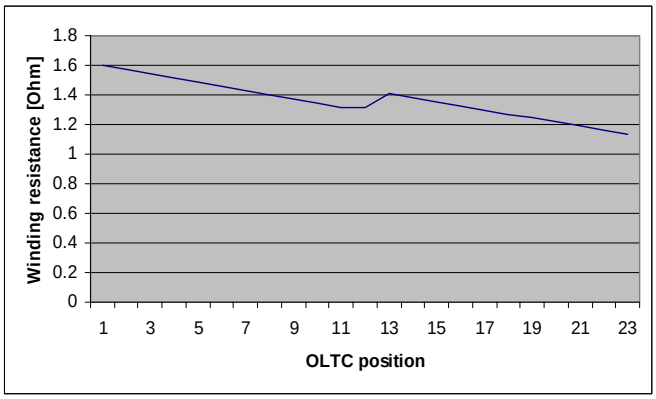

Fig.8. *Static resistance measurement on T1*

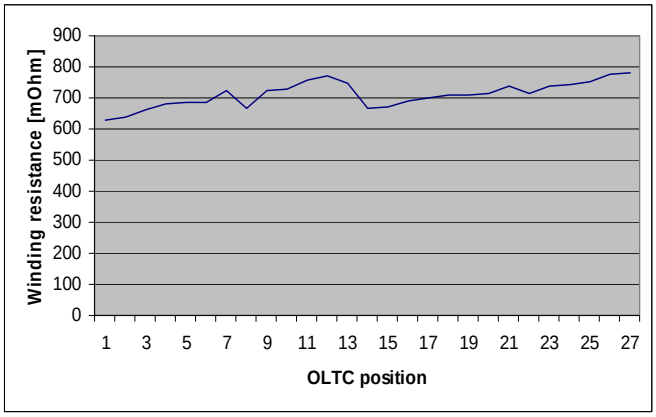

Fig.9. *Static resistance measurement on T2*

Measuring results aquired during the change of OLTC positions are saved in special format that enables graphing the current values while changing from one position to another. Based on this graph, it is possible to diagnose the operating condition of OLTC switching elements. Positions are usually changed starting from the first or the last position. After each position change, the software displays a graph showing current value change during the transition from two subsequent positions. Measured values can be saved after each transition or after completing the measurement by reaching the final OLTC position. The analysis of OLTC operating condition is realized in two separate modes. The first one is on-line mode, while using the test instrument on real test object. The other one is off-line mode, which enables analysing data saved in files.

Fig.10 and 11 show current values while changing the OLTC positions from minimum to maximum on tranformers T1 and T2. The values shown on abscissa denote the transition (e.g. 3>4 for transition from position 3 to position 4), while values on the ordinate denote current value during the transition.

Fig.10 displays a graph which shows good operating condition of T1 OLTC; figure 11 displays a graph which shows bad operating condition of T2 OLTC.

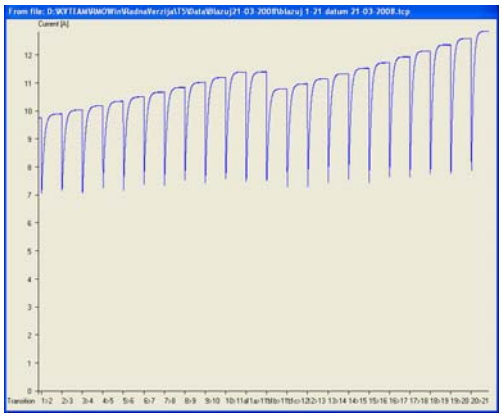

Fig.10. *Current value during transitions on T1*

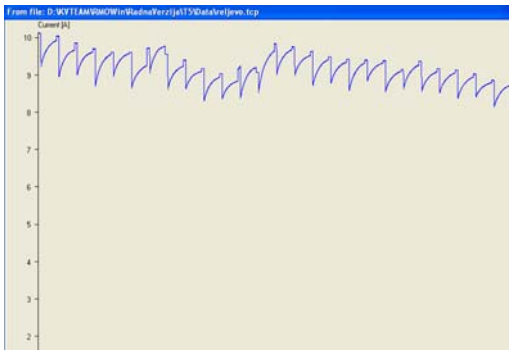

Fig.11. *Current value during transitions on T2*

It is possible to show more detailed diagram by zooming the interesting parts of the graph. The most interesting part on each transition is the part which shows current value during the change from maximum to minimum value. Typical current value diagram is shown on Fig.12. This diagram shows a good condition of OLTC.

Separate control window enables displaying markers on the graph and measuring characteristic values between the markers. Markers can be moved to desired position on the graph. The values shown on the control window are the time interval between two markers, current difference and percent current difference between the markers.

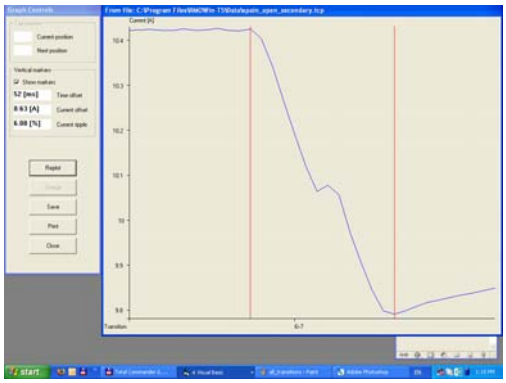

Fig.12. *Current change during one transition*

Fig.13 shows current value during the transition with a short discontinuity. This current diagram is related to bad operating condition of OLTC switching elements.

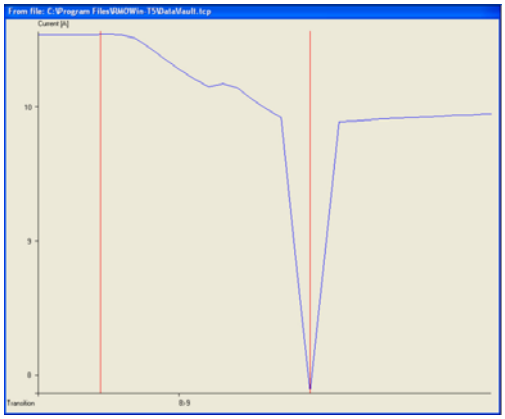

Fig.13. *Current interruption during the transition*

5. CONCLUSION

Transformers are very reliable devices which are able to work corectly for a long time under regular maintenance and service. Transformer failures are very serious and usualy require expensive repairement and long out-of-service time. The most important thing to do in order to prevent failures is to provide correct installation and regular maintenance.

It is required to measure transformer winding resistance each time the transformer testing is done. Modern measuring devices provide reliable, accurate and easy measurement. Comparison to „fingerprint“ resultsIts, which were taken when the transformer OLTC where in good condition and to the other phases, alows for an efficient analysis.

Defective contacts (e.g. tap selector contacts) could be detected by measuring static resistance in all OLTC positions. It is recommended to perform the measurement starting from the first position to final position, and vice versa, and then to compare the measurement results in the same positions.

Switching problems of diverter switch could be detected by measuring dynamic resistance.

Dynamic resistance measurement is a new method still unknown worldwide. A big advantage of this method is that there is no neccessity to open the OLTC, then to remove the oil from the tank, and at the end to see what the problem inside the OLTC is. In such a way maintenance and service costs are significantly decreased.

6. REFERENCES

[1] IBEKO Power AB *“Manual of Winding Resistance Ohmmeter RMO50T, February 2008.*

[2] Michael Krüger *“Fault location on Power Transformers with electrical measuring methods” Klaus, Austria 2007*

INSTRUCTION FOR AUTHORS

Name of the author/s, Affiliation/s

Abstract: *Short instruction for authors is presented in this paper. Works that are to be printed in the review "Electronics" should be typed according to this instruction.*
Keywords: *Review Electronics, Faculty of Electrical Engineering in Banjaluka, Instruction for authors.*

1. INTRODUCTION

In the review "Electronics", we publish the scientific and professional works from different fields of electronics in the broadest sense like: automatics, telecommunications, computer techniques, power engineering, nuclear and medical electronics, analysis and synthesis of electronic circuits and systems, new technologies and materials in electronics etc. In addition to the scientific and professional works, we present new products, new books, B. Sc., M. Sc. and Ph.D. theses.

In order to enable the unification of the technical arrangement of the works, to simplify the printing of the review "ELECTRONICS", we are giving this instruction for the authors of the works to be published in this professional paper.

2. TECHNICAL DETAILS

2.1. Submitting the papers

The works are to be delivered to the editor of the review by the E-mail (elektronika@etfbl.net) or on floppy (or CD) by post mail to the address of the Faculty of Electrical Engineering (Elektrotehnicki fakultet, Patre 5, 78000 Banja Luka, Republic of Srpska, Bosnia and Herzegovina).

2.2. Typing details

The work has to be typed on the paper A4 format, 8.27" width and 11.69" height (21.0x29.7 cm), upper margin of 1" (2.54 cm) and lower margin of 0,59" (1,5 cm), left and right margins of 1,57" (2 cm) and 0,39" (1cm) (mirrored margins). The header and footer are 0,5" (1.27cm) and 57" (2 cm). The work has to be written in English language. Our suggestion to the authors is to make their works on a PC using the word processor MS WORD 97/2000, and for the figures to use the graphic program CorelDraw, if the graphs are not going from the original programs, i.e., from the programs received (like MATLAB).

The title of the work shall be written on the first page, in bold and 12 pt. size. Also, on the first page, moved for one line spacing from title, the author's name together with the name of his institution shall be printed in the letter size (10pt, *Italic)*. The remaining parts of the manuscript shall be done in two columns with 0.5cm distance. The work shall be typed with line spacing 1 (Single) and size not less than 10 pt (like as this instruction). After the title of the work and the name of the author/s, a short content in English language follows, written in italics. The subtitles in the text shall be written in bold, capital letters of the size as in the text (not less than 10 pt.). Each work shall, at the beginning, comprise a subtitle INTRODUCTION, and, at the end, the subtitles CONCLUSION and BIBLIOGRAPHY / REFERENCES.

The operators and size marks that do not use numerical values, shall be written in common letters. The size marks that can use numerical values shall be written in italics. The equations shall be written in one column with right edge numeration. If the breaking of equations or figures is desired, those may be placed over both columns.

Illustrations (tables, figures, graphs etc.) may be wider than one column if necessary. Above a table there shall be a title, for instance: Table 2. *The experimental measuring results.* The same applies to figures and graphs but the accompanying text comes underneath the figure of graphs, for instance: Fig.3: *Equivalent circuit diagram...*

The work should not be finished at the beginning of a page. If the last manuscript page is not full, the columns on that page should be made even. Number of pages should not go over 6.

3. CONCLUSION

This short instruction is presented in order to enable the unification of technical arrangement of the works.

4. REFERENCES

At the end of work, the used literature shall be listed in order as used in the text. The literature in the text, shall be enclosed in square brackets, for instance: ...in [2] is shown ...

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