FACULTY OF ELECTRICAL ENGINEERING
UNIVERSITY OF BANJA LUKA

ELECTRONICS

VOLUME 22, NUMBER 2, DECEMBER 2018

FACULTY OF ELECTRICAL ENGINEERING
UNIVERSITY OF BANJA LUKA

Address: Patre 5, 78000 Banja Luka, Bosnia and Herzegovina
Phone: +387 51 211824
Fax: +387 51 211408
Web: www.etf.unibl.org

E L E C T R O N I C S

Web: www.els-journal.etf.unibl.org
E-mail: els-journal@etf.unibl.org

Publisher:
Faculty of Electrical Engineering, University of Banja Luka, Bosnia and Herzegovina

Number of printed copies: 100

Editor's Column

Mladen Knezic

> Start by doing what's necessary; then do what's possible; and suddenly you are doing the impossible.
>
> *St. Francis of Assisi*

Editorial Letter
DOI: 10.7251/ELS1822057K

BEFORE you is the final issue of the *Electronics* journal in this year and probably the last issue of the journal in this format and appearance. Currently, we are considering making some big steps towards changing the whole design of the journal cover and web presentation. More importantly, we initiated major changes of the journal's aims and scope in order to better reflect recent technology advancements as well as our readership.

The second issue of the volume in this year contains four outstanding papers that present some recent advancements in the fields of testing complex digital electronic circuits, improvement of medium voltage distribution networks reliability, electric machine design and modeling, and power electronics.

The paper "New Hybrid-Based Self-Test Strategy for Faulty Modules of Complex Microcontroller Systems" by M. H. El-Mahlawy, S. Hussein, and G. I. Mohameda presents a new hybrid test strategy, called HYBST, that combines the Signature Multi-Mode Hardware-Based Self-Test (SM-HBST) and Software-Based Self-Test (SBST) testing strategies for testing complex digital circuits such as microcontrollers. In the proposed test strategy, a microcontroller is divided into a number of main modules and, afterwards, the test subroutines are used to functionally test each module, based on its instruction set architecture (ISA). After conducting several experiments, it was shown that HYBST outperforms other testing strategies with regards to memory utilization, test application time, testing of internal modules of the microcontroller, and testing of general-purpose input-output (GPIO) pins of the microcontroller.

The paper "Probabilistic Techno-Economic Optimization in Medium Voltage Distribution Networks with Fault Passage Indicators and Fault Locators" by P. Mršić, Đ. Lekić, B. Erceg, Č. Zeljković, P. Matić, S. Zubić, and P. Balcerek proposes a novel stochastic techno-economic optimization method for determining the number and positions of fault passage indicators (FPIs) aiming at reduction of interruption time and investment costs in medium voltage (MV) distribution networks with and without fault locators (FLs). The proposed method is based on a probabilistic non-sequential Monte Carlo simulation model of the real network and its main goal is to provide maximum improvement of the network reliability indices with minimum number of FPIs.

The paper "Finite Element Design of Rotor Permanent Magnet Flux Switching Machine with Arbitrary Slot, Pole and Phase Combinations" by Đ. Lekić and S. Vukosavić describes a two-dimensional finite element approach for designing RPMFS (Rotor Permanent Magnet Flux Switching) machines. The proposed method enables fast, accurate and computationally efficient assessment of different RPMFS machine designs with an arbitrary number of rotor poles, stator slots and phases. In addition, the authors developed a program using the Octave FEMM (Finite Element Method Magnetics) toolbox. The program is suited for the use in the design stage, where it is necessary to determine various machine parameters for given core dimensions, terminal voltage constraints and adopted value of current density in the conductors, while taking iron saturation effects into account

The paper "Medium Voltage Impedance-Admittance Measurement System Based on the Cascaded H-Bridge Multilevel Converter" by M. Petković, N. Hildebrandt, F. D. Freijedo, and D. Dujić proposes and presents the cascaded H-bridge multilevel inverter topology for perturbation injection converter and impedance-admittance measurement. The measurement methodology is explained together with different measurements requirements. Performance and suitability of this topology for impedance-admittance measurement is evaluated through simulations. Preliminary design principles are given for the converter

I thank all the authors for their contribution to this issue of the journal. I also thank all the reviewer for making significant effort in providing timely and comprehensive reports during the review process.

New Hybrid-Based Self-Test Strategy for Faulty Modules of Complex Microcontroller Systems

Mohamed H. El-Mahlawy, Sherif Hussein, and Gouda I. Mohamed

***Abstract*—In this paper, a new hybrid test strategy, called hybrid-based self-test (HYBST), is presented to test complex digital circuits such as microcontrollers. This test strategy integrates the signature multi-mode hardware-based self-test (SM-HBST) with the software-based self-test (SBST). In this test strategy, the microcontroller is divided into a number of main modules, and then test subroutines are used to functionally test each module, based on its instruction set architecture (ISA). The ISA is used to generate test subroutines that represent test pattern generators (TPGs) and part of the test controller. The SM-HBST represents the other part of the test controller and the test response compaction (TRC). The experimental results illustrate the superiority of the HYBST in the memory utilization, test application time, testing of internal modules of the microcontroller, and testing of general-purpose input-output (GPIO) pins of the microcontroller. In addition, an integrated test solution for fault diagnosis of the circuit boards including random logic integrated circuits (ICs) and microcontroller chips is presented to indicate a real practical test strategy.**

***Index Terms*—Testing of digital circuits; Built-In Self-test for digital circuits; Testing of microcontroller circuits; Software-based self-test; Hardware-based self-test; Hybrid-based self-test.**

Original Research Paper
DOI: 10.7251/ELS1822059E

I. Introduction

With the advent of complex integrated circuits (ICs), the stream data of bits at the available test points of the printed circuit boards (PCBs) or the complex ICs on the circuit under test (CUT) become very complex. Testing the CUT for correct operation after manufacturing is an important issue. It is to apply proper test patterns to the CUT, and the test response generated from the CUT is analyzed to locate the faulty source components. Several testing approaches achieve this objective. Most of them fall into two main categories: in-circuit testing (ICT) and functional testing [1-5]. The ICT requires a costly special kind of the test fixture (bed of nails) [2]-[3], [6]. The functional tester verifies that the CUT board performs the functions it was designed for. Only CUT inputs and CUT outputs need to be tested with inexpensive test fixture (edge connector) [5], [7]-[8].

Microcontrollers are considered an important part of the electronic system. The complexity of microcontrollers with poor accessibility makes their test process a difficult task using external automatic test equipment (ATE) [2]-[3], [6]. Therefore, empowering chip to test itself looks the suitable solution for the microcontroller testing. The built-in self-test (BIST), considered a mechanism of the hardware based self-test (HBST), provides significant advantages not only for processor module but also for other peripherals found in the microcontroller [6]. [8]-[9]. The BIST adds special hardware overhead to the circuit design in the chip level, the board level, and the system level to realize self-test operations. This hardware overhead is the test pattern generator (TPG), the test response compactor (TRC), and the BIST controller. The required test patterns generated from the TPG are applied to the CUT board, and the test responses are compacted using the TRC for fault diagnosis so that the CUT board can be replaced and returned to the service [10]-[11].

The easiest way to test a small circuit is to apply all possible test patterns, called exhaustive testing. This testing is not practical for large circuits [1], [12]-[13]. The more common approach for testing is to use computer algorithms for automatic test pattern generation (ATPG) [2]-[3], [5], [14]-[15]. These algorithms are effective at finding sequences of test patterns that can detect all detectable hardware faults [14]-[15]. Pseudorandom testing is widely used in testing of digital circuits, whose test patterns can be generated by simple hardware circuits [1]-[3], [5]. Signature analysis is a TRC technique that detects errors in stream data of bits, caused by hardware faults. It compacts the test response for each output node of the CUT board into a signature [4], [6], [9]-[11]. After all required input test patterns are applied, the reference (good) signature is generated. This signature is compared with the corresponding measured signature. When they are different, a fault is detected. The signature analyzer (SA) requires the storage of fewer bits. The aliasing probability of an n-stage signature analyzer approaches 2^{-n} [16].

The signature analysis performs the hot functional test for conventional digital random logic ICs, and memory devices [9]. By determining a unique signature for each node in the CUT board, the fault detection and then fault location (fault diagnosis) can be achieved. In addition, another test strategy was presented to functionally test single-shot (SS) circuit on the PCB [17]. It can test the SS circuit by measuring the time duration. The time

Manuscript received 18 September 2017. Received in revised form 21 February 2018, 4 April 2018, and 28 July 2018. Accepted for publication 16 August 2018.

Mohamed H. El-Mahlawy is with Electrical Engineering department, faculty of Engineering and Technology, Future University in Egypt (FUE), Cairo, Egypt (corresponding author: +201121455800; email: mohamed.elmahlawy@fue.edu.eg).

Sherif Hussein is with Computers department, military technical college, Cairo, Egypt (email: sherif.i.morsy@gmail.com)

Gouda I. Mohamed is with Computers department, military technical college, Cairo, Egypt (e-mail: gisalama@mtc.edu.eg).

duration is considered the signature of its proper functionality. The HBST is limited to properly test digital CUT including a microcontroller chip. Adding hardware parts of that HBST have a negative impact on the circuit area and performance degradation. The alternative to the HBST is the software-based self-test (SBST) that promises an attractive and non-intrusive test solution for embedded systems [18].

In the SBST strategy, no extra test hardware is required. Fig. 1 illustrates the concept of the embedded SBST strategy, where the test program is resided in the flash memory of a microcontroller. During the application of the testing, the on-chip test generation program emulates a TPG to generate required test patterns, applied to main modules of a microcontroller. In addition, the on-chip test application program collects the test response and stores them in the memory. The stored test response is compacted into a signature using the TRC program. Test response can later be unloaded and analyzed by an external ATE. At the final stage, the external ATE will provide a decision about the microcontroller under test.

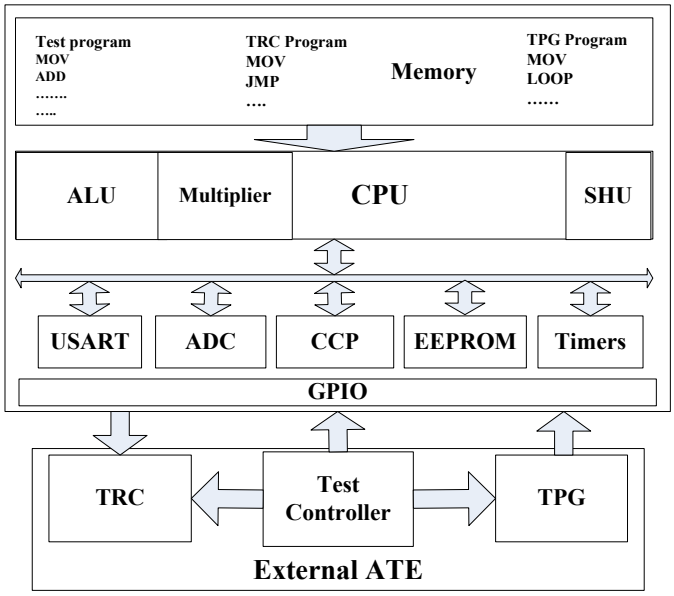


Fig. 1. Block diagram of the SBST strategy.

The SBST strategy is classified in two different categories. The first category is functional in nature [19]. The functional SBST strategy is either based on functional fault models [20]-[23] or based on the checking experiment principle without assuming any fault model [24]. It was found that these approaches are not exactly suited for embedded processor cores and that they achieve low fault coverage. The second category is structural in nature and requires a structural fault driven test development.

L. Chen [25] presented a structural SBST strategy that targets processor components using pseudo-random pattern sequences. This strategy is not considered the regular structure of critical components within a processor and hence leads to large self-test code, large memory requirements, and excessive test application time, even when applied to a small processor model. N. Kranitis [26] presented a structural SBST strategy for testing a processor in an embedded system, based on the divide-and-conquer strategy and the instruction set architecture (ISA) of the processor. For every component and its operations within the processor, deterministic test patterns are generated to detect structural faults. In addition, N. Kranitis [27] introduced a hybrid-SBST strategy that combines deterministic test patterns and random test patterns to test commercial processor cores.

The objectives of an effective SBST strategy are to increase fault coverage, reduce self-test code, reduce memory utilization, and reduce test application time. Therefore, the structural SBST strategy is more efficient than the functional SBST strategy in terms of fault coverage without system modifications, the size of the self-test code, memory utilization, and test application time [18], [26]-[28].

Most of recent researches utilize the SBST strategy for embedded processors and large microprocessors. However, the researches for testing of microcontrollers with small memories, used in industrial applications, are limited. N. Kranitis [29] proposed a low-cost SBST methodology for *Reduced Instruction Set Computer* (RISC) processor cores with the aim of producing small test code sequences. It is based on two phases to test the functional modules such as the *register file*, the *arithmetic-logic unit* (ALU), the *shifter*, and the *multiplier* in the first phase. Then, the control and hidden modules are tested in the second phase. In these phases, a few deterministic test patterns (not ATPG) are used to utilize small test application time. This methodology achieves 92% of the *single stuck-at* fault coverage on the architecture of the Plasma/MIPS model using the fault simulator. This test strategy, proposed in [29], is limited only to test functional modules of the processor with high fault coverage. However, the control and hidden models are tested with low fault coverage. This proposal cannot test microcontrollers with small memories, used in industrial applications.

Dattatraya [30] proposed an expert work for fault diagnosis of the Philips 89v52RD2 microcontroller. He proposed checking experiments for every fault, based on the intelligent diagnostic assessment and management of testing process. The knowledge base consists of a procedural description of the test, and uses the knowledge about troubleshooting process. The results obtained are validated using experts and testing equipment under the same input patterns for automation in knowledge acquisition and updating process. This strategy is limited to test a microcontroller with high fault coverage, and needs huge alteration to get the proper knowledge base. In addition, the authors in [30] did not illustrate the memory utilization, test application time, and the fault coverage for the Philips 89v52RD2 microcontroller under test. Therefore, the authors did not prove the applicability of this test strategy.

The authors in this paper implemented the SBST strategy to test two different families of the PIC microcontrollers (PIC16F87X – PIC18F4X2) [6], [31]. It was found that the SBST needs large space of memory for the instruction set code that emulates the TPG, the TRC, and the test controller to realize self-test operations. In addition, the SBST strategy cannot test most modules in the microcontroller like timers, general-purpose input-output (GPIO) pins and Capture/ Compare/PWM (CCP)

modules without the external ATE. Therefore, the SBST strategy is limited to test microcontrollers with small memories. The necessity to introduce a test strategy for testing microcontrollers with small memories is highly required.

In this paper, the new test strategy for testing microcontrollers, called hybrid-based self-test (HYBST), is presented. It integrates the HBST strategy and the SBST strategy. Due to the diversity of the digital CUT boards in the practical field, the signature multi-mode hardware-based self-test (SM-HBST) strategy is highly required. Therefore, the HYBST strategy integrates the SM-HBST strategy and the SBST strategy. Based on divide-and-conquer strategy, the microcontroller is structurally divided into a number of main modules and test subroutines are constructed to exhaustively test each of these modules. Generation of these test subroutines requires knowledge of the ISA of the microcontroller. The exhaustive testing guarantees the detection of all detectable combinational faults, detected by single-pattern test generator [1], [12]-[13]. This leads to achieve high fault coverage without performance degradation and without fault simulator. Test subroutines, embedded in the microcontroller memory, generate test patterns for each module in a microcontroller chip, and the test response is then propagated to GPIO pins of a microcontroller chip to be compacted by the external SM-HBST. Test subroutines are used to emulate TPG and part of the emulated test controller, running in the microcontroller itself. The SM-HBST outside a microcontroller chip represents the other part of the test controller and the TRC. To realize a real practical test strategy, the merging of the presented HYBST strategy with the developed software part of the SM-HBST is applied as a fault diagnosis solution for electronic digital boards that contains both conventional random logic ICs and a microcontroller chip. It is evaluated on two different families of Microchip microcontrollers; PIC18F4X2 and PIC16F87X [31].

This paper is organized into six sections. The presented section introduces the previous published works. Section II describes the basic concept of the microcontroller test strategy. Section III describes the design and implementation of the SM-HBST strategy. Section IV presents testing of microcontroller modules, and states the comparisons between the HYBST strategy and the SBST strategy using two different families of microcontrollers. Section V presents fault diagnosis of the digital circuit board including random logic ICs and a microcontroller chip, and then section VI illustrates the experimental results of the whole test strategy. Finally, the last section concludes the presented paper.

II. Basic Concept on the Microcontroller Test Strategy

The microprocessor, considered a powerful computing component, may use other components such as memory, timers, and communication peripheral environment. On the other hand, the microcontroller is designed to include the microprocessor and its components in a single integrated circuit. Microcontrollers are popular with industrial developers. The increasing logic-to-pin ratio of the microcontroller poses very serious problems in testing at the board level. These problems lead to an increasingly long test pattern generation, long test application time, and low fault coverage. In addition, the stream data bits at the available test points of the CUT board are large so detecting a hardware fault becomes difficult as well as locating the source faulty node (nodes). The SM-HBST strategy is limited for complex digital circuits such as microcontrollers that have heterogeneous components with poor accessibility.

In this paper, the comparison criteria of testing performance between different test strategies are based on the following:

1) Memory utilization (Data memory – Flash memory) is considered to reduce hardware overhead and to leave the largest space of the available memory for the application program of that microcontroller.
2) Test application time (required number of clock cycles to finish the test).
3) Testability of microcontroller modules reflects the percentage of fault coverage. When the number of tested modules increases, the fault coverage increases.

The SBST strategy cannot test all internal microcontroller modules especially timers, GPIO pins and CCP module. If the SBST strategy can test other modules in a microcontroller, then it will need an external ATE to load measured signatures from microcontroller memory for fault detection. The SBST strategy cannot be applied to test microcontrollers with small memories because it needs large space of memory for the software code to emulate TPG, TRC and test controller of the BIST system. To enable this test strategy to test digital CUT boards including a microcontroller chip, more effort is needed to achieve the criteria of the testing performance, and another test strategy is required to handle this challenge.

In this paper, a new test strategy that combines both the SM-HBST strategy and the SBST strategy is called the hybrid-based self-test (HYBST) test strategy. The HYBST divides the test operation between a microcontroller chip and the SM-HBST. The emulated TPG and part of the emulated test controller are running in the microcontroller itself using test subroutines. In addition, the TRC and the other part of the test controller are running in the SM-HBST outside the microcontroller. Fig. 2 illustrates the block diagram of the HYBST strategy.

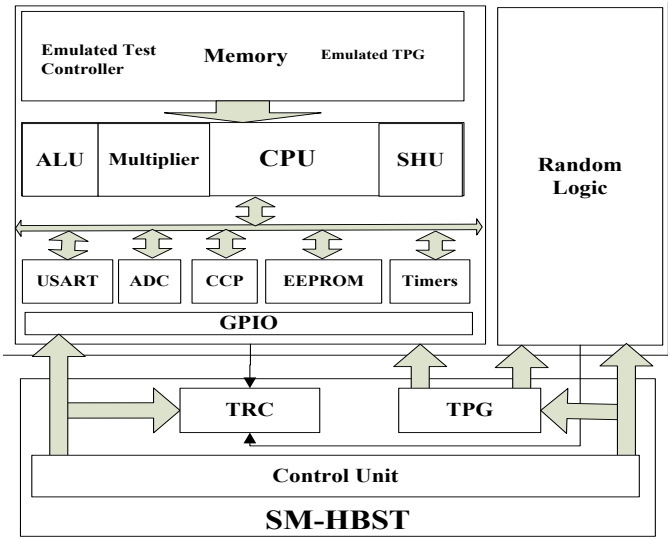


Fig. 2. Block diagram of the HYBST strategy.

Test development of the HYBST is divided into four main phases to construct test subroutines of a microcontroller. The first phase includes information extraction and modules identification of a microcontroller. The second phase is the instruction selection strategy depending on observability and controllability. The third phase is the operand selection, and the last one is the test routine development.

A. Information extraction phase

The information extraction phase shows the features of a microcontroller. According to the divide-and-conquer strategy, the microcontroller is divided into main modules. These modules are the processor, the memory, timers, the pulse width modulation (PWM), GPIO pins, the universal synchronous asynchronous receiver transmitter (USART) and the analog-to-digital converter (ADC). The information on every module is collected to be effectively tested. The ADC module is tested by [32]-[34], and it is not presented in this research. The memory of the microcontroller can be divided into the random access memory (RAM), the electrically erasable programmable read only memory (EEPROM), and the flash memory. In addition, the processor can be divided into an ALU and a multiplier. The effectiveness of this phase is evaluated on certain microcontroller families (PIC16F87X – PIC18F4X2). Table I presents the key features of two microcontrollers.

Table I
Key Features of the Microcontroller

Key Features	PIC16F877	PIC 18F452
FLASH Memory (14-bit Word)	8k Word	16k Word
Data Memory	368 Byte	1536 Byte
EEPROM (Byte)	256	256
I/O Ports	5 I/O Port	5 I/O Port
Timers	3	4
Capture/Compare/PWM Modules	2	2
Serial Communication	USART	USART
Multiplier	-	8 × 8
ISA (instruction set architecture)	35 instruction	75 instruction
Operating speed in Million instruction per second (MIPS)	5 MIPS	10-15 MIPS

B. *Instruction selection phase*

Based on the ISA of the microcontroller [31], it is found that every module M performs a set of operations O_M. $I_{M,O}$ is denoted to the set of microcontroller instructions that, during execution, enable the same control signals and cause module M to perform operation O. It is evident that, for each module M, there is at least one microcontroller instruction that, during its execution, causes module M to perform operation O, i.e. $I_{M,O} \neq \emptyset$. After identification of the set $I_{M,O}$ for every module operation, an instruction I was selected from the set $I_{M,O}$.

These instructions, which belong to the same set $I_{M,O}$:

1) Have different observability properties. When operation O is performed, the outputs of module M conduct internal microcontroller registers with different observability characteristics.
2) Have different controllability properties. When operation O is performed, the internal microcontroller registers with different controllability characteristics conduct the inputs of module M.

After identification of the set $I_{M,O}$, select an instruction $I \in I_{M,O}$ according to the following criteria:

Criterion 1: Discard instructions $\in I_{M,O}$ that when operation O is performed, the outputs of module M do not propagate to internal registers of the microcontroller. This means that the faulty component output cannot be propagated. For example, instructions *CALL* (call subroutine), *RETFIE* (return from interrupt), *RETLW* (Return with literal in *W* register (accumulator)) and *SLEEP* (go into standby mode) don't propagate to internal microcontroller registers.

Criterion 2: Between instructions I_A and $I_B \in I_{M,O}$, if I_A requires a smaller instruction sequence to propagate the outputs of module M to GPIO pins, I_A is ranked higher priority than I_B. It means that I_A is more easily observed than I_B, and it should be preferred over I_B. For example, instruction XORWF (Exclusive-OR *W* register and *f* (Register file address (0x00 to 0x7F))) is easily observed over XORLW (Exclusive-OR literal and *W* register) because it can be used to directly transfer the output to external ports.

Criterion 3: If instructions I_A and $I_B \in I_{M,O}$ have the same priority based on *criterion* 2, another criterion is required. Therefore, if I_A requires a smaller instruction sequence to generate a specific test pattern at the internal register of the microcontroller, I_A is ranked higher than I_B. For example, instruction INCF (Increment *f*) has higher priority over INCFSZ (Increment *f*, skip if zero) because it uses less clock cycles when it is executed.

At the end of this phase, test instructions are selected, based on the above three criteria. They are considered the main foundation of embedded test subroutines that test microcontroller modules. After the O_M and the $I_{M,O}$ set are identified, the number of these instructions are reduced. It should be noted that module M executes operation O during its instruction execution but the module outputs are not propagated to GPIO pins. It is not included in the $I_{M,O}$ set according to *Criterion* 1. If part of the test response of a module is not driven to a well accessible internal register (that is the case of flag outputs, driving status register or special function registers), an extra instruction sequence is required to propagate to accessible registers and then to GPIO pins. Table II and Table III illustrate the instruction reduction of the CPU module of microcontrollers (PIC18F452 – PIC16F877).

C. *Operand selection phase*

Operand selection phase chooses the appropriate test patterns to use it with test subroutines in order to get high fault coverage. The presented test strategy in this paper is based on exhaustive testing for test pattern generation to achieve high structural fault coverage for each module of the microcontroller. It detects all

detectable combinational faults detected by single-test pattern without using the fault simulator [1], [5], [6], [12]-[13].

TABLE II
INSTRUCTION REDUCTION OF THE CPU MODULE OF THE PIC16F877

Module *M*	Operation *O* that can be executed by this module	$I_{M,O}$ used to test this module according to *Criteria* 1, 2 & 3
CPU ALU	ADDWF, ANDWF, CLRF, CLRW, COMF, DECF DECFSZ, INCF, INCFSZ, IORWF, MOVF, MOVWF NOP, RLF, RRF, SUBWF SWAPF, XORWF, BCF, BSF, BTFSC, BTFSS, ADDLW, ANDLW, CALL, CLRWDT, GOTO, IORLW, MOVLW, RETFIE, RETLW, RETURN, SLEEP, SUBLW, XORLW	CLRF , CLRW, MOVLW, BCF, ADDWF, SUBWF, XORWF, IORWF, ANDWF, COMPF, DECF, INCF, MOVWF, MOVF, BSF, ADDLW, BTFSS, GOTO, RETURN
	35 instruction	19 instruction

The next sections present the fourth phase. It describes the design and implementation of the SM-HBST strategy, presented in section III. In addition, test subroutines that test internal modules of a microcontroller are presented in section IV. These test subroutines have been completely implemented using the previous SBST strategy with two different compaction techniques and the HYBST strategy. Test subroutines are developed for each of the microcontroller modules based on the above three criteria using both assembly and *C* programming languages.

TABLE III
INSTRUCTION REDUCTION OF THE CPU MODULE OF OF THE PIC18F452

Module *M*	Operation *O* that can be executed by this module	$I_{M,O}$ used to test this module according to *Criteria* 1, 2 & 3
CPU ALU	ADDWF, ADDWFC, ANDWF, CLRF, COMF, CPFSEQ, CPFSGT, CPFSLT DECF, DECFSZ, DCFSNZ, INCF, INCFSZ, INFSNZ IORWF, MOVF, MOVFF, MOVWF, NEGF, SETF, SUBFWB, SUBWF, SUBWFB, SWAPF, TSTFSZ XORWF, BCF, BSF, BTFSC BTFSS, BTG, BC, BN, BNC, BNN, BNOV, BNZ, BOV BRA, BZ, CALL, CLRWDT, DAW, GOTO, NOP, POP PUSH, RCALL, RESET, RETFIE, RETLW, RETURN SLEEP, ADDLW, ANDLW, IORLW, MOVLB, MOVLW, RETLW, SUBLW, XORLW, TBLRD*, TBLRD*+, TBLRD*-, TBLRD+*, TBLWT*, TBLWT*+, TBLWT*-, TBLWT+*	CLRF , MOVLW, MOVWF, XORWF, SUBWF, ANDWF, IORWF, ADDWF, COMPF, SWAPF, XORLW, ADDLW, ANDLW, SUBLW, IORLW, DECF, INCF, BSF, BNZ, RETURN
	68 instruction	20 instruction

III. DESIGN AND IMPLEMENTATION OF THE SM-HBST

In this section, the FPGA-based design and implementation of the SM-HBST for testing the digital CUT is presented. The SM-HBST is responsible of generating the required test patterns to the CUT through the TPG, compacting the test response from the target test node on the CUT through the TRC, and controlling the test cycle of the presented self-test strategy through the control unit (CU). The main block diagram of the SM-HBST, shown in Fig. 3, is composed of the TPG, the TRC, and the CU. In addition, the schematic diagram of the FPGA-based design is illustrated in Fig. 4. The SM-HBST has four main test modes; pseudorandom test mode (PRT mode), deterministic test mode (DET mode), hybrid test mode between the PRT and the DET mode (HPDT mode), and single-shot test mode (SS mode).

A. *Design of the PRT mode*

In the PRT mode, the TPG tests the digital CUT as a test stimulus. It stimulates all nodes in the CUT. The TPG, based on the PRT mode, is called pseudorandom TPG (PRTPG). The simplified block diagram that shows the basic test operation of a CUT in the PRT mode is shown in Fig. 5. Test patterns, generated from the PRTPG, are applied to the CUT and the test response is captured by the TRC every clock cycle. The TRC compacts all bits of a test response, generated from a stimulated node into a measured signature. The measured signatures are stored and compared to the reference (good) signatures for fault diagnosis. The TRC in the SM-HBST, shown in Fig. 3, has two blocks; the SA and the edge detection compactor (EDC). The SA is a linear feedback shift register (LFSR) as a compactor circuit [1], [6], [10]-[11]. The SA, designed in the SM-HBST, is the 23-bit whose primitive polynomial equals to $1 + x^5 + x^{23}$ with aliasing probability 0.000012 % (2^{-23}). Therefore, the probability of detecting error bits of a test response, clocked to the 23-stage SA, equals to 99.9999 %. The EDC will be discussed later in section *C*.

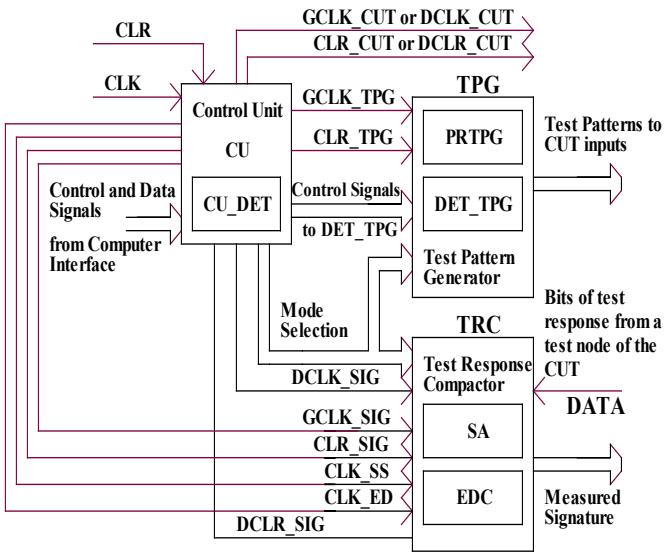


Fig. 3. Main block diagram of the SM-HBST.

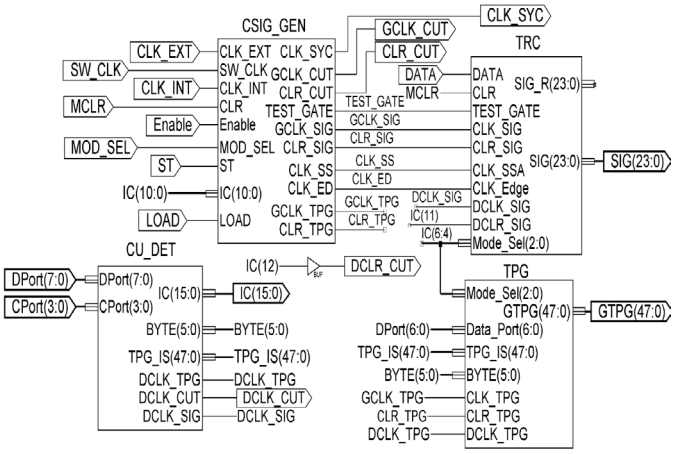


Fig. 4. Schematic diagram of the FPGA-based design of the SM-HBST.

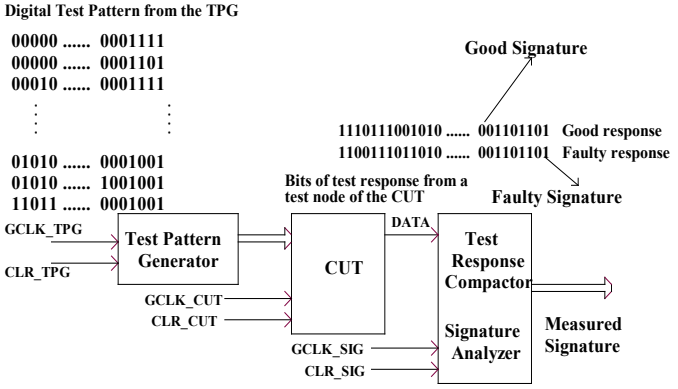


Fig. 5. Simplified block diagram of the test operation in the PRT mode.

The CU, shown in Fig. 3, is implemented with two modules *CSIG_GEN* and *CU_DET* in the FPGA-based design, shown in Fig. 4. Either the internal clock (CLK_INT) or the external clock (CLK_EXT) synchronizes the main clock of the module CSIG_GEN that controls each part of that test scheme. Both internal and external clock are utilized to synchronize the test operation. The selection of the clock is based on the control signal *SW_CLK* that switches between the *CLK_INT* and the *CLK_EXT*, shown in Fig. 4. The presented SM-HBST board unit has the TPG with forty-eight outputs that stimulate all nodes in the CUT with at most forty-eight inputs. To increase the test capability of large CUT inputs (more than forty-eight inputs), two or more SM-HBST board units can be used. The clock *CLK_SYC*, generated from module *CSIG_GEN* of the first SM_HBST board unit, is designed to synchronize the second SM_HBST board unit by feeding the *CLK_EXT*.

Fig. 6 shows the timing diagram of the test operation in the PRT mode. The required clocks and clear signals for the test operation are properly asserted. All clocks during the test gate are three-phase clocks, shown in Fig. 7. By applying known input test patterns from the bus *GTPG*(47:0) to the CUT, an unique signature can be generated at each node in the CUT. The PRTPG is clocked by *GCLK_TPG* and the SA is clocked by *GCLK_SIG*. The test patterns, generated from the PRTPG, are asserted at the rising edge of the *GCLK_TPG*, and the SA is asserted at the falling edge of the *GCLK_SIG*. The *GCLK_CUT* clocks the practical digital CUT either at the rising edge trigger or at the falling edge trigger. The required clear signals of each clock signal; *CLR_TPG*, *CLR_SIG*, and *CLR_CUT* are designed for proper timing operation to start the test gate as shown in Fig. 7(a). They are properly asserted at the starting of every test gate to provide the proper initialization of sequential circuits in the CUT. In addition, the closing of the test gate is shown in Fig. 7(b).

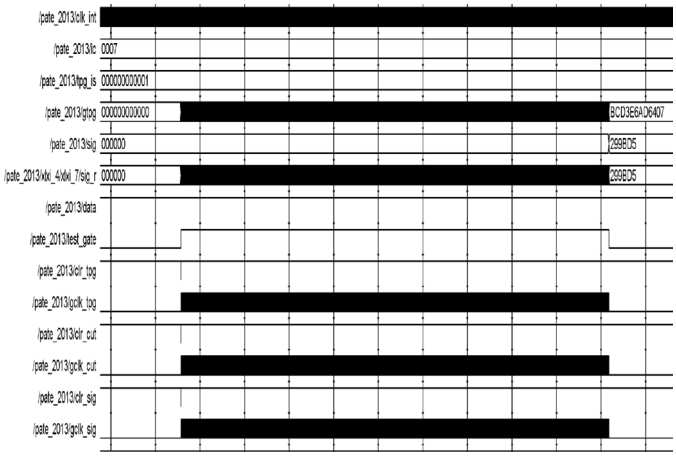
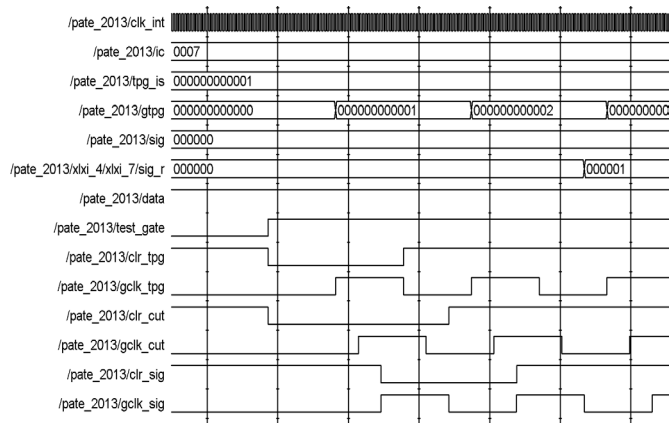


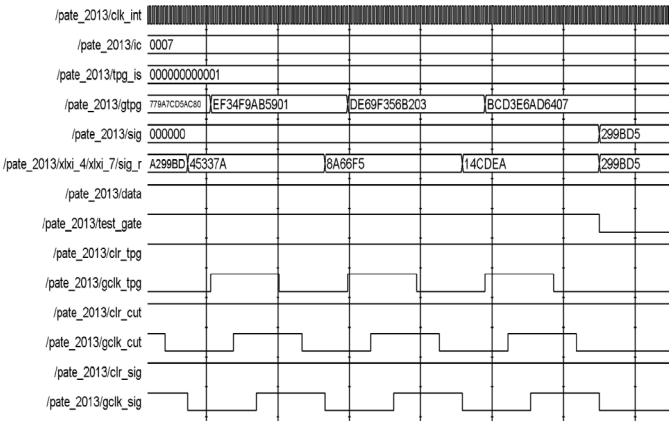
Fig. 6. Timing diagram of the test operation in the PRT mode.

The SA processes the output bits of a target node every clock cycle during the test gate interval. The test gate is controlled by the control signal *TEST_GATE*. After certain clock cycles, the test gate is closed, and the final signature is generated from the bus *SIG*(23:0). Three-phase clocks provide the test pattern enough time to propagate through the integrated circuits in the CUT either at the rising edge trigger or at the falling edge trigger of the *GCLK_CUT*, before the acquisition of the test response (received through the input signal, DATA, showed in Fig. 3, Fig. 4, and Fig. 5). The assertion of the proper timing ensures the stability of the signature generation for the proper test operation. The incorrect signature will accurately indicate an incorrect waveform of the target node as long as the error appears in the bits of the test response. The error appears only if the TPG generates the test patterns that detect hardware faults and the SA generates the incorrect signature. Data compaction is achieved by probing the target node asserted at the falling edge of *GCLK_SIG* during the *TEST_GATE*. The input binary sequence may be in different lengths but at the end of the test gate only the signature is the residue of the SA. The outputs of the SA has proper hexadecimal signature “299BD5” when the DATA sets HIGH.

The system has master clear (*MCLR*). The control signal, *Enable*, is set HIGH to enable the test operation. The switching between multiple opening and the single opening of the *TEST_GATE* is based on the control signal *MOD_SEL*. When the *MOD_SEL* sets LOW, the *TEST_GATE* is opened once to calculate a new signature, and the control signal *ST*, shown in Fig. 4, is asserted for every new signature. The multiple opening of *TEST_GATE* is used, when *MOD_SEL* sets HIGH. The module *CU_DET* in the *CU* produces the programmable code



(a) Starting test gate.



(b) Closing test gate.

Fig. 7. Timing waveforms of the starting and closing test gate interval.

IC(15:0) to configure the test scheme. It is considered the initial condition code to the target chip for proper test operation. Table IV illustrates the control code *IC*(3:0) to produce the test clocks and the phase delay between the three-phase clocks. Table V illustrates the control code *IC*(6:4) for the selection of the test operation modes. The control code *IC*(10:7) illustrates the required number of clock cycles inside the *TEST_GATE*.

Table IV
Generated frequency and the phase delay according to *IC*(3:0) or *N*

N	three-phase clocks		*Delay*	*N*	three-phase clocks		*Delay*
	Period	Frequency			Period	Frequency	
1	240 ns	4.17 MHz	40 ns	9	1200 ns	833.3 kHz	200 ns
2	360 ns	2.78 MHz	60 ns	10	1320 ns	757.6 kHz	220 ns
3	480 ns	2.08 MHz	80 ns	11	1440 ns	694.4 kHz	240 ns
4	600 ns	1.67 MHz	100 ns	12	1560 ns	641.0 kHz	260 ns
5	720 ns	1.39 MHz	120 ns	13	1680 ns	595.2 kHz	280 ns
6	840 ns	1.19 MHz	140 ns	14	1800 ns	555.6 kHz	300 ns
7	960 ns	1.04 MHz	160 ns	15	1920 ns	520.8 kHz	320 ns
8	1080ns	0.93 MHz	180 ns				

Table V
Test Modes According to *IC*(6:4)

IC(6:4)		Test Modes
“000”	Mode 0	Pseudorandom testing only
“001”	Mode 1	Deterministic testing only
“010”	Mode 2	Programming deterministic testing for TPG
“011”	Mode 3	Hybrid the deterministic testing with pseudorandom testing
“100”	Mode 4	Single-Shot testing in microsecond range
“101”	Mode 5	Single-Shot testing in millisecond range

B. Design of the DET mode

Some inputs of the CUT board need the specific binary states; not pseudorandom binary signals. The TPG, based on the *DET* mode, is the DET_TPG whose outputs are 48-bit. The DET_TPG that tests the CUT board as a test stimulus generates deterministic test patterns with arbitrary test length. These test patterns are calculated from algorithmic methods that support the detection of different fault models [2]-[3], [5], [14]-[15]. The DET_TPG retrieves these test patterns and generates all required control signals to automatically transfer these test patterns to the CUT inputs. In the *DET* mode, the start, stop, and all control signals of the deterministic test cycle are generated from the data port *DPort*(7:0) and the control port *CPort*(3:0). These ports are applied to the *CU_DET* module by the personal computer (PC), shown in Fig. 4. These ports generate the required control signals for the proper test operation in the DET mode.

The *CU_DET* module generates the *DCLK_TPG* to synchronize and control the test pattern rate of the DET_TPG at the rising edge. In addition, it generates the *DCLK_CUT* that clocks the CUT board either at the rising edge trigger or at the falling edge trigger before the receiving of the test response of the *DATA* by the SA, clocked by the *DCLK_SIG* at the falling edge. In this case, the number of clock cycles inside the test gate depends on the required test patterns to test the CUT board in the *DET* mode. In the *DET* mode, *IC*(11) is the signal that clears the SA at the beginning of the test gate, and the *IC*(12) is used to clear the memory element in the CUT board in the *DET* mode. When the test gate is closed, the proper signature is generated. After that the next three bits *IC*(15:13) are used to automatically transfer the signature to the PC through the status port.

The *CU_DET* module has three sub-modules. They are the decoder of the *CPort*(3:0), the initial condition port (ICP) for the generation of *IC*(15:0), and the initial seed port (ISP) of the PRTPG (*TPG_IS*(47:0)). Table VI illustrates the truth table of the decoder of the *CU_DET*. Each state of *CPort*(3:0) generates a specific control signal. The data port *DPort*(7:0) is used to write the command in the ICP and the data in both the ISP (*TPG_IS*(47:0)) and the DET_TPG (*GTPG*(47:0)).

Table VI
Truth Table of the Decoder of the CU_DET module.

CPort(3:0)	*Control Signal*	*Function*
“0000”	BYTE(0)	Latch the *GTPG*(7:0) and *TPG_IS*(7:0)
“0001”	BYTE(1)	Latch the *GTPG*(15:8) and *TPG_IS*(15:8)

CPort(3:0)	*Control Signal*	*Function*
"0010"	BYTE(2)	Latch the *GTPG*(23:16) and *TPG_IS*(23:16)
"0011"	BYTE(3)	Latch the *GTPG*(31:24) and *TPG_IS*(31:24)
"0100"	BYTE(4)	Latch the *GTPG*(39:32) and *TPG_IS*(39:32)
"0101"	BYTE(5)	Latch the *GTPG*(47:40) and *TPG_IS*(47:40)
"0110"	BYTE_L	Latch the *IC*(7:0)
"0111"	BYTE_H	Latch the *IC*(15:8)
"1000"	Reserved	Reserved
"1001"	Reserved	Reserved
"1010"	DCLK_TPG	Clock the DET_TPG
"1011"	DCLK_CUT	Clock the CUT
"1100"	DCLK_SIG	Clock the SA
"1101"	DCLK_IC	Clock the *IC*(15:0)
"1110"	DCLK_IS	Clock the *TPG_IS*(15:0)
"1111"	Reserved	Reserved

Each 48-bit deterministic test pattern needs six latches to sequentially store six data bytes of *DPort*(7:0). From Table VI, there are six control signals *BYTE*(5:0) that control the latching data and the *DCLK_TPG* clocks the latched data to simultaneously transfer to *GTPG*(47:0) through the DET_TPG in the TPG module. This sequence is repeated each test pattern generation. In the same way, the *DCLK_IS* clocks the latched data to simultaneously transfer to *TPG_IS*(47:0). In addition, the *DCLK_SIG* clocks the SA in the TRC module, and the *DCLK_CUT* clocks the CUT board outside the SM-HBST. Finally, there are two control signals *BYTE_L*, and *BYTE_H* that control the latching data and the *DCLK_IC* clocks the latched data to simultaneously transfer to *IC*(15:0). The programmable code *IC*(15:0) controls the presented test architecture. The problem of the glitch-free affects the control of the test cycle in the *DET* mode. Different delays in the decoder of the *CU_DET* generate glitches in the outputs of control signals. To eliminate these glitches, the signal *DPort*(7) is used to disable the decoder during the changing states of the *CPort*(3:0). This situation eliminates glitches and provides stable test operation in the *DET* mode.

Some inputs of the CUT board need a fixed binary state, and the other inputs need pseudorandom binary signals. The hybrid between the PRT mode and the *DET* mode, called *HPDT* mode, divides inputs of the CUT board into two sets. The first set needs a fixed binary state as a single deterministic test pattern, generated from the *DET_TPG*. The other set needs pseudorandom binary signals, generated from the *PRTPG*. Therefore, test patterns applied to board inputs are the concatenation of the *PRTPG* and *DET_TPG* through the multiplexer selections. This mode increases the ability of the SM-HBST to test different circuit topology.

C. *Design of the SS mode*

The microcontroller oscillator uses quartz crystal for its operation. The frequency of such oscillator is precisely defined and very stable that makes it ideal for time measurement. If it is necessary to measure time between two events, it is sufficient to count pulses generated by this oscillator. In practice, pulses generated by the quartz oscillator are applied either directly or via a prescaler to increment the number stored in the timer register. In the *TRC* module of the SM-HBST, the edge detection compactor (*EDC*) measures the time interval of the stimulated pulse, generated from at least one basic timer module of the microcontroller. The time measurement of the stimulated pulse is considered the measured signature of the output of the single-shot (*SS*) circuit. The simplified block diagram that illustrates the testing application of an *SS* circuit is shown in Fig. 8. In the SS mode, a sequence of deterministic test patterns, generated from *DET_TPG*, is utilized to trigger the SS circuits for the proper pulse generation. The testing criterion of the *EDC* is used to generate the measured signature, based on the edge detection of the *SS* signal. In addition, the interaction between the *EDC* of the SM-HBST and the testing of the timer module in the microcontroller is presented in section IV (part D).

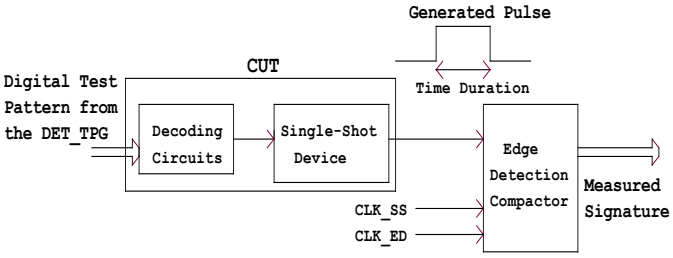


Fig. 8. Digital testing of the SS circuit in the SS mode.

The schematic diagram of the *EDC* and the timing waveform of it are shown in Fig. 9 and Fig. 10, respectively. The *CU* in Fig. 3, and the *CSIG_GEN* module in Fig. 4 generate the required test signals to control the *EDC* in the *SS* mode by two clocks; *CLK_SS*, and *CLK_ED*. The *CLK_SS* (1 MHz in μs range and 1 kHz in ms range) is used to measure the time duration of the stimulated pulse. The *CLK_SS* clocks the 23-bit binary counter (*SS_Counter* shown in Fig. 9). The *CLK_ED* (5 MHz in μs range and 1 MHz in ms range) is used to generate two synchronized pluses; *Edge_1* and *Edge_2*. They are generated either at the rising edge or at the falling edge of the stimulated pulse (*DATA*) of the *SS* circuit. When both edges of the pulse are asserted, the *Edge_1* is generated and the falling edge of it triggers the *Edge_2*, shown in Fig. 10. The *SS* counter starts the counting by the *CLK_SS* and the *ST_STOP* signal generated from *Edge_1* and *Edge_2*. *Edge_1* is a latch pulse for the *SS_LATCH* cell. The assertion of *Edge_1* latches the bus *SSCO*(23:0) to the output bus *SS_SIG*(23:0), and then to output bus of the *TRC* (*SIG*(23:0)). The assertion of *Edge_2* is to clear the *SS_counter*.

D. *FPGA Implementation of the SM-HBST*

All modules of the presented design are connected and the timing simulation of the complete design is achieved to verify the proper operation of the chip design before the implementation on the FPGA chip (Xilinx - X3S200FT256-4). Other cells are used to assist the interface between the inputs and the outputs of the whole chip and the interface circuitry. The debouncer of the *MCLR*, and the other debouncers of the push-bottom switches are used to provide the required *test mode* selection and the required clock selection. In addition, the module that displays a signature of the presented design through the seven-segment

display is used. The device utilization summary and the timing summary report, generated from the FPGA implementation, are presented in Table VII.

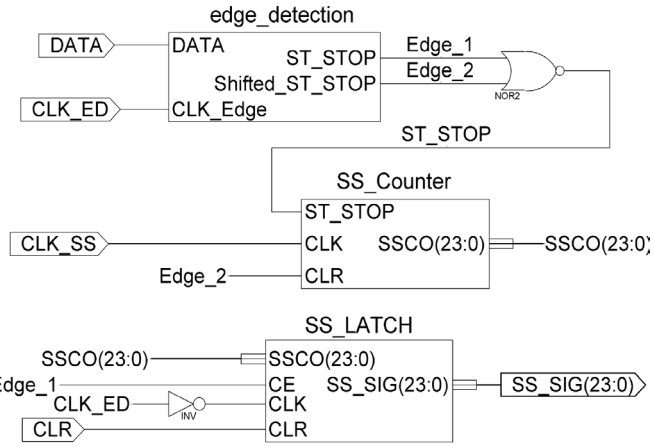


Fig. 9. Schematic diagram of the EDC of the SM-HBST.

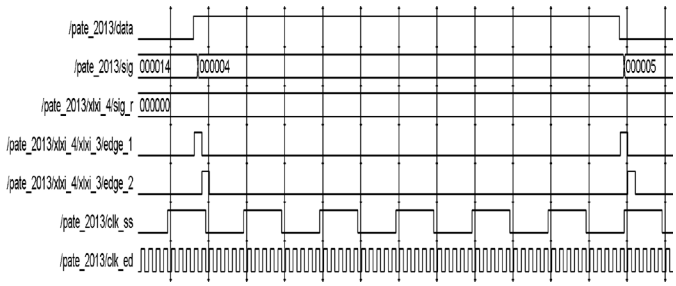


Fig. 10. Timing waveforms of the testing of the SS circuit in the SS mode.

Table VII
FPGA Utilization Summary and Timing Summery of the Spartan-3 (xc3s200-4ft256)

Logic Utilization	Used	Available	Utilization
Number of occupied Slices	411	1,920	21%
Number of Slice Registers	491	3,840	12%
Number of 4 input LUTs	439	3,840	11%
Number of bonded IOBs	115	173	66%
Number of GCLKs	8	8	100%
Number of DCMs	4	4	100%
Total equivalent gate count for design: 34,373			
Timing Summary: Speed Grade -4			
Minimum period: 17.928ns (Maximum Frequency: 55.779MHz)			
Minimum input arrival time before clock: 11.375ns			
Maximum output required time after clock: 16.976ns			
Maximum combinational path delay: 11.600ns			

IV. Testing of Internal Microcontroller Modules

The complexity of microcontrollers that have heterogeneous components with poor accessibility makes their test process a difficult task. In this section, the test process of the internal microcontroller modules is presented. The flowchart of the complete test program of the HYBST strategy for Microchip PIC microcontrollers is illustrated in Fig. 11. The test program asks first, if the system is going to operate either in the normal mode or in the test mode. If the normal mode is chosen, the system will do the predefined industrial application, and if it operates in the test mode, the system will be prepared to operate in the test mode. In the test mode, the microcontroller receives an input selection from one of its ports (*PORTA*), used to test a specific module. This input selection is sent from the SM-HBST. Other microcontroller ports are set output ports to propagate the test response to the SM-HBST.

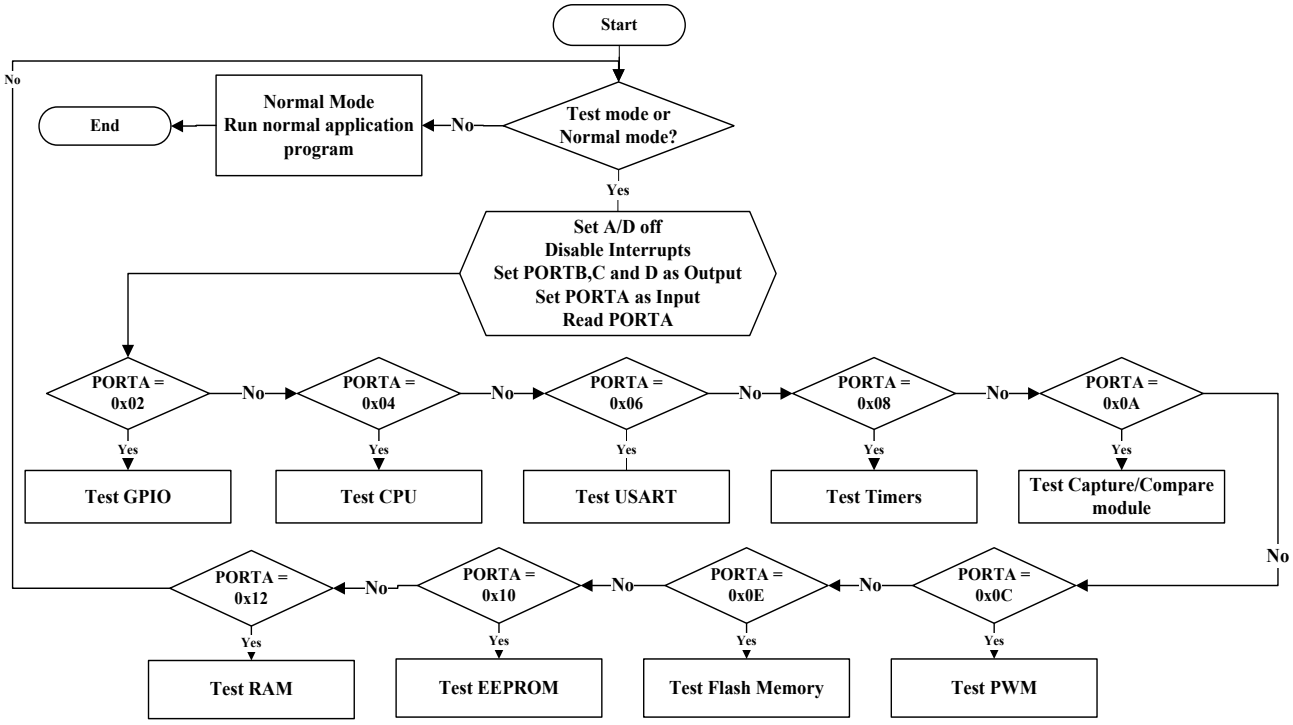


Fig. 11. The flowchart of the complete test program of the HYBST strategy for Microchip PIC microcontrollers.

The test program is composed of several test subroutines, stored in the flash memory of the microcontroller. Test subroutines are based on the ISA of the microcontroller. The emulated TPG of the HYBST provides the required test patterns for testing each internal module of the microcontroller. Test response of each internal module is propagated to the SM-HBST for test response compaction through GPIO pins of the microcontroller. Test subroutines were written in *mikroC* compiler and were simulated in Proteus 7 professional.

A. GPIO test

GPIO pins of the microcontroller allow observing and controlling modules of the microcontroller. Some pins are multiplexed with alternate functions. For all ports, the data direction register, called the TRIS register, controls the directions of I/O pins (either input or output). In this test, GPIO pins (PORTB, PORTC and PORTD) are set output ports. Then, test subroutine sends exhaustive test patterns to these ports. It is noted that some of microcontroller ports are used in other tests, shown in the next sections. Other ports like PORTA and PORTE operate in the input mode to help in running test subroutines and swapping the operation between the test mode and the normal mode. The GPIO test is designed and implemented using the HYBST strategy only. Reference signatures of the GPIO test, based on the SM-HBST, are shown in Table VIII (Last two columns of the table).

Table IX shows the statistics of the GPIO test for the HYBST strategy in terms of memory utilization and the total number of clock cycles for both PIC16F877 and PIC18F452. GPIO pins cannot be tested using the SBST strategy.

Table VIII
Reference signatures of the CPU test and GPIO test

Port	PIN	*signatures of the CPU test*		*signatures of the GPIO test*	
		PIC 16F877	PIC 18F452	PIC 16F877	PIC 18F452
PORTD	0	4F461D	3C2EAD	FFB597	98A6B8
	1	207353	F2C053	4B4474	30B502
	2	16CCD1	86F82A	15C0F5	C40F5E
	3	F5C88A	9AA92E	803D50	8077CC
	4	589ED2	4BDB14	4E4EAF	A0DC17
	5	19F564	243FD2	53F0E0	9A5D2C
	6	449194	8EF7CD	00E9F9	CB508C
	7	AD4496	EB5A81	3F4772	7F1705
PORTB	0			77B646	6E592F
	1			B3FF0A	EF6287
	2			38714E	5D5B1D
	3			046D41	1AD23C
	4			188AE6	DF0D0E
	5			352BC7	6C503A
	6			FD55AC	5F26C3
	7			A5F29A	F341F5
PORTC	0			51F32A	DC2A3F
	1			132938	371FEC
	2			7E08EF	442883
	3			AA24AD	3EEEF0
	4			725B95	9AD2DA
	5			667634	746187
	6			E22CDD	D352F1
	7			ADE6ED	D4FE96

Table IX
Statistics of the GPIO Test for Both PIC16F877 and PIC18F452

GPIO test	Unit	HYBST	
		PIC16F877	PIC18F452
RAM utilization	Byte	16 4.34 %	21 1.36 %
Flash Memory utilization	Word	37 0.45 %	56 0.17 %
Clock cycles	Clock cycle	5,232	6,224

B. CPU test

The central processing unit (CPU) is the brain of the microcontroller. It is responsible for fetching the correct instruction for instruction decoding and then executing it. The CPU executes the instruction to control the microcontroller operation. It controls the address bus of the program memory, the address bus of the data memory, and the accesses to the stack. The CPU is structurally divided into small sub-modules. In this paper, the test subroutine structurally divides the CPU into the ALU, the shift unit (SHU), and the 8*8 multiplier. The ALU performs arithmetical and logical operations, and controls status bits, found in the STATUS register. The result of some instructions forces status bits to a value depending on the state of the result.

In the CPU test, the test subroutine is designed and is then implemented to functionally test the CPU of the microcontroller for both the HYBST strategy and the SBST strategy. The CPU test is based on the divide-and-conquer strategy and the exhaustive testing. The CPU instructions are selected based on the above three criteria, presented in section II. Instruction set $I_{M\text{-}CPU,O}$ from Table II and Table III can test the CPU module. Moreover, the instructions are not randomly chosen, but they are carefully crafted in order to test the desired sub-modules of the CPU. Faulty sub-modules are detected by applying the proper instruction, and then the results of this instruction must be directly sent to the SM-HBST for signature generation and comparison. The control unit is already tested during the CPU test.

Some selected instructions are used to test status bits after arithmetic and logic operations. It is found from the extracted information that microcontroller families have three basic operations. They are word-oriented file register operations, literal and control operations, and bit-oriented file register operations. Some instructions in $I_{M\text{-}CPU,O}$ do the same function with different arguments. Only one form of these instructions is used. Therefore, thirteen instructions are used to test the full capabilities of the CPU (the PIC16F877 has not a multiplier). For example, the $I_{M\text{-}CPU,O}$ set has ADDWF and ADDLW instructions. Both instructions make an addition but the first instruction adds the working register to any other register and the second instruction adds literal to the working register (the working register is the accumulator in the microprocessors).

Reference signatures of the CPU test are taken by the SM-HBST through PORTD port, shown in Table VIII (Middle two columns of the table). Table X and Table XI compare between the HYBST strategy and the SBST strategy in terms of memory utilization and the total number of clock cycles for both PIC16F877 and PIC18F452 to finish the target test. The CPU test process is outlined in List 1.

From Table X and Table XI, the HYBST strategy in the CPU test achieves a significant amount of reduction in the memory utilization and the test application time. In the SBST strategy, the test application code in the flash memory is responsible for generating the test patterns as the TPG and compacting the test response using either emulated LFSR or emulated MISR as the TRC for signature generation. Either the emulated LFSR or the emulated MISR is a group of instructions that increases the size of the test application code, shown in Table X and Table XI. Every single shift of the binary states of either the emulated LFSR or the emulated MISR consumes large clock cycles. The MISR simultaneously compacts the test response of the selected module, and the LFSR individually compacts the test response of each output. Therefore, the TRC code as the MISR is executed 3328 times (thirteen instructions * 256), and the TRC code as the LFSR is executed 26624 times (thirteen instructions * 256 * 8). Therefore, the test application time in the case of the LFSR is greater than the test application time in the case of the MISR. In addition, the on-chip test application code collects the test responses and stores them in the data memory after being compacted into signatures using the TRC code. The usage of the data memory during the CPU test will delay the test process and hence the number of clock cycles is dramatically increased in the case of the SBST strategy.

Table X
Statistics of the CPU Test for PIC16F877

CPU test	Unit	HYBST	SBST with TRC using			
			MISR		LFSR	
RAM utilization	Byte	16 4.34%	40	10.86%	84	23.36%
Flash Memory utilization	Word	49 0.59%	2235	27.28%	2431	29.67%
Clock cycles	Clock cycle	20,500	41,645,103		76,081,267	

Table XI
Statistics of the CPU Test for PIC18F452

CPU test	Unit	HYBST	SBST with TRC using			
			MISR		LFSR	
RAM utilization	Byte	21 1.36%	47	3.05%	93	6.05%
Flash Memory utilization	Word	92 0.28%	3934	12.00%	4788	14.61%
Clock cycles	Clock cycle	25,576	42,365,535		82,430,191	

```
Extract information about CPU modules (ALU – SHU – Multiplier if
exist), then
for (each CPU module M_CPU)
{
    for (every operation Є O_M-CPU)
    {
        Determine I_M-CPU,O
        Select I Є I_M-CPU,O, using controllability and observability criteria
        Apply Exhaustive test patterns for all I_M-CPU,O
        Send test response to PORTD pins
        Acquire and compact test response using the SM-HBST
    }
}
Evaluate compacted test response using the SM-HBST.
```

Listing 1. CPU test process

In the HYBST strategy and during the CPU test, the instructions in $I_{M\text{-}CPU,O}$ use two operands (registers). One of these registers is the working register and the other register is the PORTD, connected to the SM-HBST. In GPIO test, the exhaustive test patterns are applied to the working register only and the result on any instruction is saved in the register of the PORTD. The result of every instruction in the CPU test is directly sent to the PORTD, connected to the SM-HBST for signature generation. The hardware-based TRC in the SM-HBST consumes only single clock cycle every single shift of the binary states, shown in Fig. 7(b) (section III). In addition, the number of memory access is reduced by using the SM-HBST and there is no need to access the data memory of the microcontroller during the execution of the hardware-based TRC to store the generated signatures. Therefore, the memory access that consumes large clock cycles is not required. For 8*8-multiplier test, the exhaustive test patterns are applied to the working register only and the register of the PORTD takes the same value. The result of the multiplication is sent to the PORTD. Therefore, the HYBST strategy that uses the hardware-based TRC in the SM-HBST consumes a small number of clock cycles compared to the software-based TRC of the SBST strategy during the CPU test.

C. USART test

The USART module is known as the *serial communication interface* (SCI). The USART can be configured as a full duplex asynchronous system that can communicate with peripheral devices such as personal computers. In addition, it can be configured as a half duplex synchronous system that can communicate with peripheral devices. The test subroutine of the USART test is designed and is then implemented to test the functionality of the USART module. First, it sets the baud rate of the USART module to 1200 bps. Then, the test patterns (0x00 – 0xFF – 0x33 – 0xCC – 0x0F – 0xF0) are sent to the transmitter (TX) of the USART module and loop it back again through MAX232 chip outside the microcontroller to receive it through the receiver (RX) of the USART module. These received test patterns are propagated to the PORTD. In addition, the signatures on each pin of the PORTD, a signature on TX pin, and a signature on RX pin are measured using the SM-HBST (RX pin and TX pin is multiplexed with the PORTC). Reference signatures, generated by the SM-HBST, are shown in Table XII, and the USART test process is outlined in List 2.

Table XII
Reference signatures of the USART

Ports	PIN	PIC16F877	PIC18F452
PORTD	0	8FE6ED	470BC1
	1	024B37	BD5481
	2	370115	70EC7A
	3	BAACCF	8AB33A
	4	28555F	75D341
	5	A5F885	8F8C01
	6	90B2A7	4234FA
	7	1D1F7D	B86BBA
PORTC	RX	731F53	8AABC8
	TX	731F53	8AABC8

```
Configure USART, then
Set baud rate to 1200 bps, Data to 0x00, and PORTD to 0
Loop
 {
      Send data through transmitter pin
      Check for received data from receiver pin
      If (received data = sent data) then
         Send received data to PORTD.
      Else
         Send received data to PORTD, set error, and exit loop
}
Change data and continue loop until test patterns are sent through
transmitter pin
Acquire and compact test response using the SM-HBST
Evaluate compacted test response using the SM-HBST
```

Listing 2. USART test process

Table XIII and Table XIV compare between the HYBST strategy and the SBST strategy in terms of memory utilization and the total number of clock cycles for both PIC16F877 and PIC18F452 to finish the USART testing. From Table XIII and Table XIV, the HYBST test strategy in the USART test achieves a significant amount of reduction in the memory utilization and the test application time.

Table XIII
Statistics of the USART Test for PIC16F877

USART test	Unit	HYBST	SBST with TRC using	
			MISR	LFSR
RAM utilization	Byte	23 6.25%	40 10.86%	89 24.18%
Flash Memory utilization	Word	213 2.60%	2292 27.97%	2528 30.85%
Clock cycles	Clock cycle	70,852	176,043	242,219

Table XIV
Statistics of the USART Test for PIC18F452

USART test	Unit	HYBST	SBST with TRC using	
			MISR	LFSR
RAM utilization	Byte	28 1.82%	45 2.92%	96 6.25%
Flash Memory utilization	Word	354 1.08%	4002 12.21%	4876 14.88%
Clock cycles	Clock cycle	67,416	164,095	232,715

D. Timer test

From *information extraction* phase, PIC microcontroller families have at least one basic timer module. It can be used as timers/counters. These timers have different sizes (8 bits or 16 bits) and different prescalers. This test subroutine is designed and implemented to functionally test the timers based on two different prescalers. For each timer, special function registers (SFRs) are configured for timer operation using the internal clock cycles. The initial value and the prescaler (1:1, 1:2 and 1:4) are set. The timer is started for counting and PORTB pins are set to HIGH state from LOW state. When the overflow of the timer is occurred, then PORTB pins are deactivated to LOW state.

During this test, the on-time is measured as a signature in the SS mode of the SM-HBST. This test subroutine, based on the HYBST strategy, cannot be implemented in the case of the SBST strategy because the timers must be externally tested through the GPIO pins. The timer test process is outlined in List 3. Reference signatures, generated by the SM-HBST in mode SS (mode 4 or mode 5), are shown in Table XV. Table XV illustrates the measured on-time pulse in µs range (mode 4) for both PIC16F877 (has three timers) and PIC18F452 (has four timers) and compares them with the expected pulse duration from the calculations based on the internal clock cycles of the corresponding microcontroller [6].

```
Configure Timer presale
Enable timer interrupt
Start timer
Set GPIO pin to high
Loop
{
   Watch timer interrupt to check if over flow or not
   If (timer over flow)
     Exit loop
}
Reset GPIO pin to low
Acquire on-time pulse from a GPIO pin using the SM-HBST

Repeat this process but using different prescalers and apply it to all timers
```

Listing 3. Timer test process

Table XVI shows the statistics of the timer test for the HYBST strategy in terms of memory utilization and the total number of clock cycles for both PIC16F877 and PIC18F452. Timer modules cannot be tested using the SBST strategy.

Table XV
Reference Signatures of the Timers and the CCP

Timer/ Prescale	PORT PIN / PIC	PIC16F877	Expected	PIC18F452	Expected
Timer test signatures					
TIMER 0/ (1:2)	PORTB 0	006930 µs	006895 µs	006906 µs	006895 µs
TIMER 0/ (1:4)	PORTB 1	013828 µs	013791 µs	013720 µs	013791 µs
TIMER 1/ (1:1)	PORTB 2	003506 µs	003447 µs	003520 µs	003447 µs
TIMER 1/ (1:2)	PORTB 3	006933 µs	006895 µs	006825 µs	006895 µs
TIMER 2/ (1:1)	PORTB 4	003466 µs	003447 µs	003479 µs	003447 µs
TIMER 2/ (1:4)	PORTB 5	013787 µs	013791 µs	013801 µs	013791 µs
TIMER 3/ (1:1)	PORTB 6			003519 µs	003447 µs
TIMER 3/ (1:2)	PORTB 7			006826 µs	006895 µs
CCP test signatures					
TIMER2	PWM1	E70FD2		9F5EB5	
TIMER2	PWM2	11C8AC		272632	
TIMER1	COMP	006873 µs	006895 µs	003446 µs	003447 µs
TIMER1	COMP	006873 µs	006895 µs	003446 µs	003447 µs

Table XVI
Statistics of the Timer Test for PIC16F877 and PIC18F452

Timer test	Unit	HYBST	
		PIC16F877	PIC18F452
RAM utilization	Byte	16 4.34%	23 1.49%
Flash Memory utilization	Word	98 1.19%	244 0.74%
Clock cycles	Clock cycle	14,680	17,796

E. Capture/Compare/PWM (CCP) test

Both microcontroller families contain two CCP modules, used together with the timers tested in timer test. The CCP modules are identical in operation, with the exception of the operation of the special event trigger. Different CCP modes

depend on timers in the microcontroller. Each CCP module can operate in the following modes:

- *Capture* mode: The CCP module captures the value of Timer1 when an external event occurs in CCPx pin.
- *Compare* mode: The register in the CCP module stores a number (16-bit), compared to the value in Timer1. The result of the comparison may generate an event that may include a change in the CCPx pin.
- *Pulse width modulation* (*PWM*) mode: The CCP module and Timer2 make up a PWM modulator whose output is located in CCPx pin.

The test subroutine of the CCP test is designed and implemented to functionally test CCP modules in *Compare* and *PWM* modes only, based on the HYBST strategy. CCP modules are not tested in all modes because timers were fully tested before in the timer test. First, CCP modules are configured to operate in the *PWM* mode where *PWM1* and *PWM2* are configured to work at frequency 5 kHz with 50% duty cycle. After that, CCP modules are configured to operate in the compare mode. Timer1 is started to count, and its value is then compared with CCP modules until it reaches these known values. Reference signatures of CCPs, based on the SM-HBST in both modes of operations, are taken from PORTC.CCP1 pin and PORTC.CCP2 pin, shown in Table XV. The CCP module test process is outlined in List 4.

Table XVII shows the statistics of the CCP test for the HYBST strategy in terms of memory utilization and the total number of clock cycles for both PIC16F877 and PIC18F452. The CCP module cannot be tested using the SBST strategy.

```
Configure CCPx registers to work in compare mode
Initialize the value of timer1 and enable interrupt
Start timer
Set PORTC.CCPX to HIGH
Loop
 { Watch timer1 until reaching compare value
      If (timer1 = compare value)
                Exit loop  }
Reset PORTC.CCPX to LOW
Evaluate CCPx pin output using the SM-HBST
Repeat this process for CCPx
Configure CCPx registers to work in the PWM mode
Initialize PWMx duty cycle to 50% of 5 KHz clock
Start PWMx
      Watch PWMx output using the SM-HBST
Stop PWMx
```

Listing 4. CCP module test process.

TABLE XVII
STATISTICS OF THE CCP TEST FOR PIC16F877 AND PIC18F452

CCP test	Unit	HYBST	
		PIC16F877	PIC18F452
RAM utilization	Byte	20 5.43%	25 1.62%
Flash Memory utilization	Word	356 4.34%	624 1.90%
Clock cycles for PWM	Clock cycle	8,828	6,776
Clock cycles for COMPARE	Clock cycle	52,292	52,264

F. Memory Test

Microcontrollers have three main memory organization; the flash memory (program memory), the EEPROM and the data memory. Each memory block has its own bus as in Harvard architecture [6], so that access to each block can occur during the same clock cycle. The data memory can further be broken down into the general-purpose RAM and Special Function Registers (SFRs). The SFRs are used to control the peripheral modules found in the microcontroller. The RAM are used to store data that microcontroller needs during its normal operation. This RAM can be divided into smaller banks, also.

1. *Flash Memory Test*: The Flash memory is an important module in a microcontroller chip, because it stores the application program and the test program. Microcontroller modules are going to be tested after the application program and the test program are correctly downloaded. This test is divided into two steps. In step 1, run a C++ program, written on Visual Studio 2010 package, on a personal computer. This program reads the hexadecimal (*Hex*) file words of the application program and the test program, generated from the *mikroC* compiler. Then, the *Hex* file is compacted based on the MISR with primitive polynomial $x^8 + x^6 + x^5 + x^4 + 1$, for the reference signature generation [1], [6]. The reference signature will be stored in the last location in the EEPROM. In step 2, the CPU of the microcontroller will read the data word of the flash memory and the data word is compacted using the same MISR. After that, the generated measured signature will be compared with the reference one, stored in the EEPROM. If both signatures are the same, then the application program and the test program is successfully downloaded and the flash memory is successfully tested. This test subroutine is designed and is then implemented for both HYBST strategy and SBST test strategy.

2. *RAM Test*: J. V. De-Goor and Z. Al-Ars introduced many functional fault models (FFMs) for memories like static faults and dynamic faults [35]-[36]. Based on divide-and-conquer strategy, the RAM module is divided into smaller banks and each bank is individually tested. In the case of the PIC16F877, the RAM can be divided into four smaller bank and twelve banks for the PIC18F452. Then, each bank is individually tested using March test algorithms [37] because of their simplicity and linearity with the memory size. The March test can be defined as a sequence of March elements, where a March element is a sequence of memory operations sequentially performed on all memory cells. In a March element, the way from one cell to the next one is specified by the address order. For some March elements, the address order can be chosen as increasing or decreasing. In a March element, it is possible to perform a write 0 (W0), a write one (W1), a read zero (R0) and a read one (R1). The zero and one after read operations represent the expected values of the read on the output. An example of a March element is ↑ (R0; W1), where all memory cells are accessed in an increasing address order while performing R0 then W1 on each cell, before continuing to the next cell. By arranging a number of March elements one after the other, a March test is constructed.

The RAM test is designed and implemented based on March AB algorithm. March AB {↕(W0); ↑(R0;W1;R1;W1;

R1); ↑(R1;W0;R0;W0;R0); ↓(R0;W1;R1;W1;R1); ↓(R1;W0;R0;W0;R0); ↕(R0)} was introduced by S. Carlo, A. Bosio, G. Natale, and P. Prinetto [37]. Their March test targets realistic memory static linked faults and dynamic unlinked faults in SRAMs and has a test length with a complexity of 22*n*. Here the test subroutine, based on March test AB, is constructed. (In addition, it is possible to extend this test subroutine to any March test [38].) The test response from the RAM is propagated through the PORTC (GPIO pins) to the SM-HBST for signature generation.

Table XVIII contains reference signatures of the RAM test using March AB, generated by the SM-HBST. The data bus of each RAM bank is propagated to PORTC. The data bus is 8-bit with eight same signatures on each pin of PORTC. For simplicity, only single signature will be presented for each RAM bank.

Table XVIII
RAM test Signatures Based on March AB

Module	RAM Bank	PIC 16F87X	PIC 18F4X2	RAM Bank	PIC 18F4X2
RAM	1	0438F8	EFF5D9	7	08E472
	2	B300AE	511ECC	8	B2691B
	3	CFB46B	A83A68	9	C3162B
	4	379AAD	BA8630	10	A5A126
	5		A33AFC	11	DFB602
	6		9EC7E8	12	93B255

Table XIX and Table XX compare between the HYBST strategy and the SBST strategy in terms of memory utilization and the total number of clock cycles for both PIC16F877 (368 byte divided into 4 parts) and PIC18F452 (1536 byte divided into 12 parts) to finish RAM test using March AB. From Table XIX and Table XX, the HYBST strategy in the RAM test using March AB achieves the reduction in memory utilization and the test application time except in the RAM utilization in Table XX.

Table XIX
Statistics of the RAM Test Using March AB for PIC16F877

RAM test	Unit	HYBST		SBST with TRC using MISR		SBST with TRC using LFSR	
RAM utilization	Byte	16	4.34%	16	4.34%	16	4.34%
Flash Memory utilization	Word	200	2.44%	336	4.10%	336	4.10%
Clock cycles	Clock cycle	279,668		531,399		532,039	

Table XX
Statistics of the RAM Test Using March AB for PIC18F452

RAM test	Unit	HYBST		SBST with TRC using MISR		SBST with TRC using LFSR	
RAM utilization	Byte	23	1.49%	21	1.36%	21	1.36%
Flash Memory utilization	Word	302	0.92%	528	1.61%	528	1.61%
Clock cycles	Clock cycle	1,221,368		2,071,891		2,071,891	

3. *EEPROM Test:* The EEPROM is read and is written during normal operation. This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the SFRs. There are four SFRs used to read and to write this memory. These registers are EECON1, EECON2 (not a physically implemented register), EEDATA and EEADR. User program can use the EEPROM to store the important data during the application run and to read it again after the end of the application. First, the test subroutine reads the data from EEPROM locations. Then, the test subroutine stores the data into a temporary location before testing this module.

Since the large delay (20 *ms*) is required between the written data cycle of the EEPROM and the read data cycle of the EEPROM, therefore the required number of clock cycles is large to deal with the SM-HBST. Therefore, the EEPROM test subroutine was implemented based on a simple marsh algorithm with low time complexity. It is the modified algorithmic test sequence (MATS) algorithm that detects all combination of stuck-at faults (SAF) in RAMs and has a test length with a complexity of 4*n* [39]-[40]. MATS test sequence is {↑(W0); ↑(R0,W1); ↑(R1)} where the EEPROM is internally tested and the data results are sent for validation.

The measured signature in the HYBST strategy is calculated inside the microcontroller like the SBST strategy. Therefore, from Table XXI and Table XXII, there is no improvement in the memory utilization and no reduction in the total test application time for both PIC16F877 and PIC18F452 to finish the EEPROM test.

Table IV XXI
Statistics of the EEPROM Test using MATS for PIC16F877

EEPROM test	Unit	HYBST		SBST with TRC using MISR		SBST with TRC using LFSR	
RAM utilization	Byte	22	5.97%	22	5.97%	22	5.97%
Flash Memory utilization	Word	190	2.32%	190	2.32%	190	2.32%
Clock cycles	Clock cycle	15,493,952		15,493,951		15,493,951	

Table XXII
Statistics of the EEPROM Test using MATS for PIC18F452

EEPROM test	Unit	HYBST		SBST with TRC using MISR		SBST with TRC using LFSR	
RAM utilization	Byte	27	1.75%	27	1.75%	27	1.75%
Flash Memory utilization	Word	316	0.96%	316	0.96%	316	0.96%
Clock cycles	Clock cycle	15,445,035		15,445,035		15,445,035	

G. Comparisons between the HYBST and the SBST

Test subroutines were individually investigated for testing all microcontroller modules in the previous sections. In this section, all test subroutines are merged together in one complete test program. The effectiveness of the complete test program using the HYBST strategy and the SBST strategy will be evaluated on two Microchip® microcontrollers (PIC16F877A and PIC18F452). Table XXIII and Table XXIV show the comparison of the complete test program between the HYBST strategy and the SBST strategy, based on the emulated LFSR and the emulated MISR as the TRC. These tables present the statistics of the complete test program such as the memory utilization (data memory, and flash memory), the test application time (the number of clock cycles taken to finish the complete test), and the testability of microcontroller modules (the number of tested modules in a microcontroller).

Table XXIII
Statistics of the Complete Test Program for PIC18F452

Microchip® PIC18F452	Unit	HYBST		SBST with TRC using			
				MISR		LFSR	
RAM utilization	Byte	30	1.95%	47	3.06%	94	6.12%
Flash Memory utilization	Word	2326	7.09%	5592	17.06%	6682	20.4%
Clock cycles	Clock cycle	21,112,792		70,023,259		112,101,595	
Tested Modules		All Passed		Timers, GPIO and CCP Failed			

Table XXIV
Statistics of the complete test program for PIC16F877

Microchip® PIC16F877	Unit	HYBST		SBST with TRC using			
				MISR		LFSR	
RAM utilization	Byte	27	7.33%	44	11.95%	93	25.27%
Flash Memory utilization	Word	1663	20.3%	3568	43.55%	3897	47.57%
Clock cycles	Clock cycle	25,600,168		78,348,171		114,734,099	
Tested Modules		All Passed		Timers, GPIO and CCP Failed			

Performance enhancement of the HYBST strategy is shown in Table XXV. The comparisons between the HYBST strategy and the SBST strategy based on the emulated LFSR and the emulated MISR as the TRC present the superiority of the presented HYBST strategy over the SBST strategy. It achieves a significant amount of reduction in the memory utilization and the test application time. Besides, the fault coverage of the HYBST strategy is greater than the other SBST strategies.

Table XXV
Performance Enhancement Based on the HYBST Test Strategy

Microcontroller	PIC 18F452		PIC 16F877	
	SBST with TRC using		SBST with TRC using	
	LFSR	MISR	LFSR	MISR
RAM reduction	68.08%	36.17%	70.96%	38.63%
Flash memory reduction	65.19%	58.40%	57.32%	53.40%
Clock cycle reduction	81.16%	69.84%	77.68%	67.32%

From Table XXV, the superiority of the HYBST strategy in the memory utilization is achieved due to the reduction of the RAM utilization by 70.96% and 38.63% for PIC16F877 and by 68.08% and 36.17% for PIC18F452. In addition, the HYBST strategy reduces flash memory utilization by 57.32% and 53.40% for PIC16F877 and by 65.19% and 58.40% for PIC18F452. The superiority of the HYBST strategy in the total number of clock cycles is achieved due to the reduction of the test application time by 77.68% and 67.32% for PIC16F877 and by 81.16% and 69.84% for PIC18F452.

From Table XXIII, Table XXIV, and Table XXV, the complete test program in the PIC18F452 utilizes larger memory space than in the PIC16F877 because the PIC18F452 has more features than the PIC16F877 especially in timers and the multiplier that needs more effort to test them. Since the PIC18F452 achieves from 10-15 MIPS, and the PIC16F877 operates in 5 MIPS [6], [31], therefore the complete test program of the PIC18F452 consumes lower test application time because of its higher performance rate. In addition, the HYBST strategy can test all modules and the SBST strategy cannot test timers, GPIO pins, and CCP modules because the SBST strategy cannot properly test GPIO pins of the microcontroller without using the SM-HBST strategy.

In the next section, the integrated test strategy of the microcontroller testing on the printed circuit board (PCB) for fault diagnosis indicates a real practical test strategy.

V. Fault Diagnosis of the Circuit Board Including Microcontroller Chip

Fault diagnosis of the CUT board including a microcontroller chip for correct operation is an important issue. It is required to apply the proper test patterns to the inputs of the CUT board and to analyze the test response for fault diagnosis. During the fault diagnosis, the faulty source components are located so that the CUT board is returned back to the service. The testing of a microcontroller chip in the board level requires integrating test strategies that test random logic integrated circuits (ICs) based on the SM-HBST strategy and test a microcontroller chip based on the HYBST strategy. The following integrated test strategy consists of two main phases; the *CUT preparation and preprocessing* phase and the *testing and fault diagnosis* phase.

A. CUT preparation and preprocessing phase

In this phase, the schematic diagram of the CUT should be defined. To clarify the idea of this phase, a simple CUT board is selected, shown in Fig. 12. It consists of three main parts. The first part is random logic part that consists of one decoder (74LS138 - U7), and two 4-Bit magnitude comparators (74LS85 - U3, U5). The second part is the microcontroller part that consists of the microcontroller chip (PIC16F877 or PIC18F452), and the integrated circuit (MAX232 - U8). Both the application program used in the normal mode and the test program used in the test mode are loaded to the microcontroller. The third part is the design for testability (DFT) part that enables the CUT board to operate in two operation modes; normal mode and test mode. The DFT part has three multiplexer ICs (74LS157 - U4, U6, U9) that partition the microcontroller part from the random logic part in the test mode. The DFT part enables the testing of each part in the CUT board with its own test strategy to reduce the testing difficulty, and to assist the fault isolation. In the normal mode, the CUT board does its normal operation according to industrial applications.

The CUT board layout is generated from the circuit layout tool (ORCAD layout), shown in Fig. 13. The *layout netlist file* that defines a component list and a complete description of the connectivity nets between the components on the PCB is generated. From the *layout netlist file*, different related files are generated. These files will be very useful in the next phase to locate the faulty source components. The *Node file* is constructed from the *layout netlist file*. It holds node number, node name such as *U04P04-74LS157* (it means IC number in

the schematic diagram U04, pin number in the IC 04, and IC name 74LS157), node type (input node or output node), and the status of the node test. The *Dependency file* is also constructed, and holds output nodes such as *U04P04-74LS157* and input nodes affect this output node in the same IC {*U04P01-74LS157*, *U04P02-74LS157*, *U04P03-74LS157*, *U04P015-74LS157*}. After constructing dependency file, the *connectivity file* will be created from the *layout Netlist file*. It holds the output nodes, connected to input nodes of other ICs. It is like the output node *U04P04-74LS157*, connected to the input node *U05P01-74LS85*. These files are related to each other. When the output node, *U04P04-74LS157*, in the node file is chosen, the related information to this node appears in the dependency file and in the connectivity file.

This phase ends by capturing reference signatures for all nodes of the golden CUT board with the aid of the SM-HBST strategy. The capturing reference signatures can be achieved for the random logic part and DFT part according to section III, and then the microcontroller part according to section IV. This phase is executed only once for every new CUT board.

B. Test and fault diagnosis phase

This test phase achieves the testing of the CUT board in two different directions. First direction is to test random logic part and the DFT part. The SM-HBST generates required test pattern signals, propagated through these ICs, and then it detects the stream binary data, generated from a target node on the CUT board by the test probe. The measured signature of that node, based on the test strategy in section III, is generated. The other direction is to test the microcontroller part. The SM-HBST generates required test signals to select the test routines of the target microcontroller module. The stream binary data, generated from a target node on the microcontroller part, is also captured by the SM-HBST to generate the measured signature of that node, based on test strategy in section IV.

After the measured signatures of every node in the CUT board are generated, they are automatically compared with the corresponding reference signatures, captured using the previous phase. If the measured signature of a node is equal to a corresponding reference one, the test status flag of that node is set true (good node), and if this signature is not equal to a corresponding reference one, the test status flag of that node is set false (bad node).

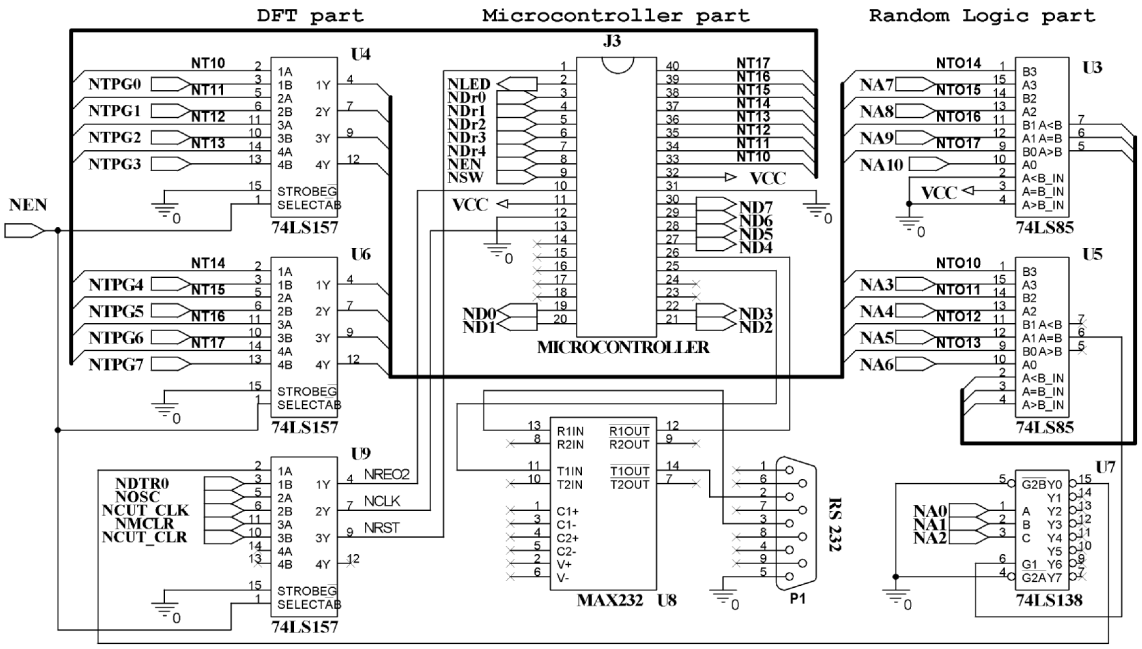
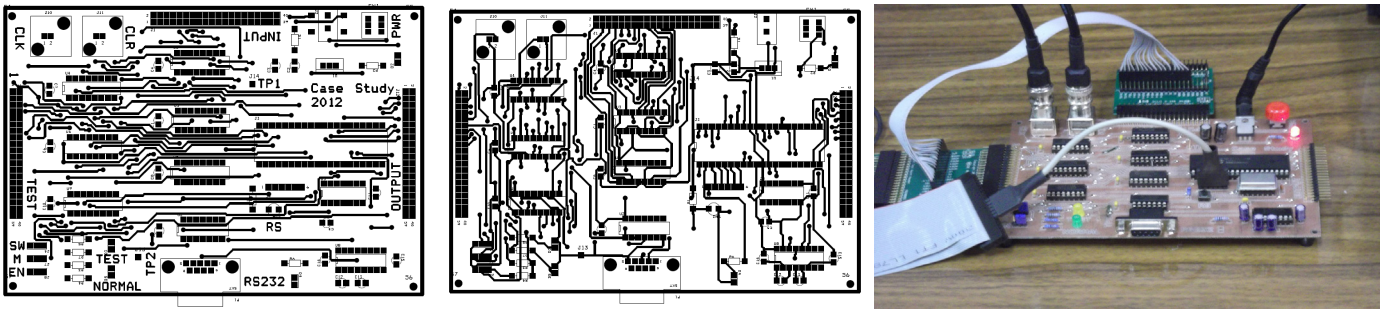


Fig. 12. Schematic diagram of the CUT.



(a) The CUT layout fornt plane. (b) The CUT layout back plane. (c) The printed circuit board of the CUT.

Fig. 13. The CUT board.

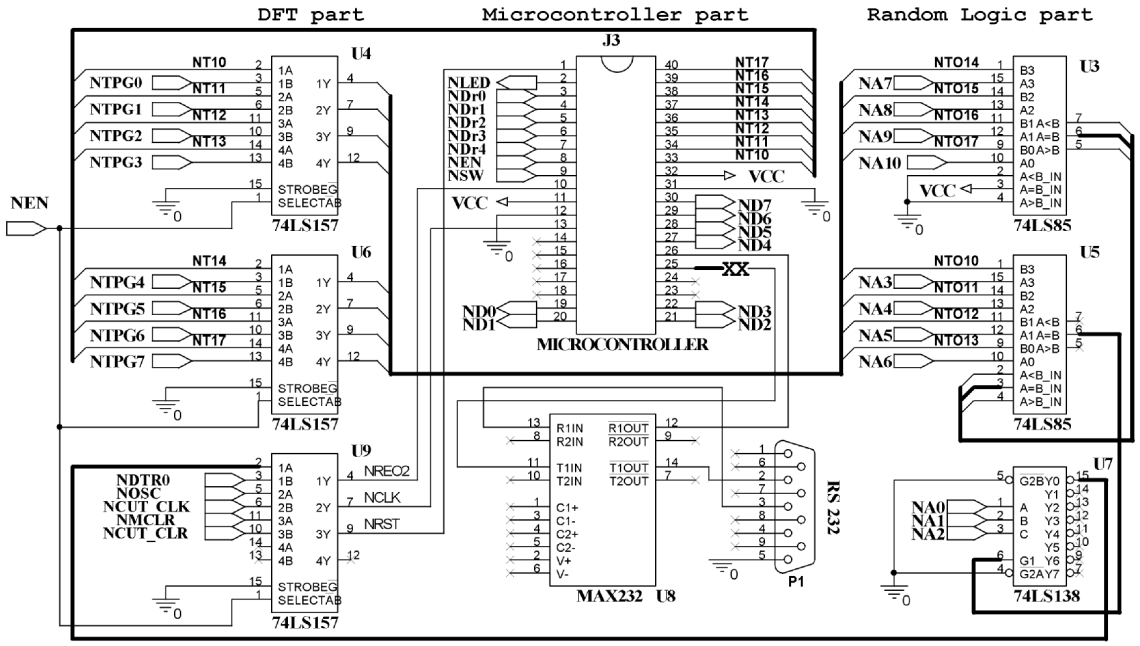


Fig. 14. Schematic diagram of the faulty CUT propagation.

When the fault is applied to the pin U03P06-74LS85 in the random logic part, it propagates from the source faulty node (pin) to the multiplexer U9 pin 2 (U09P02). In the test mode, this fault cannot propagate to the microcontroller part (input PORTE), shown in Fig. 14. The node U09P02 is considered the output of the random logic part in the test mode. The SM-HBST generates required test patterns in the test mode 0, and the measured signatures of every node in the random logic part are captured. All output nodes that have *false* test status are stored in a temporary file as bad nodes. If this file has no bad nodes, then this CUT board is fault-free, and if this file has at least one bad node, then this CUT board is faulty. The bad nodes of the CUT board shown in Fig. 14 are shown in Table XXVI with the shadow rows. They are {*U03P06*, *U05P05*, *U05P06*, *U05P07*, *U07P07*, *U07P08*, *U07P09*, *U07P10*, *U07P11*, *U07P12*, *U07P13*, *U07P14*, *U07P15*}.

The dependency file and connectivity file, generated from the previous phase, are utilized to track each bad node in the temporary file to get the source faulty node (nodes). For example, the bad node U07P15-74LS138 in the temporary file has the dependency set, DU07P15 {U07P01, U07P02, U07P03, U07P04, U07P05, U07P06}. If the node U07P06-74LS138 that belongs to DU07P15 is connected to the node U05P06-74LS85 in the temporary file, skip the node U07P15-74LS138 and another bad node in the temporary file is tracked. This search processes until the source faulty node U03P06-74LS85 is determined. This node has the dependency set, DU03P06 {U03P01, U03P02, U03P03, U03P04, U03P09, U03P10, U03P11, U03P12, U03P13, U03P14, U03P15}. All nodes in the DU03P06 have no connection with any bad node. Therefore, the node U03P06-74LS85 is selected as the source faulty node. If the measured signature of the source faulty node is varying from test cycle to another test cycle (flashing), and the measured signature of any node in the temporary file is flashing, a short circuit (bridging fault) among the nodes in the temporary file may be occurred.

TABLE XXVI
REFERENCE AND MEASURED SIGNATURES OF TESTED NODES OF THE RANDOM LOGIC PART

No.	Node Name	Reference (Good) signature		Measured signature		Status
226	U03P05-74LS85	B0B300	0 - 0	B0B300	0 - 0	True
227	U03P06-74LS85	25FA0A	0 - 0	299BD5	0 - 0	False
228	U03P07-74LS85	BCD2DF	0 - 0	BCD2DF	0 - 0	True
241	U04P04-74LS157	82775E	0 - 0	82775E	0 - 0	True
244	U04P07-74LS157	413BAF	0 - 0	413BAF	0 - 0	True
246	U04P09-74LS157	A09DD7	0 - 0	A09DD7	0 - 0	True
249	U04P12-74LS157	D04EEB	0 - 0	D04EEB	0 - 0	True
251	U05P05-74LS85	8044B1	0 - 0	0B3009	0 - 0	False
252	U05P06-74LS85	4D5644	0 - 0	EF8624	0 - 0	False
253	U05P07-74LS85	E48920	0 - 0	CD2DF8	0 - 0	False
273	U06P04-74LS157	682775	0 - 0	682775	0 - 0	True
276	U06P07-74LS157	B413BA	0 - 0	B413BA	0 - 0	True
278	U06P09-74LS157	DA09DD	0 - 0	DA09DD	0 - 0	True
281	U06P12-74LS157	ED04EE	0 - 0	ED04EE	0 - 0	True
292	U07P07-74LS138	680659	0 - 0	3E6B17	0 - 0	False
294	U07P09-74LS138	5147C1	0 - 0	69A611	0 - 0	False
295	U07P10-74LS138	D1F135	0 - 0	5385D7	0 - 0	False
296	U07P11-74LS138	1F0722	0 - 0	CB4EF9	0 - 0	False
297	U07P12-74LS138	A1990C	0 - 0	6A5924	0 - 0	False
298	U07P13-74LS138	8A29C0	0 - 0	9B24BD	0 - 0	False
299	U07P14-74LS138	A29B21	0 - 0	D29304	0 - 0	False
300	U07P15-74LS138	33CA26	0 - 0	036E91	0 - 0	False
321	U09P04-74LS157	299BD5	0 - 0	299BD5	0 - 0	True
324	U09P07-74LS157	000000	0 - 0	000000	0 - 0	True
326	U09P09-74LS157	299BD5	0 - 0	299BD5	0 - 0	True
329	U09P12-74LS157	299BD5	0 - 0	299BD5	0 - 0	True

VI. Experimental results

This section presents the complete application of this hybrid test strategy, applied to the CUT board in Fig. 14. In the normal mode, the main input signals (*NA0* to *NA10*), the master clear (*NMCLR*), and the main clock oscillator (*NOSC*) are propagated through the random logic part and the microcontroller part. The presented hybrid test strategy does not depend on the embedded application of the CUT board. It is applicable for any CUT board including a microcontroller chip whatever its industrial applications are.

In previous section, the fault was applied to the pin U03P06-74LS85 in the random logic part. The reference (good) signatures and the corresponding measured signatures of the CUT board were captured and then stored in the database according to test mode 0. In this section, the other fault is applied to the input pin J03P26-RX-PIC18F452 in the microcontroller part.

To properly test the CUT board, it is required to go through various modes and to connect the SM-HBST with the CUT board. First, it is required to know some control signals for the operation modes of the CUT board. The control input signal, *NEN*, is connected to all multiplexers in the DFT part. It allows the switch between the normal mode and the test mode. These multiplexers can switch between main inputs of the CUT board in the normal mode and the required test signals, generated from the SM-HBST in the test mode. Multiplexers (U4 and U6) switch the output port PORTB (pin 33 to pin 40) of the microcontroller and the test pattern inputs (*NTPG0* to *NTPG7*), generated from the SM-HBST (*GTPG*(7:0)). The signal input, *NSW*, enables the microcontroller operation in the normal mode. Multiplexer U9 switches between the output signal generated from the output of decoder U7 and the input signal *NTDR0* that enables the microcontroller part in the test mode. In addition, multiplexer U9 switches between the master clear (*NMCLR*) of the CUT, and the test clear (*NCUT_CLR*), generated from the SM-HBST (*CUT_CLR*). It also switches between the clock oscillator (*NOSC*) of the CUT board, and the test clock (*NCUT_CLK*), generated from the SM-HBST (*GCUT_CLK*).

Signal *NEN, NSW*, and signal *NTDR0* are connected to the port PORTE (pin 8 to pin 10) of the microcontroller as an input port. These signals, shown in Table XXVII, partition the CUT into two main parts (the random logic part and the microcontroller part) in the test mode. The inputs of the random logic part (*NTPG0* to *NTPG7*, and *NA0* to *NA10*) are connected to test signals, generated from the SM-HBST (*GTPG*(18:0)). The SM-HBST generates the required test patterns and the measured signatures of target nodes according to test mode 0, explained in section III. In the microcontroller part, the microcontroller receives an input selection (*NDr0* to *NDR4*) from port PORTA (pin 3 to pin 7) as an input port. This input selection is stimulated from the SM-HBST as the deterministic test patterns (*GTPG*(42:47)) according to test mode 3 shown in Table V. These deterministic test patterns are used to select the proper microcontroller module for testing. Other microcontroller ports are set to be output ports (PORTB, PORTC, and PORTD) to propagate the test response to the SM-HBST for signature generation.

Table XXVII
Control signals for modes of the CUT operation

Control signals			Operation
NEN	*NSW*	*NTDR0*	
0	0	X	Disable the microcontroller operation in the normal mode.
0	1	X	Enable the microcontroller operation in the normal mode.
1	X	1	Enable switching of the multiplexers in test mode and enable the testing of the microcontroller part.
1	X	0	Enable switching of the multiplexers in test mode and disable the testing of the microcontroller part.

The applied fault to the pin J03P26-RX-PIC18F452 in the microcontroller part is examined. The fault is the open-circuit in the output track on the CUT board between pin J03P26-RX-PIC18F452 and pin U08P11-MAX232. It affects the *USART Receive* part of the serial port connection. This leads to a number of bad nodes in the serial port of the microcontroller part. The USART test routine, presented in section IV, sends test patterns to the USART transmitter pin J03P25-TX-PIC18F452 and loops it back again through MAX232 chip to receive it from USART receiver pin J03P26-RX-PIC18F452 (a short circuit through RS232).

Based on the CUT board shown in Fig. 14, Table XXVI shows some tested nodes that include the reference and the measured signatures of the random logic part, and Table XXVIII shows some tested nodes that include the reference and the measured signatures of the microcontroller part. Every tested node in Table XXVI has a single reference signature, a single measured signature and a single test status. However, in Table XXVIII, some external tested nodes of the microcontroller have multiple reference signatures, multiple measured signatures, and different test status according to the testing of the selected module of the microcontroller.

Table XXVIII
Reference and measured signatures of tested nodes of the microcontroller part

No.	Node Name	Reference Signature		Measured Signature		Status
73	J03P19-RD0-PIC18F452	98A6B8	PORTS	98A6B8	PORTS	True
74	J03P20-RD1-PIC18F452	30B502	PORTS	30B502	PORTS	True
75	J03P21-RD2-PIC18F452	C40F5E	PORTS	C40F5E	PORTS	True
76	J03P22-RD3-PIC18F452	8077CC	PORTS	8077CC	PORTS	True
81	J03P27-RD4-PIC18F452	A0DC17	PORTS	A0DC17	PORTS	True
82	J03P28-RD5-PIC18F452	9AD2DA	PORTS	9AD2DA	PORTS	True
83	J03P29-RD6-PIC18F452	CB508C	PORTS	CB508C	PORTS	True
84	J03P30-RD7-PIC18F452	7F1705	PORTS	7F1705	PORTS	True
95	J03P19-RD0-PIC18F452	3C2EAD	CPU	3C2EAD	CPU	True
96	J03P20-RD1-PIC18F452	F2C053	CPU	F2C053	CPU	True
97	J03P21-RD2-PIC18F452	86F82A	CPU	86F82A	CPU	True
98	J03P22-RD3-PIC18F452	9AA92E	CPU	9AA92E	CPU	True
99	J03P27-RD4-PIC18F452	4BDB14	CPU	4BDB14	CPU	True
100	J03P28-RD5-PIC18F452	243FD2	CPU	243FD2	CPU	True
101	J03P29-RD6-PIC18F452	8EF7CD	CPU	8EF7CD	CPU	True
102	J03P30-RD7-PIC18F452	EB5A81	CPU	EB5A81	CPU	True
103	J03P19-RD0-PIC18F452	470BC1	USART	00F4BF	USART	False
104	J03P20-RD1-PIC18F452	BD5481	USART	00F4BF	USART	False
105	J03P21-RD2-PIC18F452	70EC7A	USART	00F4BF	USART	False
106	J03P22-RD3-PIC18F452	8AB33A	USART	00F4BF	USART	False
107	J03P27-RD4-PIC18F452	75D341	USART	00F4BF	USART	False
108	J03P28-RD5-PIC18F452	8F8C01	USART	00F4BF	USART	False
109	J03P29-RD6-PIC18F452	4234FA	USART	00F4BF	USART	False
110	J03P30-RD7-PIC18F452	B86BBA	USART	00F4BF	USART	False
111	J03P25-TX-PIC18F452	8AABC8	USART	8AABC8	USART	True
112	J03P26-RX-PIC18F452	8AABC8	USART	299BD5	USART	False

In Table XXVIII, nodes 73 to 76 and nodes 81 to 84, generated from PORTD with PORTS status, test the GPIO module. Nodes 95 to 102, generated from PORTD with CPU status, test the CPU module, and nodes 103 to 110, generated from the PORTD with USART status, test the USART module. Shaded rows in Table XXVI and Table XXVIII show bad nodes, resulted from the target fault in the microcontroller part besides the applied fault in the random logic part.

Since the USART transmitter generates proper test patterns from node J03P25-TX-PIC18F452 according to the USART test, therefore the measured signature (8AABC8) is similar to the reference signature (8AABC8). Due to the open-circuit between pin J03P25-TX-PIC18F452 and pin U08P11-MAX232, the measured signature of pin U08P11-MAX232 (299BD5) is different from the reference signature (8AABC8). These patterns return back again through MAX232 chip from node U08P12-MAX232 and the microcontroller receives them from USART receiver pin J03P26-RX-PIC18F452. Therefore, the measured signature of pin J03P26-RX-PIC18F452 (299BD5) will be different from the reference signature (8AABC8). The test status of node J03P25-TX-PIC18F452 is a good node, but the test status of node J03P26-RX-PIC18F452 is a bad node. In addition, nodes 103 to 110, generated from PORTD, are bad nodes in the USART test. However, the nodes generated from PORTD in the GPIO test and the CPU test, are good nodes. Therefore, the source faulty node of the microcontroller part is node J03P26-RX-PIC18F452 of the USART module in the microcontroller.

Discussion: In this paper, three main test strategies are discussed. The first one is the HBST strategy. All testing system will be outside the CUT board on the external ATE. It costs large hardware overhead and large test application time to stimulate the target fault in the CUT board, besides small DFT circuitry is used to increase the controllability and observability of the CUT board. Increasing the controllability and observability of the CUT board assists the external ATE to properly apply the TPG and to acquire the test response. The CUT board including a microcontroller chip is a heterogeneous system with poor accessibility, so its embedded modules need large application time to properly apply test patterns. Therefore, the SBST strategy is considered the second test strategy to resolve the test cost of the HBST. The SBST strategy is mainly used to test large microprocessors.

In the SBST strategy, the testing system including the TPG, TRC, test controller, and testing evaluation will be emulated using the software code inside the memory of the microprocessor system. The cost of the testing system is based on the hardware utilization, test application time, and the fault coverage. This microprocessor system has large memory, and the usage of the testing system inside this large memory does not utilize much space in it. Therefore, the SBST is an efficient test strategy for large microprocessors. However, when the SBST strategy is applied to the microcontroller with limited memory space, the cost of the hardware utilization is increased. No authors proposed solution for this issue. The authors in this paper propose a new hybrid test strategy to solve this issue, called the HYBST.

The cost of the testing system based on the HYBST strategy is composed of three parts. The first part is the SM-HBST design based on the FPGA implementation whereas the total gate equivalent of the presented design on the FPGA is 34,373 gate equivalent (equals 137,492 transistors) where the gate equivalent unit is 2-input NAND gate that equals four transistors. The second part is the used ICs in the DFT on the CUT board, and the third part is the hardware utilization in the microcontroller. The HYBST strategy is used to test the CUT board including the microcontroller chip. It is required to make a comparison between the number of transistors used in the testing system and the CUT. This discussion can be concluded by what the expected number of transistors in the microcontroller is.

From Table I and for the PIC18F452, the data memory (SRAM) used is 1536 byte (1536 x 8 = 12288 bits). Every bit of the SRAM cell needs six transistors. This leads to 73,728 transistors in the 12288 bits of the data memory. The excepted number of transistors in the periphery circuitry is around 2,224 transistors according the memory design steps in [41]. Therefore, the total required transistors in the data RAM of the PIC18F452 microcontroller is around 76,000 transistors. The Flash memory that has 16 kword (word = 14 bits) is around 267,376 transistors [41]. The used EEPROM memory has 256 byte. It is around 2,648 transistors [41]. Therefore, the total transistors in these three modules, only in the microcontroller chip, are 346,024 transistors. From this estimation of the expected number of transistors in the data memory (SRAM), the flash memory, and the EEPROM memory, it exceeds the total transistors in the FPGA implementation. If all microcontroller modules are considered, the expected number of transistors in the microcontroller will be greater than the CUT board.

The HYBST strategy is proposed to solve the testing cost of the HBST strategy and the SBST strategy in the hardware overhead, test application time and the fault coverage. If the test cost of the HYBST strategy is compared to the test cost of the SBST strategy for testing the microcontroller with small internal memory, the memory utilization and test application time are reduced besides increasing in the fault coverage. Adding FPGA circuit board increases the hardware overhead in the case of the HYBST strategy. However, the hardware overhead in the case of the SBST strategy is the memory utilization only. If the test cost of the HYBST is compared to the test cost of the HBST strategy for testing the microcontroller with poor accessibility, the hardware overhead is nearly the same but the test application time is reduced besides increasing in the fault coverage.

The presented test strategy in this paper has some limitations. The maximum frequency of the three-phase clocks (GCLK_TPG, GCLK_CUT, and GCLK_SIG) from Table IV is 4.17 MHz. Whereas, the maximum frequency of most microcontrollers is greater than 4 MHz, therefore, the proposed test strategy is not suitable for at-speed testing. In addition, and due to the small numbers of input modules in the microcontroller, the exhaustive testing is used to detect all combinational faults, detected by single-pattern test generators without fault simulator [1], [13]. Therefore, the proposed test strategy is not suitable for the detection of the delay fault, detected by two-pattern test

generators without fault simulator [12]. It is required to expand the following proposal to the two-pattern test generators, presented in [12]. This extension will increase the required hardware overhead in the memory utilization and will increase the required number of the clock cycles.

Finally, in the EEPROM test, the large delay (20 ms) between the written data cycle and the read data cycle increases the required number of clock cycles to deal with the SM-HBST, shown in Table XX and Table XXI. Therefore, the EEPROM test subroutine was implemented based on a simple marsh algorithm with low time complexity and low fault coverage. From Table XX and Table XXI, there is no improvement in the memory utilization and no reduction in the total test application time for both PIC16F87X and PIC18F4X2.

VII. Conclusion

The HBST strategy is limited to test complex digital circuits such as microcontrollers that have heterogeneous components with poor accessibility. In addition, the SBST strategy is efficient in the case of complex embedded processors. However, for microcontrollers with small internal memories, the SBST is limited in the memory utilization, and cannot test all its internal modules and its GPIO pins without the external ATE.

In this paper, the integrated test strategy solution of the CUT board including a microcontroller chip with small internal memories for fault diagnosis was presented. It targets both conventional random logic ICs and a microcontroller chip on the CUT board. Conventional random logic ICs is tested based on the SM-HBST strategy. Every pin (node) in the random logic ICs is stimulated by the TPG of the SM-HBST, and the test response from a tested pin (node) is compacted for signature generation. Measured signatures are generated according to different test modes and are automatically compared to get the source faulty pins (nodes).

In addition, the new hybrid-based self-test strategy, HYBST that tests the microcontroller circuits with small internal memories was presented. It combines both the SM-HBST strategy and the SBST strategy. Based on divide-and-conquer strategy, the microcontroller is divided into a number of main modules. The ISA of the microcontroller family is used to generate test subroutines as a part of the BIST scheme, which is the emulated TPG and part of the emulated test controller. The SM-HBST represents the other part of the BIST scheme as the test controller and the test response compaction. Each microcontroller module is exhaustively tested and all test patterns detect all combinational faults without fault simulator. The comparisons between the SBST strategy and the HYBST strategy show that the HYBST strategy is more suitable for testing of microcontroller chips with small internal memories. The HYBST strategy is superior in:

1) RAM utilization; where it reduces RAM utilization.
2) Flash memory utilization; where it reduces flash memory utilization.
3) Test application time; where it reduces total number of clock cycles.
4) Testing all internal microcontroller modules, and testing of GPIO pins using the SM-HBST.

Experimental results showed that the presented test solution offers a suitable test strategy for complete digital electronic boards, composed of digital random logic ICs and microcontroller chips with small internal memories. It indicates a real practical strategy with the aid of the SM-HBST, and reduces testing difficulty to achieve high fault coverage.

References

[1] M. H. El-Mahlawy, "Pseudo-Exhaustive Built-In Self-Test for Boundary Scan", Ph.D. dissertation, Kent University, U.K., 2000. Accessed on December 19th, 2018, available at: https://www.researchgate.net/profile/Mohamed_El-Mahlawy/publication/35962900_Pseudo-exhaustive_built-in_self-test_for_boundary_scan/links/58931820a6fdcc45530af29c/Pseudo-exhaustive-built-in-self-test-for-boundary-scan.pdf

[2] N. K. Jha and S. Gupta, *Testing of Digital Systems*, Cambridge University Press, 2003.

[3] A. Miczo, *Digital Logic Testing and Simulation*, John Wiley & Sons, 2003.

[4] M. El Said Gohniemy, S. Fadel Bahgat, Mohamed H. El-Mahlawy, and E. E. M. Zouelfoukkar, "A Novel Microcomputer Based Digital Automatic Testing Equipment using Signature Analysis," *IEEE International conference on Industrial Applications in Power Systems, Computer Science and Telecommunications*, pp. 140-144, Bari, Italy, May 13-16, 1996.

[5] M. Abramovici, M. A. Breuer, A. D. Friedman, *Digital systems testing and testable design*, Wiley-IEEE Press, New York, 1994.

[6] S. I. Morsy, "Hybrid Self-Test Solution in Embedded System on Chip", M.Sc. thesis, Military Technical College, Cairo, Egypt, 2012.

[7] M. H. El-Mahlawy, Ehab A. El-Sehely, Al-Emam S. Ragab, and Sherif Anas, "Design and Implementation of a New Built-In Self-Test Boundary Scan Architecture." *IEEE 15th International conference on Microelectronics*, pp. 27-31, Dec. 9-11, 2003.

[8] D.K. Sharma, Meerut, R.K. Sharma, B.K. Kaushik, and Pankaj Kumar, "Boundary scan based testing algorithm to detect interconnect faults in printed circuit boards," *Circuit World*, vol. 37, no, 3, pp. 27–34, 2011.

[9] M. H. El-Mahlawy, "Signature Multi-Mode Hardware-Based Self-Test Architecture for Digital Integrated Circuits," *IEEE International Conference on Electronics, Circuits, & Systems*, pp. 437-441, Dec. 6-9, 2015.

[10] M. H. El-Mahlawy, and Ahamed Seddik, "Design and Implementation of New Automatic Testing System For Digital Circuits Based on The Signature Analysis," *12th International Conference on Aerospace Sciences & Aviation Technology*, Military Technical College, Egypt, May 29-31, 2007.

[11] M. H. El-Mahlawy, Ahmed Abd El-Wahab, and Al-Emam S. Ragab, "FPGA Implementation of the Portable Automatic Testing System for Digital Circuits," *6th International Conference of the Electrical Engineering*, Military Technical College, Egypt, May 27-29, 2008.

[12] M. H. El-Mahlawy, Emad H. Khalil, Fawzy Ibrahim, and Mohamed. H. Abd El-Azeem, "Two-Test Pattern Capabilities of the LFSR/SR Generator in Pseudo-Exhaustive Testing based on Coding Theory Principles," *European Journal of Scientific Research*, vol. 140, no. 2, pp. 161-177, July 2016.

[13] Mohamed H. El-Mahlawy, and Winston Waller, "New Test Pattern Generators for the BIST Pseudo-Exhaustive Testing based on Coding Theory Principles," *Communications on Applied Electronics*, vol. 4, no. 8, pp. 29-44, April 2016.

[14] P. K. Lala, *Digital circuit testing and testability*, Academic Press, 1997.

[15] A. Krstic, and Kwang-Ting (Tim) Cheng, *Delay Fault Testing for VLSI Circuits*, Kluwer Academic Publishers, 1998.

[16] T. W. Williams, W. Daehn, M. Gruetzner, and C. W. Starke, "Bounds and analysis of aliasing errors in linear feedback shift register," *IEEE transactions on computer-aided design*, vol. 7, no. 1, pp 75-83, Jan. 1988.

[17] M. H. El-Mahlawy, "Signature-Based Self-Test Approach for Single-Shot Circuits on the Circuit Board Level," *4th International Japan-Egypt Conference on Electronics, Communications and Computers* (*JEC-ECC*

2016), pp. 38-42, May 31 - June 2, 2016.

[18] M. Psarakis, Dimitris Gizopoulos, Ernesto Sanchez and Matteo S. Reorda, "Microprocessor Software-Based Self-Testing," *IEEE Design & Test of Computers*, vol. 27, no. 3, pp. 4-19, May/June, 2010.

[19] J. Shen and J. A. Abraham, "Native Mode Functional Test Generation for Processors with Applications to Self-Test and Design Validation," *IEEE International Test Conference* (*ITC*), pp. 990-999, Oct. 18-23, 1998.

[20] Hunger and A. Gaertner., "Functional Charaterization of Microprocessors," *IEEE International Test Conference* (*ITC*), pp. 794-803, 1984.

[21] J. V. De-Goor, and O. Jansen, "Self-Test for the Intel 8085," *Microprocessing and Microprogramming*, vol. 29, no. 3, pp. 165-175, Oct. 1990.

[22] D. Brahme and J. A. Abraham, "Functional Testing of Microprocessors," *IEEE Transactions on Computers*, vol. C-33, no. 6, pp. 475–485, June 1984.

[23] S. M. Thatte and J. A. Abraham, "Test Generation for Microprocessors," *IEEE Transactions on Computers*, vol. C-29, no. 6, pp. 429-441, June 1980.

[24] R. Velazco, C. Bellon, and H. Ziade, "Analysis of Experimental Results on Functional Testing and Diagnosis of Complex Circuits," *IEEE International Test Conference* (*ITC*), pp. 64-72, Sep. 1988.

[25] L. Chen and S. Dey, "Software-Based Self-Testing Methodology for Processor Cores," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 20, no. 3, pp. 369–380, March 2001.

[26] N. Kranitis, G. Xenoulis, A. Paschalis, D. Gizopoulos, and Y. Zorian, "Application and Analysis of RT-level Software-Based Self-Testing for Embedded Processor Cores," *IEEE International Test Conference* (*ITC*), vol. 1, pp. 431-440, Sept. 30-Oct. 2, 2003.

[27] N. Kranitis, A. Merentitis, G. Theodorou, D. Gizopoulos, and A. Paschalis, "Hybrid-SBST Methodology for Efficient Testing of Processor Cores," *IEEE Design & Test of Computers*, vol. 25, no. 1, pp. 64-75, Jan.-Feb. 2008.

[28] L. Terng, W. C. E. Stroud, and N. A. Touba, *System-on-Chip Test Architectures - Nanometer Design for Testability*, Elsevier, 2008.

[29] N. Kranitis, G. Xenoulis, D. Gizopoulos, A. Paschalis, and Y. Zorian, " Low-Cost Software-Based Self-Testing of RISC Processor Cores," *Proceedings of the Design, Automation and Test in Europe Conference and Exhibition* (*DATE'03*), Munich, Germany, March 3-7, 2003.

[30] D. V. Kodavade, and S.D. Apte, "An Intelligent Framework for Fault Diagnosis in 89c51RD2 Microcontroller Based System," *IEEE International Workshop on Intelligent Data Acquisition and Advanced Computing Systems: Technology and Applications*, pp. 283- 286, Italy, Sep. 21-23, 2009.

[31] M. Predko, *Programming and Customizing PICmicro Microcontrollers*, 3rd edition, Toronto, Canada, McGraw-Hill Companies Inc., 2008.

[32] M. H. El-Mahlawy, Sherif Anis, Mahmoud E. A. Gadallah, and Emad A. El-Samahy, "FPGA-Based Implementation of the Digital Testing of Analogue Circuits," *European Journal of Scientific Research*, vol. 138, no. 4, pp. 256-286, April 2016.

[33] M. S. Saleh, Mohamed H. El-Mahlawy and Hossam E. Abou-Bakr Hassan, "Digital Signature Based Test of Analogue Circuits Using Amplitude Modulated Multi-Tone Signals" *IEEE 28th International conference on Microelectronics*, pp. 117-120, Dec. 17-20, 2016.

[34] A. Mousa, and M. H. El-Mahlawy, "Test Pattern Generator Optimization for Digital Testing of Analogue Circuits" IEEE 8th International Conference on Intelligent Computing and Information Systems (ICICIS 2017), pp. 118-126, Dec. 5-7, 2017.

[35] J. V. De-Goor and Z. Al-Ars, "Functional Memory Faults: A Formal Notation and a Taxonomy," *18th IEEE VLSI Test Symposium*, pp. 281-289, 30 Apr-04 May, 2000.

[36] S. Hamdioui1, A. J. van de Goor, and M. Rodgers, "March SS: A Test for All Static Simple RAM Faults," *IEEE International Workshop on Memory Technology Design and Testing*, pp. 95-100, 2002.

[37] S. D. Carlo, A. Bosio, G. D. Natale and P. Prinetto, "March AB, a State-of-the-Art March Test for Realistic Static Linked Faults and Dynamic Faults in SRAMs," *IET Computer & Digital Techniques*, vol. 1, no. 3, pp. 237-245, May 2007.

[38] M. S. Ragab, Mohamed H. El-Mahlawy and Emad A. El-Samahy, "Efficient Microcontroller System to Test an SRAM Chip Using Signature Analysis," *13th International Computer Engineering Conference* (*ICENCO*), Dec. 27-28, 2017.

[39] I. El-Kabbey, *Testing of Electronic Boards*, M.Sc. thesis, Military Technical College, Cairo, Egypt, 2008.

[40] M. H. El-Mahlawy, Mahmoud S. Hamed, Mohamed H. Abd-El-Zeem, and Issa Yossef, "FPGA Implementation of the BIST IP For SRAM Chips", *6th International Conference of the Electrical Engineering*, Military Technical College, Egypt, May 27-29, 2008.

[41] J. M. Rabaey, *Digital Integrated Circuits — A Design Perspective*, 2nd edition, Prentice Hall, 2003.

Probabilistic Techno-Economic Optimization in Medium Voltage Distribution Networks with Fault Passage Indicators and Fault Locators

Predrag Mršić, Đorđe Lekić, Bojan Erceg, Čedomir Zeljković, Petar Matić,
Siniša Zubić, and Przemyslaw Balcerek

***Abstract*—Fault passage indicators (FPIs) and fault locators (FLs) are employed in modern distribution networks in order to enhance the process of fault localization, thus resulting in reduction of interruption time and improving the reliability of power supply. In this paper, a novel probabilistic techno-economic optimization method is proposed for determining the number and positions of FPIs that lead to maximum reduction of interruption time and investment costs in medium voltage (MV) distribution networks with and without FLs. The proposed method is based on a probabilistic non-sequential Monte Carlo simulation model of the real network, which is a proper compromise between complicated sequential simulation models and too simplified analytical models. The main goal of the method is to obtain maximum improvement of the network reliability indices while using the minimum number of FPIs. The method is tested on a combined urban/rural MV distribution network in Bosnia and Herzegovina and results are thoroughly discussed.**

***Index Terms*—Distribution network, fault locators, fault passage indicators, non-sequential Monte Carlo simulation.**

Original Research Paper
DOI: 10.7251/ELS1822080M

I. Introduction

Occurrences of faults in the power distribution system are unavoidable due to many reasons [1]. Short circuit faults lead to interruptions in the power supply, decreasing thereby reliability offered to the customers. Each outage results in financial costs to distribution companies due to undelivered energy and penalties for energy not supplied [2]-[4]. On the other hand, quality regulation schemes adopted in many countries provide incentives to distribution system operators (DSOs) for establishing satisfactory levels of reliability indices [5]-[7]. Thus, one of the main tasks of the DSO is to improve the system reliability.

Manuscript received 26 October 2018. Accepted for publication 17 December 2018.

P. Mršić, Đ. Lekić, B. Erceg, Č. Zeljković, and P. Matić are with the Faculty of Electrical Engineering, University of Banja Luka, Banja Luka, Republika Srpska, Bosnia and Herzegovina (+387(51)221-868; fax: +387(51)221-820; e-mail: predrag.mrsic@etf.unibl.org).

S. Zubić is with ABB AB, Grid Automation Products, Västerås, Sweden (e-mail: sinisa.zubic@se.abb.com).

P. Balcerek is with ABB Corporate Research Center, Krakow, Poland (e-mail: przemyslaw.balcerek@pl.abb.com).

An efficient measure for increasing the reliability of the distribution system is to reduce the interruption time by performing faster fault localization [1]. As a cost-effective solution, fault locators (FLs) and fault passage indicators (FPIs) are employed in modern distribution networks [8]-[12]. FLs determine the distance to the fault based on the faulty line impedance, which is derived from voltage and current measured at the supply point during the fault. FLs are reasonably accurate for faults adjacent to the beginning of the line and/or for low impedance faults, while their accuracy significantly decreases in cases of remote and high impedance faults [8]. Another drawback of the FLs is that they cannot unambiguously determine the faulty branch in networks containing branches [8]. FPIs determine the location of the fault by detecting the passage of fault current through a section of a feeder on which they are installed. The fault is located in the area between the last indicator that detected the passage of fault current and the first following that did not.

Commonly, one FL is placed in the substation at the supply point of the network, while several FPIs can be placed at suitable locations in the distribution network. Because of significant costs related to the installation of FPIs, their exact number and positions for a given network must be determined in order to achieve a satisfactory ratio between installation costs and increased reliability [13]-[21].

Based on the research conducted in [21]-[24], the main goal of this paper is to propose a probabilistic techno-economic analysis for determining optimal number and positions of FPIs which will yield the maximum reduction of interruption time and costs both for networks with and without FLs. In order to take all influential factors into consideration, a comprehensive assessment methodology is developed and a simulation approach based on the probabilistic principle is employed.

The methodology is presented in Section II, where the optimization process is divided in two parts – technical and economic. Existence of the optimum, dimensionality problems and convergence of the technical optimization are addressed in detail and verified through results obtained on a real test network. Economic optimization, which is further explained, is based on achieving the techno-economic balance between benefits arisen from improved reliability and installation costs of FPIs. At the end of Section II, a comprehensive optimization algorithm is presented, followed by a thorough analysis of

mathematical models used on each step of the algorithm. As many inputs are uncertain and behave according to the laws of probability theory, the Monte Carlo simulation technique is employed. In Section III, the final results of the probabilistic optimization are displayed in form of cumulative probability density functions (CDFs) for one real combined urban/rural medium voltage (MV) distribution network in Bosnia and Herzegovina. Conclusions are given in Section IV.

II. METHODOLOGY

In this section, a methodology for determining the number and positions of FPIs in MV distribution network is proposed and discussed. According to our literature review, there are two approaches to determine optimal locations and number of FPIs. The first approach includes direct optimization methods. The most common direct approach is finding the positions of FPIs by minimizing the sum of total interruption costs and the costs of investment and installation. Since the interruption costs are in a complex relation with the locations of FPIs, the minimum of the objective function is not easily achievable. The authors in [13] employed a mixed integer linear programming (MILP) formulation. By considering not only FPIs but also the other remotely controlled switching equipment, the number of independent variables included in the problem formulation is greater than 30. The approach in [14] is similar though with a simpler objective function. Instead of using the MILP technique for optimization, the authors employed the immune algorithm. The authors in [15] showed the application of the genetic algorithm (GA) for various types of technical and economic objective functions. Another application of GA in combined techno-economic optimization can be found in [16]. The second approach is based on the indirect principle. An auxiliary objective function is created which is much simpler for optimization, while the obtained results are still located in the vicinity of the optimal solution. Under the indirect approach, the authors use rather heuristic methods to find locations in the network which are good candidates for installing the FPIs. The cost effectiveness of the method is tested and verified afterwards. One of the first ideas for indirect approach is the fuzzy method [17], [18]. Instead of computing precise positions appropriate for installation of FPIs, the method provides the results in a form of a chart which shows the installation potential for each bus along the *main feeder*, which represents distance from the network substation to the farthest network bus [19]. Another step forward is made in [19], where a simple auxiliary function is proposed and GA is employed for its minimization.

In this paper, the indirect approach is utilized because of its simplicity and acceptable accuracy in practical applications. The methodology consists of technical and economic optimization and is sketched in Fig. 1. The technical optimization is performed first, where a given number of FPIs is properly distributed across the network. After the technical optimization, the economic optimization is performed, with potential FPI locations and their number as an input. The output of economic optimization is selection of the best set of FPIs (number and locations) which will provide the greatest profit.

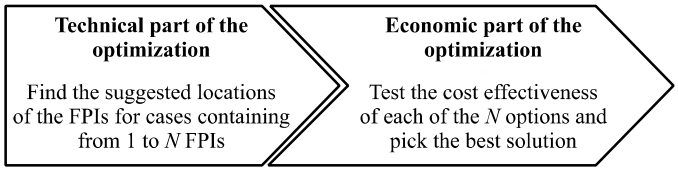


Fig. 1. The optimization process consisted of two main components.

A. Technical Optimization

The technical part of the optimization contains an algorithm which suggests potential locations for a given number of FPIs. The initial idea for technical optimization, which is based on the indirect principle, was introduced in [19]. In order to perform a fast, yet acceptably accurate, search optimization process, a simplified auxiliary objective function is formed which is in correlation with the target reliability indices. It is recognized that load, number of customers and distances between FPIs are the most important inputs for this optimization function. The following two principles are introduced:

- A feeder bus is a good candidate to install an FPI if the load and the number of customers located downstream from that feeder bus are high.
- The considered bus becomes a less favorable candidate for FPI installation if another FPI has already been installed in its vicinity.

Moreover, the technical and economic indices could be further improved if a couple of additional principles are also taken into account [21]:

- Impact of lateral branches should be included in the fault search priority.
- Failure rate is not constant along the main feeder.

The mentioned four principles are incorporated in the objective function:

$$f_{obj} = \int_0^{x_{max}} \left[\alpha_1 l(x) + \alpha_2 c(x)\right] d(x) f(x) dx \,. \tag{1}$$

In (1), the first principle is modeled by $\alpha_1 l(x) + \alpha_2 c(x)$, where $l(x)$ represents the normalized load, and $c(x)$ represents the normalized number of customers in terms of location on the main feeder. The constants α_1 and α_2 are the weighting coefficients for the load and number of customers, respectively. The second and third principles are taken into account by the distance $d(x)$. This distance represents relative distance from the location of the fault to the nearest device able to indicate that fault and the impact of lateral branches to the expected time to find a fault. Finally, the fourth principle means that the failure rate changes along the main feeder. The failure rates are not the same in urban and rural areas. In addition, the failure rates of the laterals are greater than the failure rate of the main feeder. The failure rate function which combines impacts of both main feeder and its laterals is designated with $f(x)$. A graphic illustration of (1), calculated for the test network (see Appendix), is presented in Fig. 2. In order to find the best solution, the locations of the FPIs are varied along the main feeder until the area under the curve is minimized.

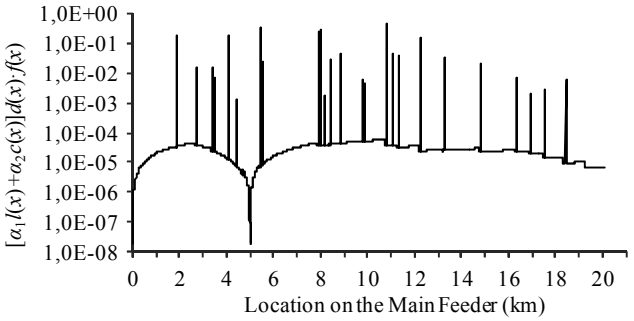


Fig. 2. Example of the objective function computed for the test network with one FPI. The FPI is located 5 km downstream along main feeder.

1) Existence of the optimum

For a small number of FPIs and an acceptable (small) search step, the objective function (1) can be minimized by employing a simple, yet time consuming, brute force search method. In this method, the value of the objective function (1) is calculated for all possible locations of FPIs and for several numbers of FPIs in a given distribution network. The combination that yields the minimum value of the objective function (1) is declared the optimal solution. For example, by moving one FPI along the main feeder of the test network (see Appendix) one obtains the diagram in Fig. 3. It can be seen that the objective function for this case reaches its minimum when the FPI is located 7908 m away from the network substation. Therefore, if one FPI is to be installed in this test network, it should be placed 7908 m away from the network substation along the main feeder.

If there are more than two FPIs, then it is not possible to construct a graphical interpretation of the objective function vs. FPI locations. However, in order to demonstrate the problems which arise when minimizing the objective function for cases with more than two FPIs, a special diagram in Fig. 4 is constructed. This diagram shows the objective function vs. positions of two FPIs for the case when eight FPIs are used, whereas six of them have fixed positions. For the area shown in Fig. 4 the objective function has a total of four extremes, of which three are local extremes. The existence of local extremes can lead to the result where the optimization algorithm converges to the local rather than to the global extreme. Thus, one should be careful when using evolutionary algorithms for finding the optimal number of FPIs.

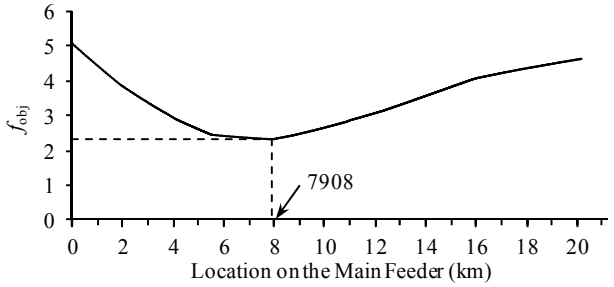


Fig. 3. Objective function vs. FPI location for the case when one FPI is located at the main feeder of the test network.

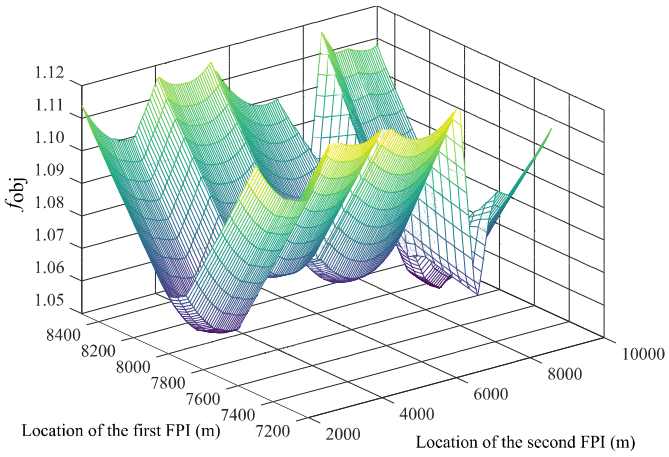


Fig. 4. Objective function vs. FPI location for the case when eight FPIs are located at the main feeder of the test network (positions of six FPIs are fixed).

2) Dimensionality problem of brute force search method

As was mentioned before, the brute force search method is applicable only for a small number of FPIs in a given distribution network. The reason behind this is the rapid increase in the number of combinations of FPI locations followed by the increase in the number of installed FPIs. In order to demonstrate this, let us consider the test network in which the length of the main feeder is 20100 m. If the resolution for FPI locations along the main feeder is chosen to be 50 m, then there would be 402 possible FPI locations. If one FPI is to be installed in this network, one would have to search for the optimum location among these 402 possible locations, i.e. there would be a total of 402 combinations. If N FPIs are to be installed, then the number of total combinations would be:

$$N_{com} = \binom{402}{N} = \frac{402!}{(402-N)!N!}. \tag{2}$$

The increase of the number of combinations with the increase of the number of FPIs and search resolution is shown in Fig. 5. By observing Fig. 5, it can be concluded that number of combinations rapidly increases with the increase in the number of FPIs. It is clear that for a large number of FPIs or in the case of a small search step, the objective function cannot be efficiently minimized in this manner.

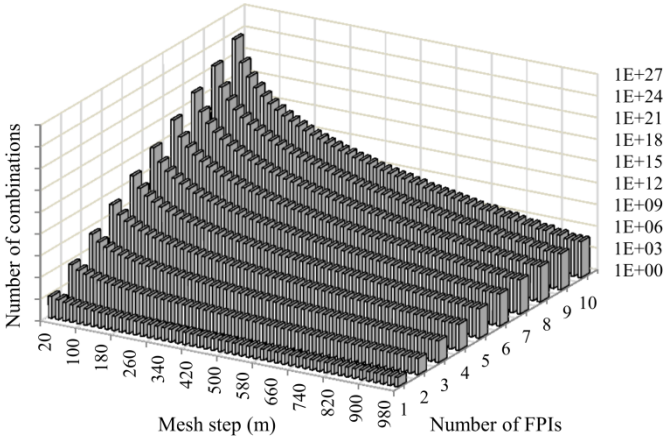


Fig. 5. Number of combinations vs. searching resolution and number of FPIs.

3) Pattern Search method

One of the fast and efficient methods for minimization of the objective function is the Pattern Search (PS) algorithm. Initial research on the applicability of the PS method to the problem of optimal location of FPIs was presented in [21]. In this paper, the method is further improved in terms of setting the initial guess, increasing the stability of convergence and applicability to the problem defined in the probabilistic form.

The idea of PS is about a half century old [25]. The method has been tested and developed over the years so far and it has been applied to many scientific disciplines. There are also applications of PS algorithm to the problems of electric power engineering [26]. The main advantage of the method is that PS does not require a gradient of the objective function. It is therefore applicable for minimization of various non-continuous and non-differentiable functions.

In order to apply the PS method for minimizing the objective function (1) a few modifications have to be made. First of all, the FPIs can be located only on the main feeder, which means that the FPI location can move along one axis of the mesh only. Second of all, if the basic PS principle is to be used, the optimum location of all or some of the FPIs could be placed to fall beyond the main feeder, due to doubling of the mesh step. By introducing constraints in the minimization of objective function (1), modified PS methods are obtained.

The first method (PS1) is similar to the original PS method [26]. Starting from the initial guess of the optimal point, the step of the mesh is doubled or divided by two depending on the location for which the value of (1) is minimal. The initial mesh step for this method is 1 m. By applying this method, it can easily happen that the optimum FPI location falls beyond the main feeder. If so, following rules are applied:

- If the obtained optimal location, measured as the distance from the network substation to the FPI along the main feeder, is less than zero, the FPI is set to location zero at the beginning of the main feeder.
- If the obtained optimal location is larger than the length of the main feeder, the FPI is moved to the end of the main feeder.

In the second method (PS2) the step of the mesh is never doubled but only divided by two if certain conditions are met [21]. In this manner, one avoids the situation where optimal FPI locations fall beyond the main feeder. The initial mesh step for this method is selected to obtain fast search for optimal FPI locations between two initial FPI locations. A good empirical value is $L_{MF}/(5N)$, where L_{MF} is the length of the main feeder and N is the total number of FPIs.

The third method (PS3) is proposed in this paper and is based on the sequential principle where in each step the PS mesh for one FPI is observed. If it turns out that the locations of FPIs are optimal for a given mesh step, the mesh step is divided by two. As in the s method the initial mesh step is chosen in a way that enables fast search for optimal FPI locations between two initial FPI locations. The optimization process is continued until a specified accuracy is achieved or until the maximum allowable number of iterations is reached.

4) Initialization and convergence analysis of PS

So far we have defined three methods obtained by the modification of the original PS method. From these definitions it can be concluded that different optimization methods in general require different total number of iterations for convergence. In order to compare convergence speed of these methods, the iteration step must be strictly defined. In the following analysis, one iteration step of the optimization method is defined as a set of operations needed to calculate the value of the objective function (1) for one particular combination of FPI locations. The initial guess of FPI locations greatly affects the convergence speed and the accuracy of the obtained solution. In order to formulate recommendations for the selection of initial FPI locations, the influence of the initial guess on the number of iterations and solution accuracy is analyzed for several cases.

A series of simulations was conducted for different initial locations and different number of FPIs. For a particular number of FPIs, the value of the objective function (1) was calculated for all solutions with different initial guesses. The solutions for which the value of the objective function (1) was minimal were declared as global minima for that particular number of FPIs, while the other solutions were declared as local minima. The results of these simulations will serve as the basis for deriving a new method for the selection of initial FPI locations.

Before the convergence analysis, we will explain the meaning of used symbols. A circle indicates that the method converges towards the global minimum, while a triangle indicates that the method converges towards a local minimum.

If the FPIs are initially equally distributed along the main feeder:

$$x_{\mathrm{FPI}}(j) = \frac{j}{i+1} L_{\mathrm{MF}}, \quad j = 1,\ldots i \quad i = 1,2\ldots N, \tag{3}$$

results shown in Fig. 6 are obtained. In this case, the first method (PS1) converges towards the global minimum when the total number of FPIs is lower than four. The second and third method (PS2 and PS3) converge towards the global minimum when the total number of FPIs is equal to one or three. Thus, selecting the initial locations of FPIs in this manner gives poor optimization results, especially when the number of FPIs increases.

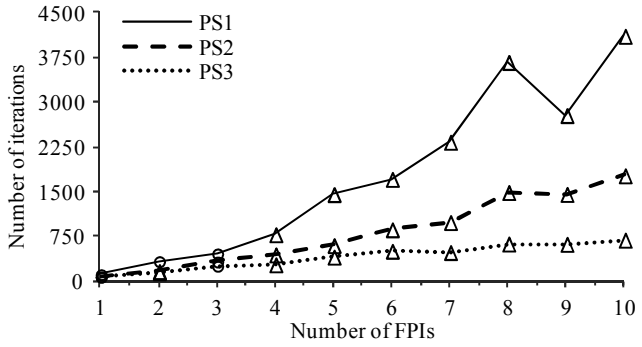


Fig. 6. Number of iterations vs. number of FPIs for the case when all FPIs are initially equally distributed along the main feeder.

In the second case, FPIs are initially equally distributed along the first half of the main feeder. For this case the results are shown in Fig. 7. All methods, except PS3 for three FPIs, converge to the global minimum when the total number of FPIs is lower than six.

In the third case, FPIs are initially equally distributed along the first 70 % of the main feeder. The first method (PS1) converges towards the global minimum when the total number of FPIs is lower than four and equal to six, seven, eight and nine. The second method (PS2) converges towards the global minimum when the total number of FPIs is lower than four and equal seven, nine and ten, while the third method (PS3) converges to the global minimum when the total number of FPIs is lower than four and higher than six. For this case the results are shown in Fig. 8.

From these results, we conclude that, for a given distribution network, optimal selection of initial FPI locations depends on the total number of FPIs. The authors did not notice any regularity in convergence that could be applied to an arbitrary number of FPIs. The convergence to the global optimum is also highly dependent on the topology of the particular distribution network.

5) Results of the technical part of the optimization

According to the optimization principle depicted in Fig. 1, the technical component of the optimization method provides the suggested positions of FPIs along the main feeder, for an initially given number of indicators. The procedure is repeated for all numbers of FPIs which can result in reasonable benefit to cost ratio.

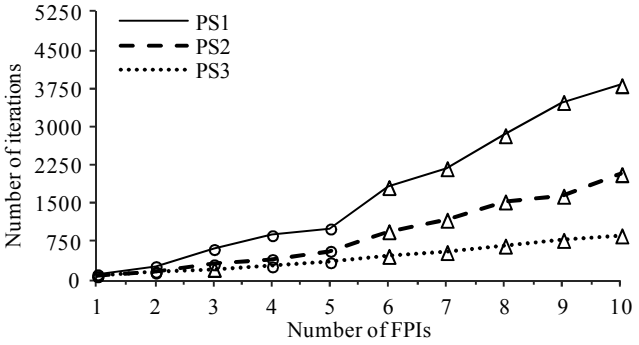


Fig. 7. Number of iterations vs. number of FPIs for the case when the all FPIs are initially equally distributed along the first half of the main feeder.

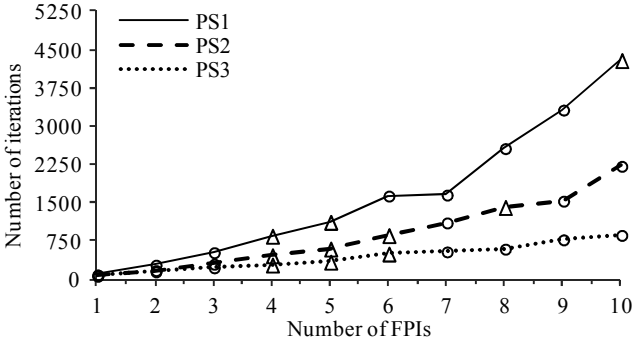


Fig. 8. Number of iterations vs. number of FPIs for the case when the all FPIs are initially equally distributed along the first 70 % of the main feeder.

It is believed that it is sufficient to test cases containing up to 10 FPIs, since the benefit of improved reliability does not uniformly follow the FPI installation costs, but significantly decreases the speed of its growth as the number of indicators increases. The results of the technical part of the optimization can concisely be shown in one chart, as represented by Fig. 9. The most profitable case from this finite set of options will be declared to be the optimum solution, which will be selected in the economic part of the optimization.

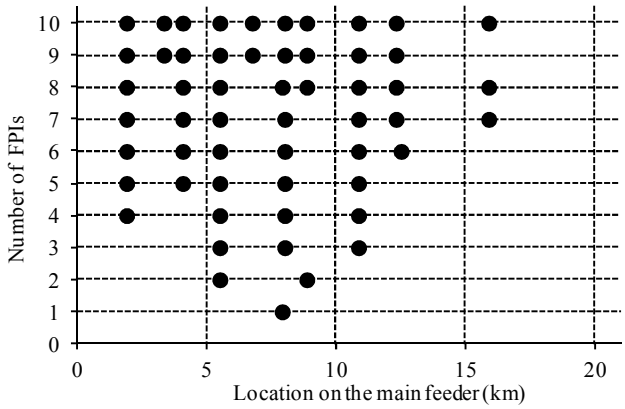


Fig. 9. The suggestion for optimal placement of the FPIs.

B. Economic Optimization

In the economic part of the optimization, the economically best solution of previously determined total FPI numbers and locations will be selected. The optimum number of FPIs is the one that yields the maximum difference between the incentive, i.e. reward or penalty, according to achieved values of reliability indices due to optimum placement of FPIs, and the total cost of installed FPIs. The objective function for the economic optimization can be formulated as [24]:

$$Y_{\mathrm{FPI}}(N) = B_{\mathrm{FPI}}(N) - N \cdot FPI_{\mathrm{cost}}, \tag{4}$$

where $Y_{\mathrm{FPI}}(N)$ is the annual financial profit of the distribution company when N FPIs are installed, $B_{\mathrm{FPI}}(N)$ is some kind of benefit of improved reliability, expressed as either avoided penalty, gained incentive or just decreased raw costs of not supplied energy (in countries without developed regulation in the area of system reliability) for the case when N FPIs are installed, and FPI_{cost} is the annual cost per installed FPI. The optimal number of FPIs in a specific distribution network is found as the number N_{opt} that yields the maximum value of (4), which is shown in Fig. 10.

The reliability indices in a specific distribution network improve with the increase in the number of installed FPIs. This increase is not linear, which means that for each distribution network there is a number of FPIs beyond which the improvement of the reliability indices, and the corresponding benefit $B_{\mathrm{FPI}}(N)$, is insignificant (solid line in Fig. 10). The investment and maintenance costs of FPIs increase with the number of installed FPIs, whereas this increase is linear (dotted line in Fig. 10). For a particular number of FPIs, all the benefit, due to increased reliability, is cancelled out by the total investment costs (point B in Fig. 10).

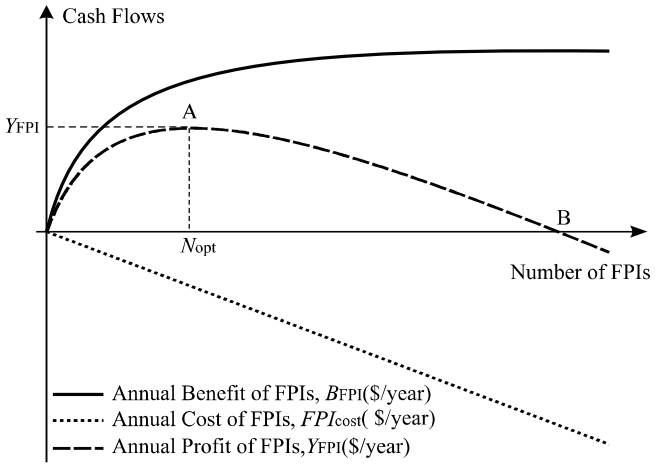


Fig. 10. The principle of finding the optimum number of FPIs [24].

The optimal number of FPIs for a given distribution network is therefore determined as the option that gives the maximum value of profit (point A on dashed line in Fig. 10).

The annual costs per FPI depend on the price of the FPI itself and on the price of additional equipment, the cost of installation and maintenance, as well as the lifetime. These costs are derived from following expression [15]:

$$FPI_{\text{cost}} = \frac{FPI_{\text{price}} + FPI_{\text{inst}}}{FPI_{\text{age}}} + FPI_{\text{maint}}, \tag{5}$$

where FPI_{price} is the price, FPI_{inst} is the installation cost, FPI_{age} is the lifetime and FPI_{maint} is the maintenance cost of one FPI. The maintenance costs primarily contain the costs for maintenance and rental of communication channels, while the installation cost is primarily related to the additional equipment needed for installation and deployment of FPIs, as well as for the purchase of certain software and other necessary equipment.

The cost of the FL is considered to be negligible in this analysis. This is done because the FL is a standard piece of equipment which is already embedded in protective relays at the moment they are shipped and it is not billed separately.

Benefits $B_{\text{FPI}}(N)$ may significantly vary from country to country so they should be analyzed in more detail. Norway was one of the first countries which introduced a penalty scheme for operation at poor reliability. The penalties introduced in 2001 were based on not supplied energy. Regulated penalty prices are determined as 38 NOK (cca \$2) per kWh for commercial/industrial customers interrupted for all sustained interruptions (longer than 5 minutes) and 4.2 NOK (cca \$0.2) per kWh interrupted for residential customers [27]. According to a principle applied in Sweden [5], Germany or Spain [7], $B_{\text{FPI}}(N)$ is calculated based on customer interruption costs and the performance using the *System Average Interruption Duration Index* (SAIDI) and *System Average Interruption Frequency Index* (SAIFI) compared to some defined baseline [27].

The optimal positions of FPIs do not affect the value of SAIFI, but they affect the value of SAIDI, which means that the incentive $B_{\text{FPI}}(N)$ can be calculated as [27]:

$$B_{\text{FPI}}(N) = \sum_{i=1}^{5}\sum_{j=1}^{2}\left[SAIDI_{\text{b},ij} - SAIDI_{ij}(N)\right]\cdot c_{ij}\cdot P_{\text{av},i}, \tag{6}$$

where i represents the index of five different customer groups (industry, residential, agriculture, public and commercial services), j represents the index of two different categories of interruption (planned and unplanned), $SAIDI_{\text{b},ij}$ is the defined baseline value of SAIDI for i-th customer group and j-th category of interruption, $SAIDI_{ij}(N)$ is the achieved value of SAIDI for i-th customer group and j-th category of interruption due to optimal placement of N FPIs, c_{ij} is a cost parameter given in €/kWh and $P_{\text{av},i}$ is the average yearly power usage for i-th customer group.

C. Simulation Algorithm

The main steps of the proposed simulation algorithm are listed in the following procedure [23], [24]:

1) *Preparing the Network Data*: Prepare the common input data such as distribution network topology, failure rates, customer power demands, number of simulated years etc.
2) *Generating the Artificial Set of Faults*: Determine the set of random faults for each simulated year, respecting their conditional probability distributions in terms of hour, weekday and month of occurrence, as well as their yearly variation.
3) *Simulating the Customer Loads*: Simulate the customer loads at the instants of faults, which are needed for calculating *Energy Not Supplied* (ENS).
4) *Simulating a Decision of the FL*: Simulate decisions made by the FLs, which are influenced both by their performance and the characteristics of the fault.
5) *Computing the Time Needed to Find a Fault*: Compute the time taken by the repair crew to find the fault (support provided by the FPIs is taken into account).
6) *Evaluating the Reliability Indices*: Evaluate the reliability indices such as SAIDI and ENS.
7) *Presenting the results*: Present the results and make conclusions.

A detailed explanation of each step of the simulation algorithm is given in the following text.

1) Preparing the Network Data

Information about the distribution network topology is stored in a matrix form. The matrix contains data about the number of buses, number, length and failure rates of power lines, number and power demands of customers, and location of disconnectors, reclosers, fuses and FPIs. In this analysis, disconnectors, reclosers, fuses and FPIs are considered to be 100 % reliable, which means that their failure rate is equal to zero or that their failure rates are included in failure rates of power lines. Furthermore, distributed generation is neglected.

2) Generating the Artificial Set of Faults

The methodology for generating random faults is inspired by the research published in [28]. The main idea is to draw random numbers to reproduce a time-dependent failure rate pattern similar to the observed pattern recorded in failure statistics. This pattern includes all types of faults, caused by the weather or by technical and human aspects. Fault causes and mechanisms are not modeled explicitly and the observed pattern is assumed to be representative for the analysis period ahead. As the first step, the number of faults in a simulated year should be determined. For that purpose, a random number is drawn from the Poisson probability distribution. The Poisson probability distribution is a discrete probability distribution that expresses the probability of a given number of events occurring in a fixed interval of time and/or space if these events occur with a known constant rate and independently of the time since the last event [23].

For the chosen number of faults per year, the timing of these faults is determined. It is widely known that instants of fault occurrence are not uniformly distributed in time. There are many reasons for this. For example, construction works will cause faults to occur more frequently during the first shift (9AM - 5PM) in working days than during the nights or weekends. Another example is summer thunderstorms which cause faults more frequently during summer months than in other seasons. Therefore, failure probability distribution should be determined from recorded instants of occurrence of faults in a given time interval (in a month or in a day/time in a week). The examples of hourly, daily and monthly failure probability distributions are given in Fig. 11 to 13, which are determined from recorded instants of fault occurrence in a test network (see Appendix). Faults which are generated for Monte Carlo simulation should follow the given probability distributions.

An example for drawing numbers which will represent a month in which fault occurs is given in Fig. 14. The input discrete failure probability distribution function by months (data in Fig. 13) is transformed into the cumulative distribution function (Fig. 14). Then, a random number from the uniform distribution U [0, 1] is drawn (in our example, the number is 0.65). The month in which the fault occurs is determined from the point where the line of constant value 0.65 intersects the cumulative distribution function (CDF), which is the eight month in the example (August). Since the probability for all numbers from 0 to 1 is the same, it can be concluded that numbers of months that have a larger increment of the CDF will be generated more frequently. In other words, months in which failures are more frequent will be selected more often.

Four types of faults are considered: Phase-to-ground fault (L-G), Double-phase-to-ground fault (L-L-G), Double-phase fault (L-L) and Three-phase fault (L-L-L). Similarly as for determining instants of failure occurrence, statistics of fault types is used as input function. A usual probability distribution per fault type is shown in Fig. 15, but there also are some specific networks when probability distribution differs from the most common cases. For instance, in networks where phase conductors touch each other more frequently, 68 % of failures are of double-phase fault type [29].

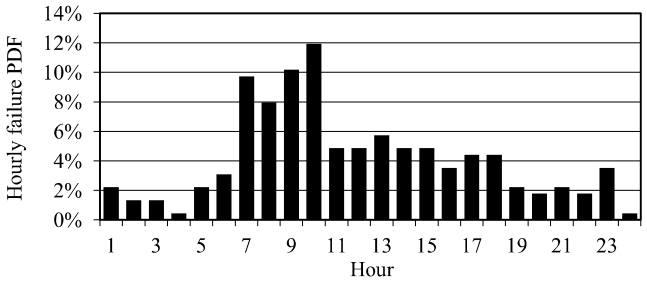


Fig. 11. Probability of faults per hour of day.

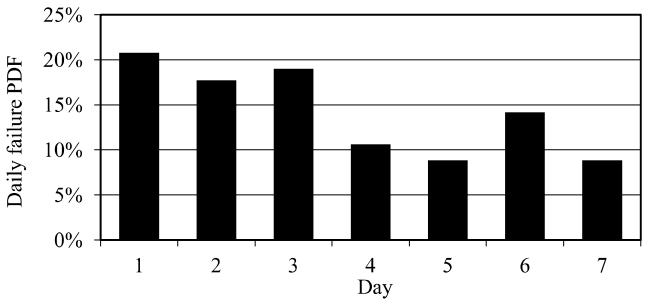


Fig. 12. Probability of faults per day of week.

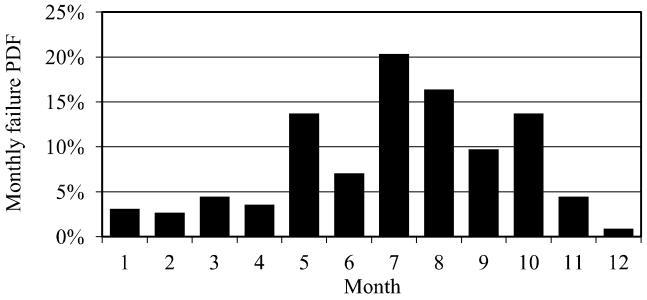


Fig. 13. Probability of faults per month [23].

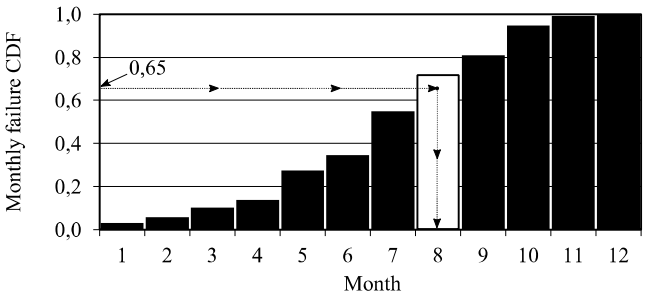


Fig. 14. The principle of drawing a random month of a fault occurrence.

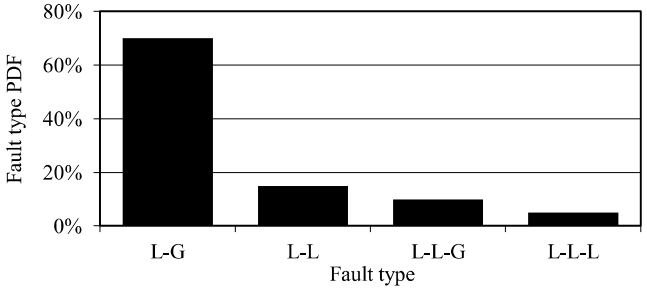


Fig. 15. Typical probability distribution per fault type [23].

The failure rates change along the main feeder as we move from urban to rural areas. Additionally, the failure rates of the lateral branches are greater than the failure rate of the main feeder. The faulted line is chosen by intersecting the CDF curve of branch failure rates with a line of constant value drawn from the uniform distribution. When the faulted line is chosen, the fault location along the line is picked by drawing a random number, again from the uniform distribution.

Fault impedance is simulated by the Weibull probability density function [8]. For inter-phase faults, fault impedance is small and in general does not exceed 0.5 Ω. They may, however, become much higher during ground faults, because tower footing resistance may be as high as 10 Ω. If there is a flashover of an insulator, the connection of towers with ground wires makes the resulting fault impedance smaller. In practice, it seldom exceeds 3 Ω. For some ground faults the fault impedances may become much higher, which happens in cases of fallen trees, or if a broken conductor lies on the high-resistive soil [8].

3) Simulating the Customer Loads

Just as the probability of fault occurrence varies with time, the customer load is also dependent on the hour of day, day of week and month of year [30]. Based on long-term measurements, it is possible to determine the usual patterns of expected customer load in terms of hour, day and month. Expected load of the customer connected at some bus i, at the instant of fault occurred in hour h, day d and month m, is computed by the following expression [23]:

$$P_e(h,d,m) = P_h \cdot P_d \cdot P_m \cdot P_i , \tag{7}$$

where P_h is the average relative load during the hour h, independent of weekday and month (presented in Fig. 16), P_d is the average load in day d, independent of month (presented in Fig. 17), P_m is the average load in month m (as illustrated in Fig. 18), and P_i is the annual peak load for the customer connected at bus i (given as a part of common input data, explained in the first step of the simulation algorithm). The actual simulated load is then sampled from the normal distribution using the following equation [23]:

$$P_{simulated} = P_e + \sigma \cdot P_e \cdot N(0,1) , \tag{8}$$

where σ is relative average standard deviation of the customer load and $N(0,1)$ is a random number drawn from the standard normal distribution, having zero mean value and unity standard deviation.

4) Simulating a Decision of the FL

The starting point for developing this model are the empirical findings which state that 1 % (of the main feeder length) fault location error can be achieved for phase-to-phase faults (R_{fault} = 15 Ω), while the errors for solid earth faults (R_{fault} = 0 Ω) are 10–15 %. The error is given as a fraction of the main feeder length. Fault location error e, according to appropriate IEEE standard [31], is defined as follows:

$$e = (IR - DF)/L_{\text{MF}} , \tag{9}$$

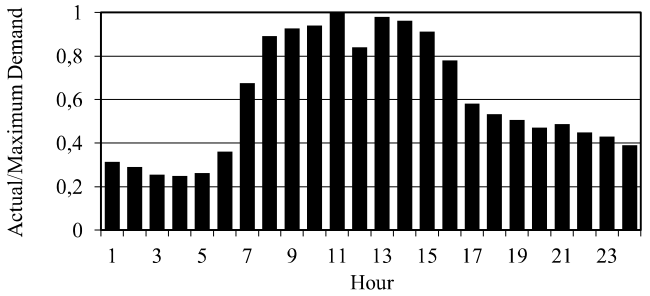


Fig. 16. Hourly load as a percentage of daily peak load.

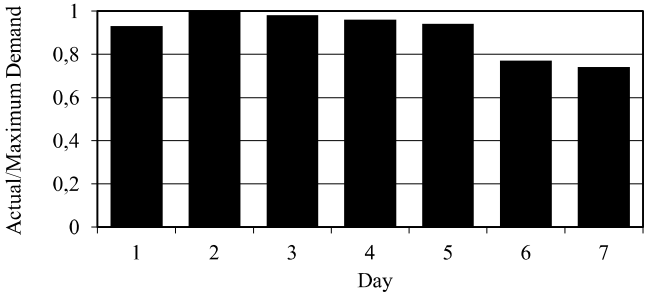


Fig. 17. Daily load as a percentage of weekly peak load.

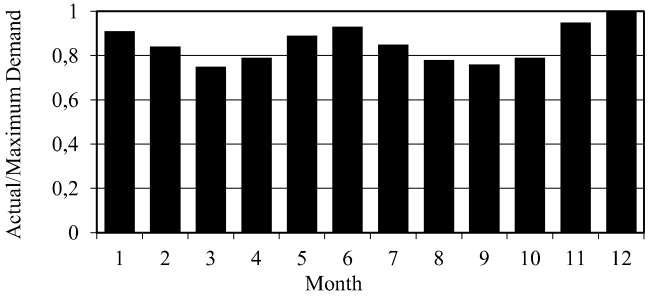


Fig. 18. Monthly load as a percentage of annual peak load.

where IR is the instrument reading and DF is the exact distance to the fault. Therefore, a simulated instrument reading would be:

$$IR = DF + e \cdot L_{\text{MF}} . \tag{10}$$

It will be assumed that the error magnitudes are normally distributed and that their values are always negative, according to testing reports published in [8]. In order to respect the assumption that the expected value of the error should be 1 % for phase-to-phase faults and 15 % for earth faults, the simulated errors will be computed as follows [23]:

$$e = -\left| Expected\ error \cdot \sqrt{\pi/2} \cdot N(0,1) \right| . \tag{11}$$

5) Computing the Time Needed to Find a Fault

When calculating the time needed for fault localization, three scenarios should be considered:

- Scenario 1: Sole application of the FL (denoted as FL),
- Scenario 2: Sole application of FPIs (denoted as FPI),
- Scenario 3: Combined application of both technologies (denoted as FL + FPI).

For the first scenario, the idea is to calculate the time needed for the maintenance crew to find the fault by searching along the lines which are located in the vicinity of the location to which the FL is pointing. This vicinity is defined by the fault location error of the FL, as illustrated in Fig. 19a. According to (11), this error is negative, meaning that the crew should only inspect lines located at distances which are larger than the FL reading. If the network contains many branches and there are multiple potential fault locations, the search is performed by a pre-established priority order.

In the second scenario, the crew should search only the network area between the tripped and untripped FPI (Fig. 19b). The search is started from the tripped FPI and finished when the fault is localized. As for the previous scenario, the priority order is respected. A constant speed of moving along the lines is assumed.

In the third scenario, when both FLs and FPIs are used, the potential area on which the fault might have occurred is found as the intersection of the FL and FPI readings (Fig. 19c). Four possible cases of FPI and FL disposition during the fault are presented in Fig. 20. For the cases shown in Fig. 20a and Fig. 20d, the FPI doesn't influence the fault localization time, while for cases shown in Fig. 20b and Fig. 20c, the presence of FPI decreases the time needed to find the fault.

The overall time taken by the crew to realize the fault occurrence, to prepare the necessary tools and spare parts and to start the search process is considered to be constant and is added afterwards.

6) Evaluating the Reliability Indices

The most frequently used reliability indices are [32], [33]:

- average number of interruptions per customer per year,
- average interruption duration per customer per year,
- energy not supplied.

The average number of interruptions per customer per year (SAIFI – System Average Interruption Frequency Index) is defined as:

$$SAIFI = \frac{Total\ number\ of\ customer\ interruptions}{Total\ number\ of\ customers\ served}, \quad (12)$$

while the average interruption duration per customer per year (SAIDI – System Average Interruption Duration Index) is defined as:

$$SAIDI = \frac{Sum\ of\ all\ customer\ interruption\ durations}{Total\ number\ of\ customers\ served}. \quad (13)$$

Energy Not Supplied (ENS) is defined as the sum of the products of all customer interruption durations and their power demands:

$$ENS = \sum_i Interruption\ duration(i) \times Power\ demand(i). \quad (14)$$

In this paper, the presence of FLs and/or FPIs affects the value of SAIDI and ENS only, while SAIFI remains the same, regardless of the analyzed scenario.

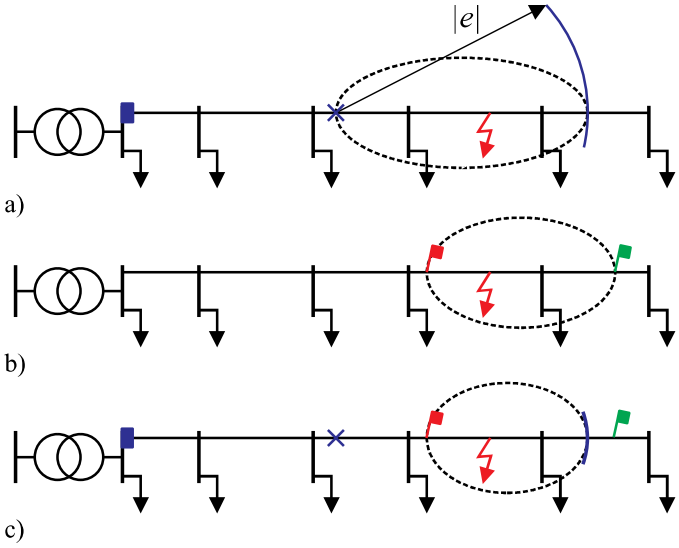


Fig. 19. Illustration of fault detection in a simple radial distribution system with a) one FL, b) two FPIs, and c) two FPIs and one FL. The red flag represents a tripped FPI, the green flag represents an untripped FPI, the blue square represents the FL installed in the substation, while the blue cross represents the FL reading.

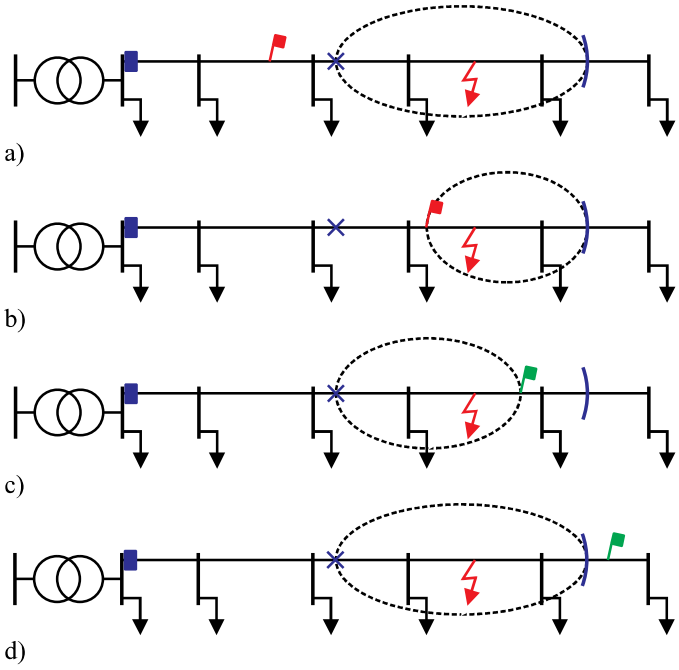


Fig. 20. Illustration of fault detection in a simple radial distribution system with one FPI and one FL in the case when a) the tripped FPI is located in front of the FL reading, b) the tripped FPI is located beyond the FL reading, inside the FL error area, c) the untripped FPI is located beyond the FL reading, inside the FL error area and d) the untripped FPI is located beyond the FL reading, outside the FL error area.

7) Presenting the results

The main outputs of the presented methodology are the reliability indices displayed in function of the number of installed FPIs, and cumulative probability density functions (CDFs) for objective function (4). As described above, three scenarios are compared: sole usage of one FL, sole usage of FPIs, and combined usage of both the FL and FPIs.

III. Application to Real-Life Test Network

In this Section the methodology proposed in the previous Section is applied to a representative real-life test network in Bosnia and Herzegovina (see Appendix). The results are obtained using the non-sequential Monte Carlo simulation method. Contingencies, that are determined before the simulation begins, are randomly selected from a pool of possible contingencies based on their probabilities of occurrence. The selected contingencies are then simulated in any order, assuming that all contingencies are mutually exclusive [34], [35]. As a consequence of the non-sequential approach, the actualization of costs is not considered.

A. Base case results

The inputs to the simulation algorithm are given in Table I and include target (baseline) value of SAIDI required by the distribution system regulator, cost parameter c_{ij}, average number of faults per year and time horizon (number of simulated years). Cost-benefit analysis is based on the approach explained in Section II, where the annual benefit is defined according to (4). The key economic benefit is modeled by cost parameter c_{ij} which makes the worth of reliability proportional to the difference between target and real SAIDI. The solution with the largest benefit is declared as "the optimal" for the given set of inputs, and contains "optimal number" and "optimal locations" of FPIs. By analyzing the final results, which are in the form of CDFs, the investor can select a proper solution from several cases: possibility of high profit, risk of possible loss, or a stable solution not having high possibility nor for extra high profit, nor for significant loss.

Fig. 21 shows main results of the proposed methodology for the base case. In this case, the installation options with 1, 2 or 3 FPIs represent the best achievable solutions, being very similar to each other. As seen from Fig. 21, the lines for 1 and 2 FPIs are more on the right-hand side with larger values of CDF. Therefore, 1 or 2 FPIs can be selected by risk taking investors which could achieve larger profits in some particular cases. On the other hand, risk averse investors would select 3 FPIs, which would provide a solid benefit with a lower risk of possible losses. Fig. 22 shows average SAIDI (expected value) as a function of the number of FPIs added in the network together with the FL. From Fig. 22, it can be concluded that for the case with no fault locating equipment installed (nor FL, nor FPI), SAIDI is 77.9 (value for zero FPIs on red FPI curve), while for the case with one FL only, SAIDI is decreased to 25.6 (blue FL curve).

TABLE I
The Values Of The Key Variables

Input variable	Value		
	Min.	Base	Max.
Cost parameter c_{ij} (€/kWh)	0.25	0.50	1.00
Average number of faults per year	5	10	20
Target SAIDI (hours/customer/year)	20	35	50
Number of simulated years		10000	
FPI price (€)		1000	
FPI installation cost (€)		2500	
FPI lifetime (years)		15	
FPI maintenance cost (€/year)		500	

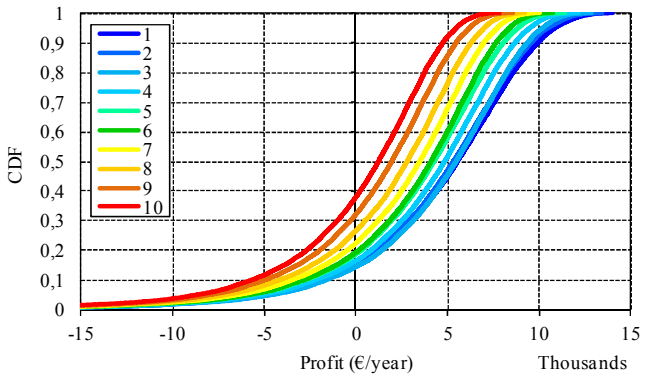


Fig. 21. CDF computed for profit, particularly for each investment solution from 1 to 10 FPIs for base values of key parameters.

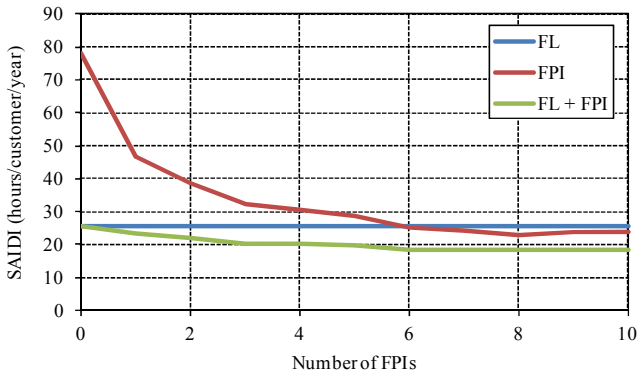


Fig. 22. Average SAIDI as a function of the number of FPIs for base values of key parameters.

For the case with both the FL and FPIs, decrease of SAIDI is the largest and it depends on the number of installed FPIs (FL + FPI curve). The curve starts at point (0; 25.6) at which the FL and zero FPIs are installed and stays below the FL and FPI curves regardless of the number of installed FPIs, which means that lowest values of SAIDI can be obtained if both the FL and FPIs are used.

B. Sensitivity Analysis

In order to analyze sensitivity of the proposed methodology to the variations of input variables, the key parameters are varied according to Table I. On the basis of this sensitivity analysis, proper planning actions for different scenarios can be undertaken in order to improve the network reliability.

Results of simulation for the case when the cost parameter is decreased from 0.5 to 0.25 €/kWh are given in Fig. 23. Since the reliability incentives are halved here, the profit earned from the installation of FPIs is decreased for any number of FPIs in the given range. In comparison with the base case results, shown in Fig. 21, the CDF curves are therefore shifted to the left. In this case, the installation option with one FPI represents the best achievable solution. Simulation results for the case when the cost parameter is increased from 0.5 to 1.0 €/kWh are given in Fig. 24. As opposed to results shown in Fig. 23, the reliability incentive is increased and all the CDF curves are pushed to the right. In this case, the installation of a greater number of FPIs becomes more profitable. The optimal number of FPIs for this scenario is 3.

Simulation results for the scenario where the number of faults per year is decreased from 10 to 5 are shown in Fig. 25. The lower failure rate reflects to the appropriate lower SAIDI, so the target level set for this reliability index is more easily achievable. The probability distributions of profit are acceptable for each considered number of FPIs, as can be seen in Fig. 25. However, the installation of one FPI represents the most profitable option. The simulation results for the scenario where the number of faults per year is increased from 10 to 20 are shown in Fig. 26. In this case, the distribution system regulator should adjust the target SAIDI to a value which would be more appropriate for the given network.

The simulation results for the scenario where the target SAIDI is decreased from 35 to 20 are shown in Fig. 27. In this scenario, due to significantly decreased value of required SAIDI, the profit is dominantly negative for any number of FPIs. Even with negative profit, the most adequate number of FPIs is 1, 2 or 3. Finally, the simulation results for the scenario where the target SAIDI is increased from 35 to 50 are shown in Fig. 28. In this scenario profit is always positive, and the optimal number of FPIs is 1, 2 or 3.

IV. Conclusion

The subject of this paper is a techno-economic analysis which determines the optimal number and positions of fault passage indicators (FPIs) for maximum reduction of interruption time and costs in radial distribution networks, both with and without fault locators (FLs) installed at the supply point.

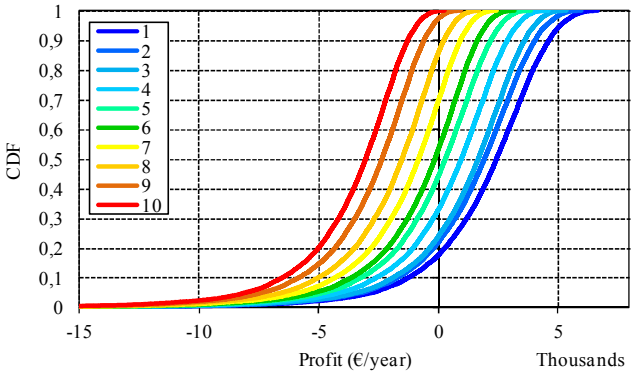


Fig. 23. CDF computed for profit, particularly for each investment solution from 1 to 10 FPIs for decreased cost parameter.

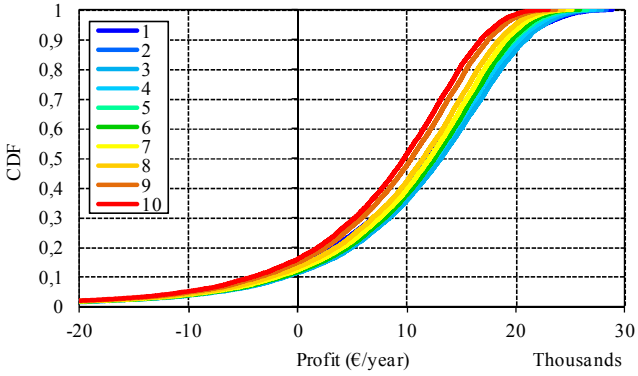


Fig. 24. CDF computed for profit, particularly for each investment solution from 1 to 10 FPIs for increased cost parameter.

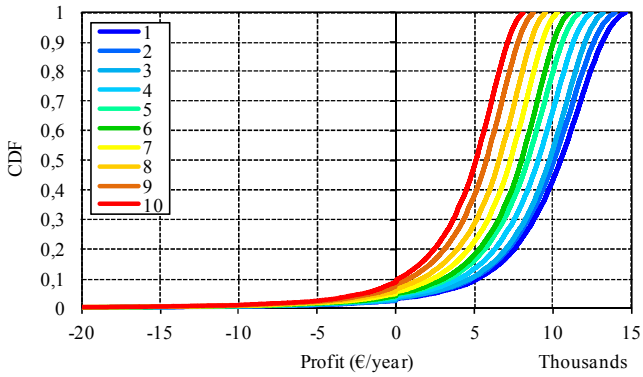


Fig. 25. CDF computed for profit, particularly for each investment solution from 1 to 10 FPIs for decreased number of faults per year.

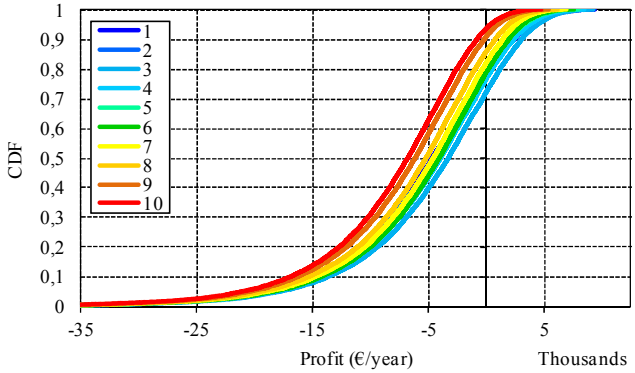


Fig. 26. CDF computed for profit, particularly for each investment solution from 1 to 10 FPIs for increased number of faults per year.

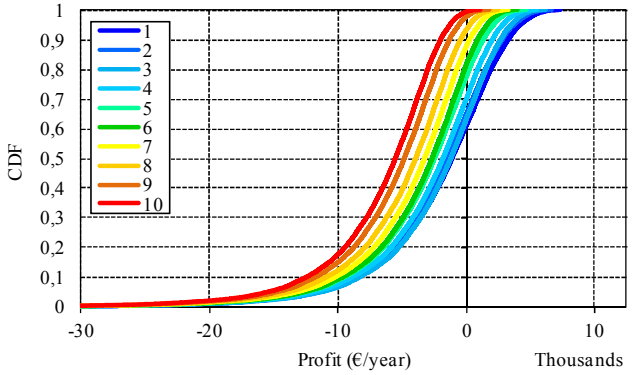


Fig. 27. CDF computed for profit, particularly for each investment solution from 1 to 10 FPIs for decreased value of target SAIDI.

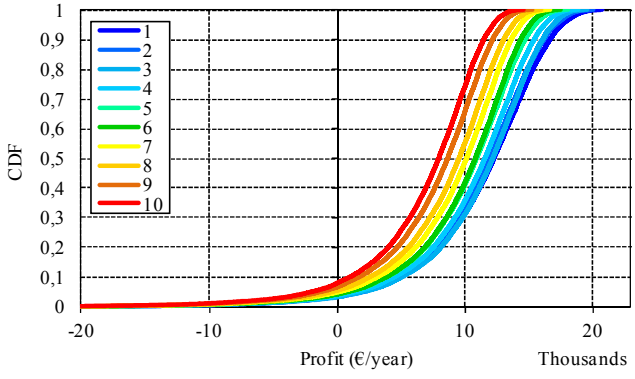


Fig. 28. CDF computed for profit, particularly for each investment solution from 1 to 10 FPIs for increased value of target SAIDI.

The developed optimization methodology is verified by several sets of simulations on a representative distribution network. The proposed method is suitable for application in suburban and rural networks which have high fault probabilities. In those networks the consumers are distributed over a large area having relatively low power consumption and priority, so it is not acceptable to invest in expensive automation equipment such as reclosers. In these networks, proper installation of FPIs can decrease the interruption time and improve network reliability quantified by indices SAIDI and ENS. On the other hand, if the proposed methodology would be applied in networks with a large number of ultra priority users and/or if the penalties for undelivered energy would be very high, it would result in the proposition of a large number of FPIs. However, those FPIs would only shorten the time of finding a fault location but would not reduce the number of power interruptions. For those networks the proposed methodology should be adjusted to include the installation of automated switching equipment as well.

REFERENCES

[1] J. Northcote-Green and R. G. Wilson, Control and Automation of Electric Power Distribution Systems, CRC Press, Taylor & Francis Group, 2007.

[2] G. Kjöle and H. Vefsnmo, "Customer Interruption Costs in Quality of Supply Regulation: Methods for Cost Estimation and Data Challenges," in *23rd International Conference on Electricity Distribution*, Lyon, France, pp. 1-5, 15-18 June 2015.

[3] I. Losa and O. Bertoldi, "Regulation of Continuity of Supply in the Electricity Sector and Cost of Energy not Supplied," in *2009 International Energy Workshop*, Venice, pp. 1-10, 2009.

[4] K. Samdal, G. H. Kjölle, B. Singh and O. Kvitastein, "Interruption Costs and Consumer Valuation of Reliability of Service in a Liberalised Power Market," in *9th International Conference on Probabilistic Methods Applied to Power Systems*, KTH, Stockholm, Sweden, pp. 1-7, June 11-15, 2006.

[5] E. Grahn, L. Ström, K. Alvehag, C. J. Wallnerström, L. W. Öhling and T. Johansson, "Incentivizing Continuity of Supply in Sweden," in *European Energy Market (EEM), 2016 13th International Conference on the*, Porto, Portugal, pp. 1-5, 6-9 June 2016.

[6] K. Alvehag and K. Awodele, "Impact of Reward and Penalty Scheme on the Incentives for Distribution System Reliability," *IEEE Trans. Power Syst.*, vol. 29, no. 1, pp. 386 - 394, 2014.

[7] C. Fernandesa, A. Candelab and T. Gómez, "An Approach to Calibrate Incentives for Continuity of Supply in the Spanish Electricity Distribution System," *Electric Power Systems Research*, vol. 82, pp. 81-87, 2012.

[8] M. Saha, J. Izykowski and E. Rosolowski, *Fault Location on Power Networks*, Dordrecht, Heidelberg, New York: Springer, 2010.

[9] E. Vidyasagar, P. V. N. Prasad, and A. Fatima, "Reliability Improvement of a Radial Feeder Using Multiple Fault Passage Indicators," *Energy Procedia*, vol. 14, pp. 223-228, 2012.

[10] H. Falaghi, M. -R. Haghifam, and M. R. Osouli Tabrizi, "Fault Indicators Effects on Distribution Reliability Indices," in *CIRED 2005 - 18th International Conference and Exhibition on Electricity Distribution*, Turin, pp. 1-4, June 2005.

[11] D. J. Krajnak, "Faulted Circuit Indicators and System Reliability," *IEEE Rural Electric Power Conference*, Kentucky, USA, pp. 1-4, May 2000.

[12] F. M. Angerer, "New developments in Faulted Circuit Indicators Help Utilities Reduce Cost and Improve Service," *IEEE Rural Electric Power Conference*, Charleston, South Carolina, USA, pp. 1-3, April 2008.

[13] Ž. Popović, S. Knežević, and B. Brbaklić, "Optimal Number, Type and Location of Remotely Controlled and Supervised Devices in Distribution Networks," in *IEEE PowerTech*, Eindhoven, pp. 1-6, June-July 2015.

[14] C. Y. Ho, T. E. Lee, and C. H. Lin, "Optimal Placement of Fault Indicators Using the Immune Algorithm," *IEEE Trans. Power Syst.*, vol. 26, pp. 38-45, February 2011.

[15] D-P. Cong, B. Raison, J-P. Rognon, S. Bonnoit, and B. Manjal, "Optimization of Fault Indicators Placement with Dispersed Generation Insertion," *IEEE Power Engineering Society General Meeting*, vol. 1, pp. 355-362, June 2005.

[16] R. Dashti and J. Sadeh, "Fault Indicator Allocation in Power Distribution Network for Improving Reliability and Fault Section Estimation," *International Conference on Advanced System Automation and Protection,* pp. 1406-1411, October 2011.

[17] D. M. B. S. de Souza, A. F. de Assis, I. N. da Silva, and W. F. Usida, "Efficient Fuzzy Approach for Allocating Fault Indicators in Power Distribution Lines," *IEEE Transmission and Distribution Conference and Exposition: Latin America*, pp. 1-6, August 2008.

[18] D. M. B. S. de Souza, I. N. da Silva, V. Ziolkowski and R. A. Flauzino, "Efficient Allocation of Fault Indicators in Distribution Circuits Using Fuzzy Logic," *IEEE Power & Energy Society General Meeting*, pp. 1-6, Calgary, Alberta Canada, July 2009.

[19] W. F. Usida, D. V. Coury, R. A. Flauzino and I. N. da Silva, "Efficient Placement of Fault Indicators in an Actual Distribution System Using Evolutionary Computing," *IEEE Trans. Power Syst.*, vol. 27, no. 4, pp. 1841-1849, November 2014.

[20] A. Shahsavari, S. M. Mazhari, A. Fereiduisn, and H. Lesani, "Fault Indicator Deployment in Distribution Systems Considering Available Control and Protect Devices: A Multi-Objective Formulation Approach," *IEEE Trans. Power Syst.*, vol. 29, pp. 2359-2369, September 2014.

[21] Č. Zeljković and P. Mršić, "Fast and Efficient Placement of Fault Indicators Based on the Pattern Search Algorithm," in *Power Electronics (Ee), 2017 International Symposium on*, Novi Sad, Serbia, pp. 1-5, 19-21 Oct. 2017.

[22] Đ. Lekić, P. Mršić, B. Erceg and Č. Zeljković, "Three Phase Line Model for Laboratory Testing of Fault Passage Indicators," in *The 10th Mediterranean Conference on Power Generation, Transmission, Distribution and Energy Conversion - Med Power 2016*, Belgrade, Serbia, pp. 1-8, 6-9 Nov. 2016.

[23] Č. Zeljković, P. Mršić, Đ. Lekić, B. Erceg, P. Matić, S. Zubić, and P. Balcerek, "Performance Assessment of Fault Locators and Fault Passage Indicators in Distribution Networks by the Non-Sequential Monte Carlo Simulation," in *2018 International Symposium on Industrial Electronics (INDEL)*, Banja Luka, Bosnia and Herzegovina, pp. 1-7, 1-3 Nov. 2018.

[24] P. Mršić, Č. Zeljković, Đ. Lekić, B. Erceg, P. Matić, S. Zubić, and P. Balcerek, "Minimization of Power Interruption Time in MV Distribution Networks with Fault Locators Based on Optimal Placement of Fault Passage Indicators," in *2018 International Symposium on Industrial Electronics (INDEL)*, Banja Luka, Bosnia and Herzegovina, pp. 1-7, 1-3 Nov. 2018.

[25] R. Hooke and T. A. Jeeves, "Direct search solution of numerical and statistical problems," *Journal of the Association for Computing Machinery* (ACM), vol. 8, no. 2, pp. 212–229, 1961.

[26] A. K. Al-Othman and K. M. El-Naggar, "Application of pattern search method to power system security constrained economic dispatch with non-smooth cost function," *Electric Power Systems Research*, vol. 78, no. 4, pp. 667–675, April 2008.

[27] Electricity Working Group, Quality of Supply Task Force, "Third Benchmarking Report on Quality of Electricity Supply 2005," Council of European Energy Regulators, Bruxelles, 2005.

[28] G. H. Kjölle and A. T. Holen, "Reliability and interruption cost prediction using time-dependent failure rates and interruption costs," *Quality and Reliability Engineering International*, vol. 14, no. 3, pp. 159-165, 1998.

[29] V. Vega-Garcia, J. C. Cebrian and N.Kagan, "Evaluation of probability functions related to short circuit random variables using power quality meters," in *2010 IEEE/PES Transmission and Distribution Conference and Exposition*, Latin America, pp. 712-718, Nov. 8, 2010.

[30] I.-S.Bae, J.O.Kim, J.-C.Kim and C.Singh, "Optimal operating strategy for distributed generation considering hourly reliability worth," *IEEE Trans. Power Syst.*, vol. 19, pp. 287-292, February 2004.

[31] IEEE Std C37.114, IEEE Guide for Determining Fault Location on AC Transmission and Distribution Lines, June 2005.

[32] E. Fumagalli, L. Lo Schiavo and F. Delestre, *Service Quality Regulation in Electricity Distribution and Retail*, Springer-Verlag Berlin, 2007.

[33] T. A. Short, *Electric Power Distribution Handbook*, Taylor & Francis Group, 2014.

[34] R. Billinton and W. Li, *Reliability assessment of electric power systems using Monte Carlo methods*, Springer Science+Business Media, LLC, New York, 1994.

[35] R. E. Brown, *Electric Power Distribution Reliability*, CRC Press, Taylor & Francis Group, Boca Raton, FL, 2009.

APPENDIX

The test network used in simulations is given below. The distances between adjacent system bus bars are indicated in meters on power lines connecting them, while the total number and annual peak load of customers are indicated by two numbers at the bus bar to which the load is connected. The failure rate of power lines in suburban area is 0.2 1/km/year, while the failure rate in rural area is 0.3 1/km/year.

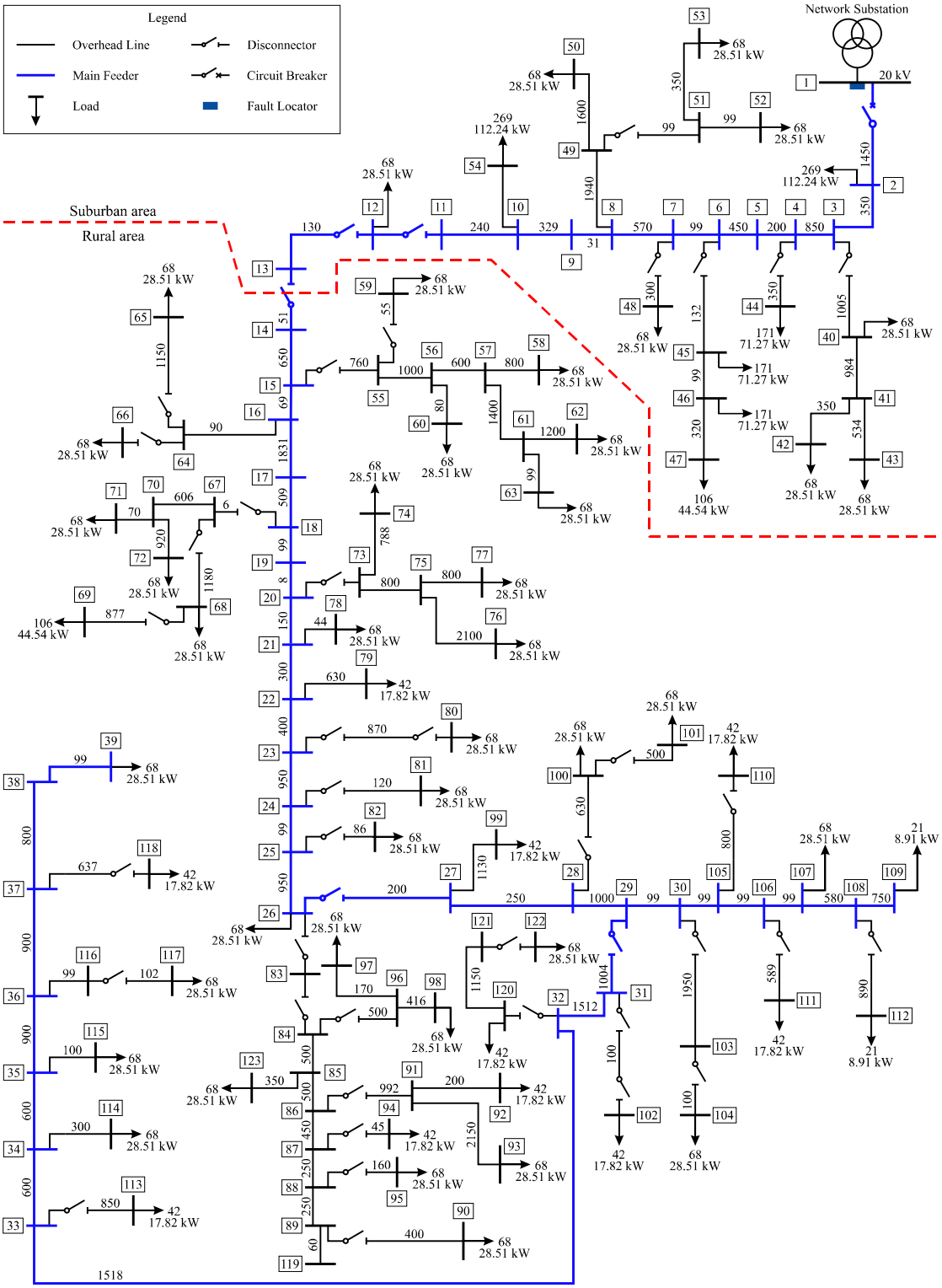


Fig. 29. Test network [24].

Finite Element Design of Rotor Permanent Magnet Flux Switching Machine with Arbitrary Slot, Pole and Phase Combinations

Đorđe M. Lekić and Slobodan N. Vukosavić

***Abstract*—A two-dimensional finite element approach for designing RPMFS (Rotor Permanent Magnet Flux Switching) machines is presented in this paper. The proposed method enables fast, accurate and computationally efficient assessment of different RPMFS machine designs with an arbitrary number of rotor poles, stator slots and stator phases. The appropriate stator winding layout is assembled for any feasible slot, pole and phase combination by employing the winding distribution table, which contributes to automating the design process. Based on the proposed method, a program is developed using the Octave FEMM (Finite Element Method Magnetics) toolbox. The program is suited for the use in the design stage, where it is necessary to determine various machine parameters for given core dimensions, terminal voltage constraints and adopted value of current density in the conductors, while taking iron saturation effects into account. Verification was carried out by simulating torque and EMF waveforms for several RPMFS machine designs.**

***Index Terms*—Rotor permanent magnet flux switching machine, Octave, finite element method magnetics.**

Original Research Paper
DOI: 10.7251/ELS1822093L

I. Introduction

ELECTRICAL machine design today is reemerging as one of the engineering disciplines that attracts wide attention of both the industrial and scientific community. This becomes evident after inspecting the literature on electrical machine design published just in the last decade [1], [2]. Advancements in the fields of computer simulation, mathematical modeling and optimization have lead to improvements in design of electrical machinery, increasing thereby the accuracy in prediction of machine performance and decreasing the costs of development in the design stage. In order to ensure market competitiveness, electrical machine manufacturers tend to reduce machine size for a given torque rating and to increase their efficiency, increasing the need for design optimization [1], [2]. In addition, a variety of novel electrical machine topologies, especially permanent magnet synchronous machines (PMSMs) and new types of multiphase and fractional slot windings demand fast and accurate evaluation of different machine designs. While the use of empirically established analytical methods is limited to design of conventional machine topologies [3], most new types of electrical machines are designed by using Computer-Aided-Design tools (CAD). As most new types of electrical machines operate in conditions where the iron core is highly saturated, their design is, for the most part, based on FEA (Finite Element Analysis) [4].

Continuing the research conducted in [5] and [6], the authors of this paper present a two-dimensional finite element (FE) approach for designing RPMFS (Rotor Permanent Magnet Flux Switching) machines. RPMFS machines represent a relatively new concept of PMSMs, which were first proposed in [7]. The basic operation principle of the RPMFS machine is presented in [7] and [8]. In comparison to SPMFS (Stator Permanent Magnet Flux Switching) and IPM (Interior Permanent Magnet) machines with the same core dimensions, RPMFS machines feature higher torque density values and lower values of torque ripple [9]. These features make RPMFS machines suitable for use in traction applications, such as EVs (Electric Vehicles) and HEVs (Hybrid Electric Vehicles), where the space available for installing the machine is limited and where high torque density and low torque ripple are required. Furthermore, torque production of RPMFS machines is not significantly influenced by permanent magnet (PM) demagnetization, as opposed to SPMFS machines, where demagnetization reduces the value of average torque [10]. In [11] several RPMFS designs with fixed core dimensions and fixed number of stator slots, but with different number of rotor poles are analyzed, confirming that torque production of the RPMFS machine can be improved by selecting the appropriate number of rotor poles. It should be noted, however, that the number of stator slots per rotor pole has a high impact on machine cogging torque [12], which is a dominant part of torque ripple, making it an important issue for traction applications. Thus, a comprehensive analysis and design optimization must take different slot, pole and phase combinations into account. The process of assembling an appropriate stator winding for feasible slot, pole and phase combinations can be generalized and, to a certain extent, automated by employing the winding distribution table (WDT), which was first proposed in [13].

Manuscript received 14 November 2018. Received in revised form 5 December 2018. Accepted for publication 7 December 2018.

Đ. M. Lekić is a PhD student at the Faculty of Electrical Engineering, University of Belgrade, Belgrade, Serbia. He is currently with the Faculty of Electrical Engineering, University of Banja Luka, Banja Luka, Republika Srpska, Bosnia and Herzegovina (+387(51)221-868; fax: +387(51)221-820; e-mail: djordje.lekic@etf.unibl.org).

S. N. Vukosavić is with the Faculty of Electrical Engineering, University of Belgrade, Belgrade, Serbia. (e-mail: boban@etf.bg.ac.rs).

The main goal of this study is to develop a methodology for finite element based design of RPMFS machines which is not restricted to any specific values of core dimensions, number of rotor poles, stator slots or even stator phases, making it suitable for use in the design stage, for evaluating torque production and induced voltage quality, or in automated design optimization. The proposed method is implemented as a program in Octave software using the Octave FEMM toolbox [14], while femm 4.2 software is employed for FE simulations [15], [16]. The program workflow is shown in Fig. 1.

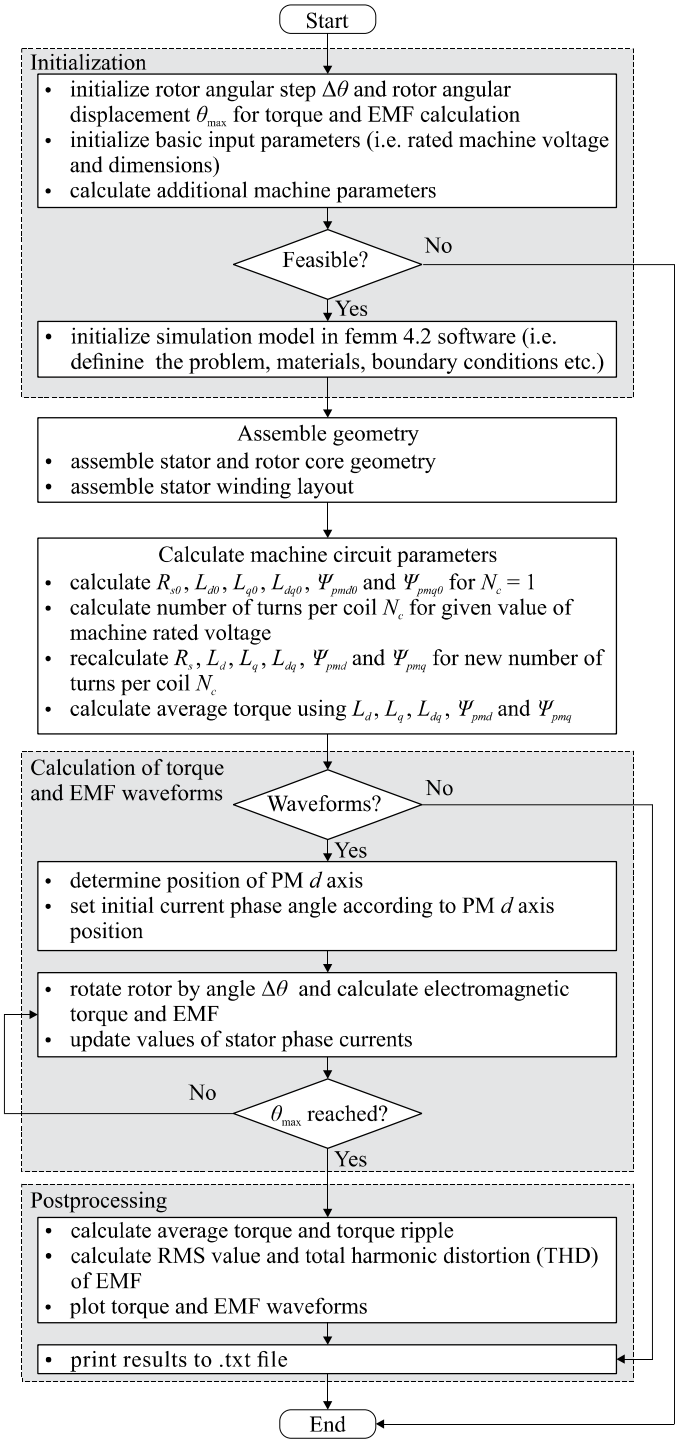


Fig. 1. Program workflow.

The organization of this paper resembles the program workflow shown in Fig. 1. In Section II the main input parameters are explained and the methodology for assembling the stator and rotor geometry, as well as the stator winding layout is presented. The algorithm for calculating machine circuit parameters such as resistances, inductances and flux linkages is given in Section III, while the methodology for obtaining electromagnetic torque and induced electromotive force (EMF) waveforms is presented in Section IV. Section V summarizes the results for several RPMFS designs with different number of slots, poles and phases, while general conclusions are given in Section VI.

II. Assembling RPMFS Machine Model

In this Section, the process for assembling the RPMFS machine model in femm 4.2 software will be explained. In order to get insight into the topology of the RPMFS machine, Fig. 2 shows an example of a 28-pole, 24-slot RPMFS machine. The stator is equipped with a single layer non-overlapping fractional slot winding. This type of stator winding consists of alternate tooth-wound coils which have short end windings, low values of resistances and copper losses, high values of slot fill factor, negligible values of coil mutual inductances and a high fault tolerance capability [18], [19]. While the stator has a conventional design, the construction of the rotor is somewhat special. From Fig. 2 it can be seen that the rotor magnetic circuit consists of so-called "rotor cells" which are placed on a non-magnetic support body [5]-[11]. Each rotor cell consists of a permanent magnet placed between two rotor teeth, whereas the rotor tooth tips form alternate magnetic poles. In this manner, one rotor cell represents one pole pair.

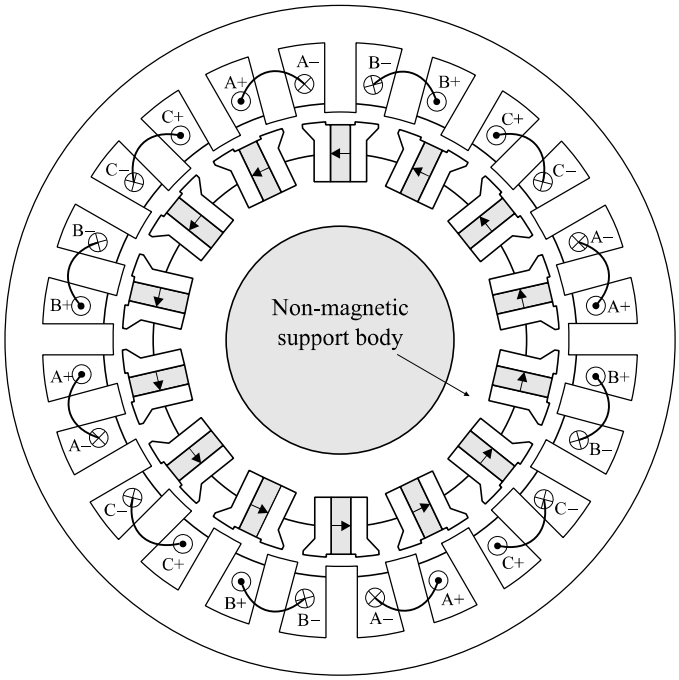


Fig. 2. Cross-section of a 28-pole, 24-slot RPMFS machine. The stator of the machine is equipped with a single layer non-overlapping fractional slot winding, consisting of 12 alternate tooth-wound coils. The rotor is equipped with 14 "rotor cells", each containing 2 magnetic poles, placed on a non-magnetic support body [6].

A. Input Parameters

In the initialization part of the program, the values of following parameters are defined:

- number of stator slots – Q_s;
- number of rotor poles – $2p$;
- number of stator winding phases – m;
- number of stator winding layers – n_{lay};
- slot fill factor – k_{Cu};
- RMS value of rated phase voltage – U,
- rated current density in the conductors – J;
- rated rotor speed – n.

The last four parameters are defined for the purpose of EMF and torque calculation, while all other parameters are used for assembling stator and rotor geometry, as well as the stator winding layout. As will be explained in Section IV, the torque and EMF waveforms are obtained by rotating the rotor in steps $\Delta\theta$ over an angle $\theta_{\max}$, so that both these values are also defined in the initialization part of the program. The stator and rotor dimensions are defined according to Tables I and II, where the proposed ranges ensure reasonable machine designs. Only the stator outer diameter D_s, the stator lamination stack length l_s and the air-gap length δ_g are defined in meters, while all other dimensions are defined in relative units, as indicated in Tables I and II. In this manner, the program is not restricted to one particular set of machine core dimensions and it is sufficient to redefine just the basic parameters (D_s, l_s and δ_g) in order to get a new set of machine core dimensions with the same mutual ratios. Also, defining the core dimensions in relative units makes the program more suited for implementation of algorithms for geometry optimization [17].

TABLE I
STATOR INPUT DIMENSIONS [5]

Parameter name	Range
Ratio of inner and outer diameter (split ratio)	$0.45 < d_s/D_s < 0.75$
Ratio of tooth width to slot pitch	$0.3 < b_{ts}/\tau_s < 0.7$
Ratio of slot opening width to slot pitch	$0.05 < b_{os}/\tau_s < 0.7$
Ratio of tooth height to difference of outer and inner radius	$0.4 < 2h_{ts}/(D_s - d_s) < 0.8$
Ratio of tooth tip height to difference of outer and inner radius	$0 < 2h_{os}/(D_s - d_s) < 0.1$

TABLE II
ROTOR INPUT DIMENSIONS [5]

Parameter name	Range
Ratio of inner and outer diameter (split ratio)	$0.45 < d_r/D_r < 0.75$
Ratio of tooth width to inner pole pitch	$0.3 < b_{tr}/\tau_{ir} < 0.7$
Ratio of PM width to inner pole pitch	$0.3 < b_{pm}/\tau_{ir} < 0.7$
Ratio of slot opening width to outer pole pitch	$0.3 < b_{or}/\tau_{or} < 0.7$
Ratio of pole width to outer pole pitch	$0.3 < b_p/\tau_{or} < 0.7$
Ratio of tooth tip height to difference of outer and inner radius	$0.05 < 2h_{or}/(D_r - d_r) < 0.1$

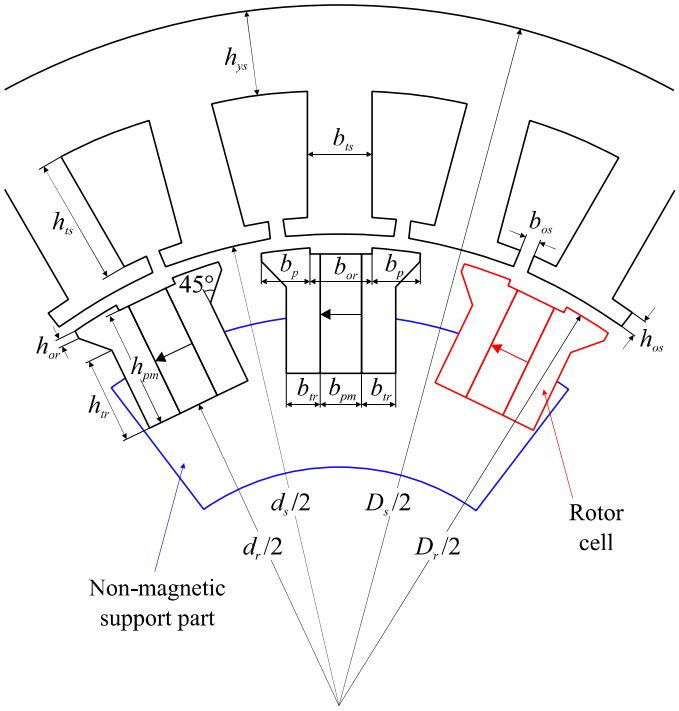


Fig. 3. A detail of a 28-pole, 24-slot RPMFS machine with main geometric design parameters [5].

Before assembling the simulation model in femm 4.2 software, the program checks the geometrical feasibility of the initialized parameters according to Table III. Geometrical feasibility implies that the initialized parameters correspond to a real machine geometry and that there is no overlapping of edges and no negative lengths [17]. If the initialized parameters pass the feasibility check, all stator and rotor dimensions are calculated in meters, respecting the topology shown in Fig. 3 and a finite element simulation model in femm 4.2 software is generated.

TABLE III
GEOMETRICAL FEASIBILITY CONDITIONS

Description	Mathematical formulation
The number of poles is even.	$\mathrm{mod}(2p, 2) = 0$
The number of slots is divisible by the number of phases.	$\mathrm{mod}(Q_s, m) = 0$
The number of slots is even for single-layer windings [18], [19].	$\mathrm{mod}(Q_s, 2) = 0$ for $n_{lay} = 1$
The number of slots per phase is divisible by $t = \gcd(Q_s, p)$ [18], [19].	$\mathrm{mod}(Q_s / m / t, 1) = 0$
Sum of stator slot opening and stator tooth width is less then stator slot pitch.	$b_{ts} + b_{os} < \tau_s$
Sum of stator tooth height and stator tooth tip height is less than difference of outer and inner stator radius.	$h_{ts} + h_{os} < (D_s - d_s)/2$
Sum of rotor tooth width and half of rotor permanent magnet width is less than rotor inner pole pitch.	$b_{tr} + b_{pm}/2 < \tau_{ir}$
Sum of rotor pole width and half of rotor slot opening width is less than rotor outer pole pitch.	$b_p + b_{or}/2 < \tau_{or}$
Rotor permanent magnet width is less than rotor slot opening width.	$b_{pm} < b_{or}$

B. Stator and Rotor Geometry

In order to assemble stator and rotor geometry, one stator slot (Fig. 4a) and one rotor cell (Fig. 4b) are constructed first. The stator slot is copied Q_s/t times and the copies are equally distributed over the angle $2\pi/t$, where t is the machine periodicity, defined as the greatest common denominator (gcd) between Q_s and p, as follows [13]:

$$t = \gcd(Q_s, p). \tag{1}$$

In a similar manner, the rotor cell is copied p/t times and the copies are again equally distributed over the angle $2\pi/t$. This means that the number of rotor poles and stator slots can be divided by their greatest common denominator in order to obtain the smallest segment of the machine that can be analyzed via symmetry [16]. For $t = 1$, the whole machine must be analyzed, while for $t > 1$, the machine can be divided in t segments and the results for the whole machine can be obtained by simulating only one out of t segments, reducing thereby the computational efforts.

After assembling the stator and rotor geometry, all stator slots are grouped (marked blue in Fig. 5) and all rotor cells are grouped (marked red in Fig. 5). For $t > 1$, end boundaries must be added to the stator (B2, B3, B14 and B15 in Fig. 5) and the rotor (B7, B8, B9 and B10 in Fig. 5) in order to enclose the areas that belong to the stator and rotor core. In order to enable the rotation of the rotor, four line segments are added to the model – two on the stator side of the air-gap (B4 and B13 in Fig. 5) and two on the rotor side of the air-gap (B6 and B11 in Fig. 5). These line segments are disconnected at the middle of the air-gap. Later on, when the rotor is rotated, the end nodes of these segments will be connected with arcs (B5 and B12 in Fig. 5) on each step of the simulation, i.e. for each analyzed rotor position.

After defining all the boundaries, the boundary conditions are imposed according to Table IV. A Dirichlet boundary condition, with zero value of magnetic vector potential ($A_z = 0$), is assigned to the stator outer boundary (B1 in Fig. 5), while (anti)periodic boundary conditions are assigned to appropriate pairs of boundaries from B2 to B15. A periodic boundary condition joins two boundaries together, whereas the boundary values on corresponding points of the two boundaries are set equal to each other [15]. In the case of an antiperiodic boundary condition, the boundary values on corresponding points of the two joint boundaries are made to be of equal magnitude but opposite sign [15]. Whether periodic or antiperiodic boundaries will be applied, depends on the number of rotor poles and on the value of machine periodicity t. If the number of rotor poles to be analyzed p/t is odd, antiperiodic boundary conditions should be used [16]. Otherwise, if p/t is even, periodic boundary conditions should be used instead [16].

Finally, the materials that will be used in the simulation are defined and assigned to appropriate enclosed areas in the model. The materials are chosen from the femm 4.2 material library [15] amongst which are air, iron, PM and conductor material, as is indicated in Fig. 5 and Table V.

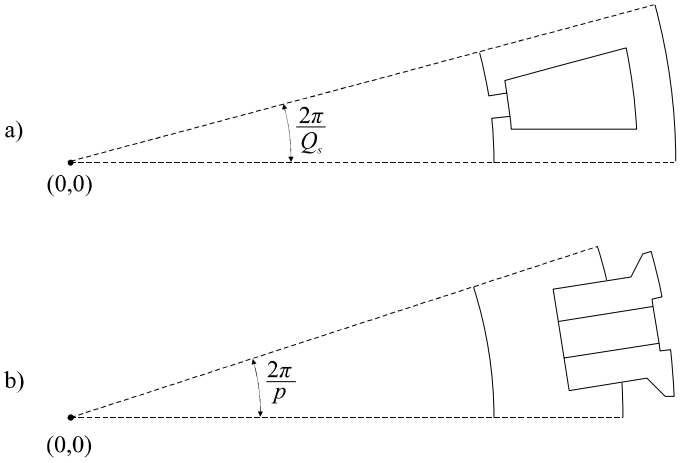


Fig. 4. a) Stator slot and b) rotor cell. The stator slot is copied Q_s/t times and the copies are equally distributed over the angle $2\pi/t$, where t is the machine periodicity. In a similar manner, the rotor cell is copied p/t times and the copies are again equally distributed over the angle $2\pi/t$ [5].

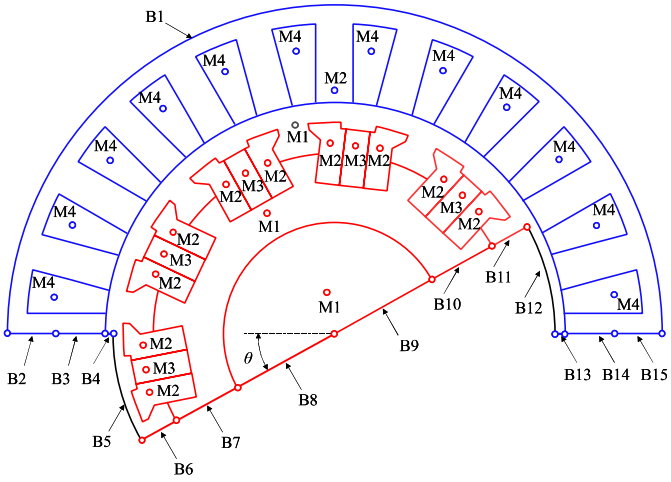


Fig. 5. Defining boundaries, boundary conditions and materials for an example 24-slot, 20-pole RPMFS machine. Only one half of the machine can be simulated in order to obtain results for the whole machine, because $t = \gcd(24,10) = 2$ [5].

TABLE IV
BOUNDARY CONDITIONS

Boundary	Boundary condition
B1	Dirichlet (Zero magnetic vector potential)
B2, B15	(Anti)periodic 1
B3, B14	(Anti)periodic 2
B4, B13	(Anti)periodic 3
B5, B12	(Anti)periodic 4
B6, B11	(Anti)periodic 5
B7, B10	(Anti)periodic 6
B8, B9	(Anti)periodic 7

TABLE V
MATERIALS

Material name	Material type
M1	Air
M2	Iron (e.g. M-19 Steel)
M3	Permanent magnet (e.g. NdFeB 32 MGOe)
M4	Conductor (e.g. Copper)

C. Stator Winding Layout

The function for assembling the stator winding is based on the construction of the so-called WDT (Winding Distribution Table), which is a winding diagram representation in matrix form [13]. Each row in the WDT corresponds to one machine phase, while the number of columns is equal to the number of slots per phase ($n_c = Q_s / m$), according to Table VI [13].

TABLE VI
ORDER OF THE WDT ELEMENTS [13]

	column 1	column 2	⋯	column n_c
row 1	1	2	⋯	n_c
row 2	$n_c + 1$	$n_c + 2$	⋯	$2n_c$
row 3	$2n_c + 1$	$2n_c + 2$	⋯	$3n_c$
⋮	⋮	⋮	⋱	⋮
row m	$(m\text{-}1)n_c + 1$	$(m\text{-}1)n_c + 2$	⋯	$m \cdot n_c$

The procedure for assembling the WDT is derived in [13], while only the key steps will be explained here. In the first step of the procedure, numbers are assigned to all stator slots. Starting from the first slot, the WDT is populated row by row, according to the progressive numbering illustrated in Table VI. The first slot number is assigned to the first element of the WDT. The second slot number is assigned to the WDT element whose distance is equal to p elements from the first one; the third slot number is assigned to the element whose distance is equal to p elements from the second one, and so on. When the element at position $Q_s = m \cdot n_c$ of the WDT is counted, the counting continues from the first element of the WDT. If the count ends in a filled cell, the adjacent empty cell is filled with the counted slot number. The procedure continues until the WDT is completely populated by stator slot numbers.

In order to visualize all positive and all negative phasors of the same phase in the same row, the WDT is further modified, depending on the phase number. For radially symmetrical (normal) polyphase systems, the last $\lfloor n_c / 2 \rfloor$ WDT columns are shifted up by [13]:

$$\gamma = \begin{cases} \dfrac{m-1}{2}, \text{ for odd } m \\ \dfrac{m}{2} - 1, \text{ for even } m \end{cases} \tag{2}$$

rows (see Fig. 6a). In addition, a minus sign is added to the shifted columns, so that the coil sides with negative phasors can be identified [13]. For reduced polyphase systems, the rows are not shifted, but the second and third quadrants in Fig. 6b are swapped and the rows are reordered as in Table VII [13]. The sign of slot numbers in the third and fourth quadrant are then changed to account for negative coil sides [13].

TABLE VII
REORDERING WDT ROWS IN REDUCED SYSTEMS [13]

	1	2	⋯	n_c			1	2	⋯	n_c
1	⋯	⋯	⋯	⋯		1	⋯	⋯	⋯	⋯
2	⋯	⋯	⋯	⋯		$m/2 + 1$	⋯	⋯	⋯	⋯
⋮	⋮	⋮	⋮	⋮		2	⋯	⋯	⋯	⋯
$m/2$	⋯	⋯	⋯	⋯	⇒	$m/2 + 2$	⋯	⋯	⋯	⋯
$m/2 + 1$	⋯	⋯	⋯	⋯		⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮		$m/2$	⋯	⋯	⋯	⋯
m	⋯	⋯	⋯	⋯		m	⋯	⋯	⋯	⋯

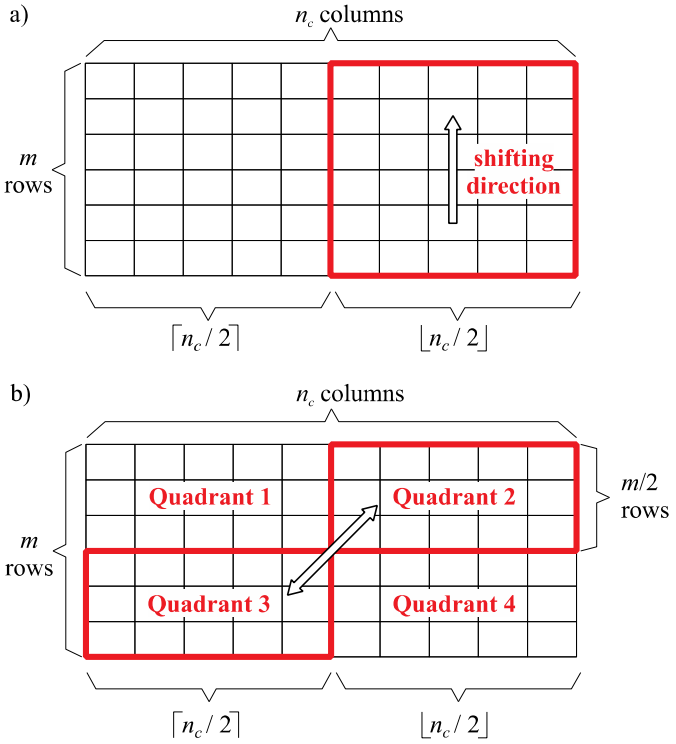


Fig. 6. Modification of the WDT for a) radially symmetrical (normal) and b) reduced polyphase systems [5].

Reduced systems, whose number of phases is not a power of two, are composed of m_g groups of m_u-phase systems, shifted by and angle π / m, where m_g is the greatest prime factor of m and $m_u = m / m_g$ [13]. A typical example would be a reduced six phase system, which consists of $m_g = 2$ three-phase systems shifted by an angle of $\pi / 6$ radians (see Fig. 20). The even groups of WDT rows (third and fourth row, seventh and eighth row etc.) must be multiplied by –1 in order to make these systems radially symmetrical and to avoid the use of a neutral line [13]. In the case of single-layer windings ($n_{lay} = 1$), the WDT elements are referred to phasors associated to each slot, i.e. to each coil side [13]. In double-layer windings ($n_{lay} = 2$), the WDT elements are referred to one coil side, whereas the second coil side position is defined by the coil pitch given as a number of stator slots [20]:

$$y_c = \text{round}\left(\frac{Q_s}{2p}\right). \tag{3}$$

In order to demonstrate this procedure, the WDT for a three-phase, 24-slot, 20-pole RPMFS machine is assembled and shown as Table VIII. From Table VIII, the stator winding layout for the case of a single-layer winding is formed according to Fig. 7a, where only one half of the machine is shown.

TABLE VIII
WDT FOR RPMFS MACHINE SHOWN IN FIG. 7 [5]

1	13	6	18	-7	-19	-12	-24
9	21	2	14	-3	-15	-8	-20
5	17	10	22	-11	-23	-4	-16

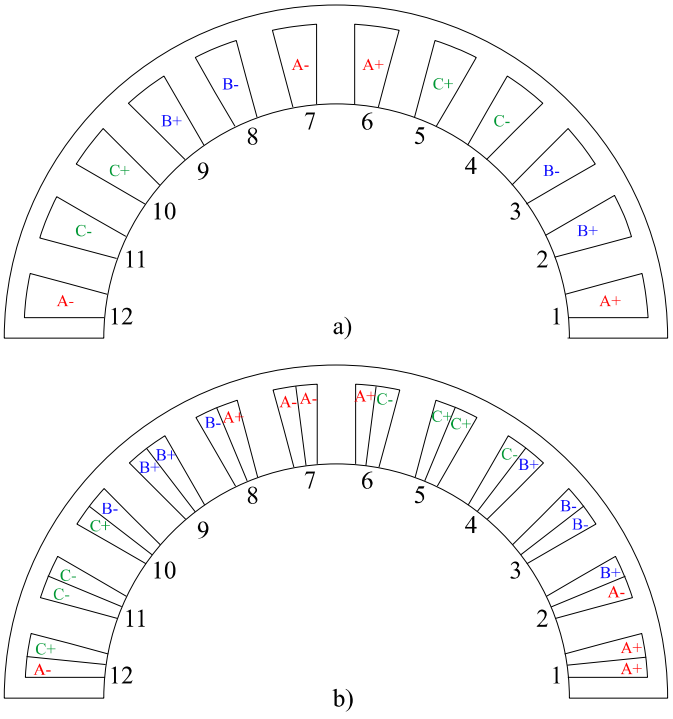


Fig. 7. Stator winding layout for an example three-phase, 24-slot, 20-pole RPMFS machine with a) single-layer and b) double-layer winding with a coil pitch of one slot ($y_c = 1$) [5].

Form Fig. 7a it can be seen that, for example, coil sides in slots 1, 6, 7 and 12 belong to phase A winding. Positive phase A current exists in coil sides located in slots 1 and 6, because these slot numbers are denoted as positive in Table VIII. Negative phase A current exists in coil sides located in slots 7 and 12, because these slot numbers are denoted as negative in Table VIII. The same WDT is used when assembling a double-layer winding. From Fig. 7b it can be seen that, for the case of a double-layer winding, one coil side in each of the slots 1, 6, 7 and 12 belongs to phase A winding. Because the coil pitch for this example is $y_c = 1$, one coil side in each of the slots $1 + y_c = 2$, $6 + y_c = 7$, $7 + y_c = 8$ and $12 + y_c = 13$ also belongs to phase A, whereas the sign of the current is opposite to that in coil sides located in slots 1, 6, 7 and 12, respectively. The same analysis can be carried out for phases B and C.

III. Calculating RPMFS Machine Parameters

In this Section, the process of calculating the circuit parameters of the assembled RPMFS machine model will be explained. Based on the methodology presented in [21], all parameters are first calculated assuming one turn per stator coil. After obtaining the values of all circuit parameters for one turn per coil, the corrected number of turns per coil N_c is calculated considering the fact that the sum of the *d*-axis and *q*-axis back electromotive forces and all voltage drops at rated speed *n* and rated current *I* has to equal the rated voltage *U*. All circuit parameters are then recalculated using the newly obtained number of turns per coil. In the remainder of this Section the values of parameters which are calculated for one turn per coil will be denoted with subscript 0, while their recalculated final values won't be denoted with any subscript.

A. Machine Inductances and Flux Linkages

In order take the iron saturation at rated conditions into account, machine inductances and flux linkages are obtained by employing the frozen permeability method in femm 4.2 software. The frozen permeability method, which is described in [21] and [22], implies that several magnetostatic simulations are performed with constant values of iron permeability in the nodes of the finite element mesh. These permeabilities are determined for the rated operating point and are used in order to preserve information about the iron saturation at rated conditions. After "freezing" the permeability in this manner, the problem becomes linear and the circuit parameters can be determined one at a time, using the principle of superposition.

In [5]-[11] it has been shown that RPMFS machines are supplied with sinusoidal currents and that they have negligible reluctance torque, which means that maximum torque for given amplitudes of phase currents is obtained with zero *d* axis current. Thus, when simulating the rated operation, *d* axis current is set to zero, while *q* axis current is set to rated current. As the number of turns per coil N_c and the RMS value of rated stator current *I* are not known, the number of ampere-turns per stator coil is calculated first [21]:

$$N_c I = \frac{k_{Cu} J A_s}{n_{lay}}, \tag{4}$$

where the slot area is determined from stator core dimensions:

$$A_s = \frac{\pi}{4Q_s}\left[\left(D_s - 2h_{ys}\right)^2 - \left(d_s + 2h_{os}\right)^2\right] - b_{ts}h_{ts}. \tag{5}$$

In (4) it is assumed that there is only one current path, but in applications where the rated current is specified in addition to the rated voltage, a method presented in [23] can be used for further fine tuning of the number of turns and number of parallel paths. The separation of the number of turns per coil N_c and of the RMS value of rated stator current *I* doesn't influence the results obtained for the magnetic field, meaning that magnetostatic simulations can be performed assuming $N_c = 1$.

Before calculating any parameters, the position of the *d* axis of the PMs relative to phase A axis must be determined. First, stator phase currents are set to zero and PMs are magnetized. Next, the RPMFS model is analyzed using femm 4.2 magnetics solver [14], [15] and the solution for *z* component of magnetic vector potential is obtained by solving Poisson's differential equation in the *xy* plane [4]:

$$-\frac{\partial}{\partial x}\left(\frac{1}{\mu_r}\frac{\partial A_z}{\partial x}\right) - \frac{\partial}{\partial y}\left(\frac{1}{\mu_r}\frac{\partial A_z}{\partial y}\right) = \mu_0 J_z. \tag{6}$$

In (6), μ_0 is the permeability of free space, μ_r is the relative permeability, J_z is the *z* component of current density vector, while A_z is the *z* component of magnetic vector potential. From the solution for A_z, the flux linkage for each phase winding is calculated [4]:

$$\psi_k = \frac{N_k l_s}{S_k}\left(\int_{\Omega_k^+} A_z d\Omega - \int_{\Omega_k^-} A_z d\Omega\right), \ (k = 1, 2, \ldots m). \tag{7}$$

In (7), N_k is the number of turns in phase k winding, l_s is the stator stack length, S_k is the cross-sectional area of all coil sides belonging to phase k winding, while Ω_k^+ and Ω_k^- represent the areas with positive and negative phase k current. Assuming that the d axis of the PMs is aligned with phase A axis, the d and q axis flux linkages are calculated as [24]:

$$\psi_d = \frac{2}{m}\sum_{k=1}^{m}\psi_k \cos\left[(k-1)\frac{2\pi}{m}\right], \tag{8}$$

$$\psi_q = \frac{2}{m}\sum_{k=1}^{m}\psi_k \sin\left[(k-1)\frac{2\pi}{m}\right], \tag{9}$$

where the amplitude invariant form of the Park transformation is employed. After calculating d and q axis flux linkages, the electrical angle α between stator phase A axis and PM d axis is obtained from Fig. 8 as [5]:

$$\alpha = \text{atan}\left(\frac{\psi_q}{\psi_d}\right). \tag{10}$$

For given values of currents i_d and i_q, stator phase currents are calculated as [24]:

$$\begin{aligned} i_k = {} & i_d \cos\left[\theta-(k-1)\frac{2\pi}{m}\right]+ \\ & -i_q \sin\left[\theta-(k-1)\frac{2\pi}{m}\right],\ (k=1,2,\ldots m). \end{aligned} \tag{11}$$

With initial rotor position set to $\theta = \alpha$ and with $i_d = 0$, the stator winding is supplied with following currents [5], [24]:

$$i_k = -\sqrt{2}I\sin\left[\alpha-(k-1)\frac{2\pi}{m}\right],\ (k=1,2,\ldots m), \tag{12}$$

where I is the RMS value of rated current, which is obtained from (4) assuming $N_c = 1$. With these values of stator phase currents and with PMs magnetized, another nonlinear magnetostatic simulation is performed in order to obtain the values of permeabilities in the nodes of the finite element mesh which correspond to rated RPMFS machine operation (Fig. 9). The values of "frozen" permeabilities are used to conduct three linear magnetostatic simulations from which the parameters Ψ_{pmd0}, Ψ_{pmq0}, L_{d0}, L_{q0} and $L_{qd0} = L_{dq0}$ are determined.

The first linear simulation is conducted by setting the stator currents to zero and leaving the PMs magnetized. The flux linkages of all phase windings are then calculated using the obtained solution for magnetic vector potential (Fig. 10), according to (6), and the d and q axis flux linkages are then calculated as [24]:

$$\psi_{pmd0} = \frac{2}{m}\sum_{k=1}^{m}\psi_k \cos\left[\alpha-(k-1)\frac{2\pi}{m}\right], \tag{13}$$

$$\psi_{pmq0} = -\frac{2}{m}\sum_{k=1}^{m}\psi_k \sin\left[\alpha-(k-1)\frac{2\pi}{m}\right]. \tag{14}$$

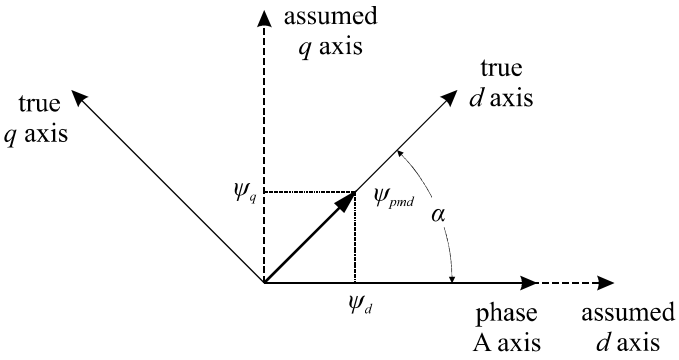


Fig. 8. Determining the relative position of phase A axis and PM d-axis.

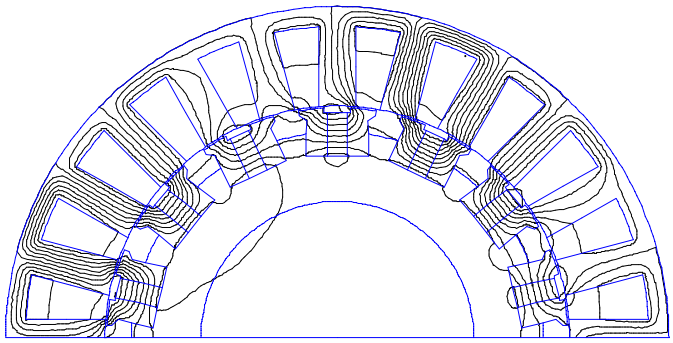


Fig. 9. Contour plot of magnetic vector potential for rated operating point of an example three-phase, 24-slot, 28-pole RPMFS machine, used to obtain "frozen" permeabilities for subsequent magnetostatic simulations.

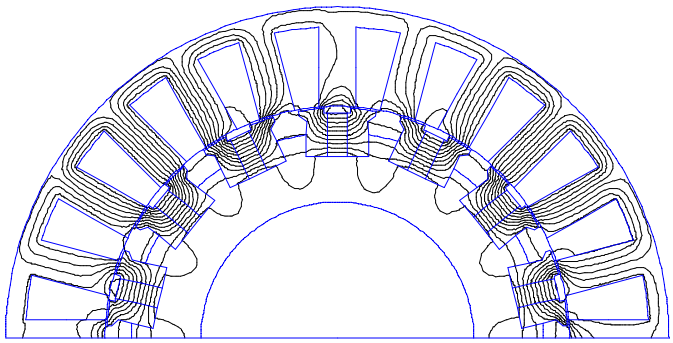


Fig. 10. Contour plot of magnetic vector potential for an example three-phase, 24-slot, 28-pole RPMFS machine with stator current set to zero and with PMs magnetized, used to obtain saturated values of Ψ_{pmd0} and Ψ_{pmq0}.

The flux linkage $\Psi_{pmd0} = \psi_{pmd0}/\sqrt{2}$ represents the RMS value of d axis flux linkage due to permanent magnets only, while $\Psi_{pmq0} = \psi_{pmq0}/\sqrt{2}$ is RMS value of q axis flux linkage due to PMs only, both calculated for one turn per stator coil. Although Ψ_{pmq0} is expected to be zero, because the flux of the PMs is expected to be aligned with d axis, Ψ_{pmq0} will nevertheless have a small non-zero value for the RPMFS machine, which is a consequence of the cross-saturation effect [21].

The second linear simulation is conducted by demagnetizing the PMs and setting the q axis current to zero ($i_q = 0$), while the d axis current can be set to an arbitrary value i_d, resulting in following stator currents [24]:

$$i_k = i_d \cos\left[\alpha-(k-1)\frac{2\pi}{m}\right],\ (k=1,2,\ldots m). \tag{15}$$

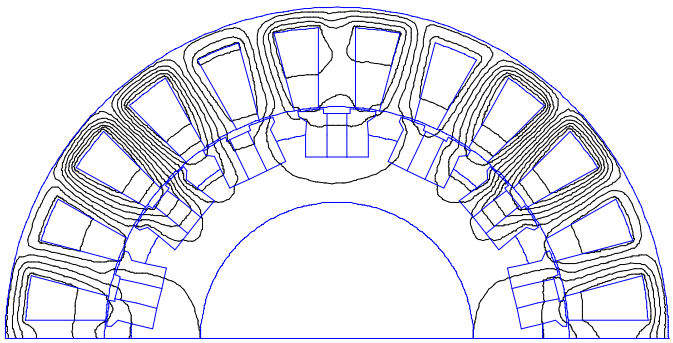


Fig. 11. Contour plot of magnetic vector potential for an example three-phase, 24-slot, 28-pole RPMFS machine with stator q-axis current set to zero and with PMs demagnetized, used to obtain saturated values of L_{d0} and L_{qd0}.

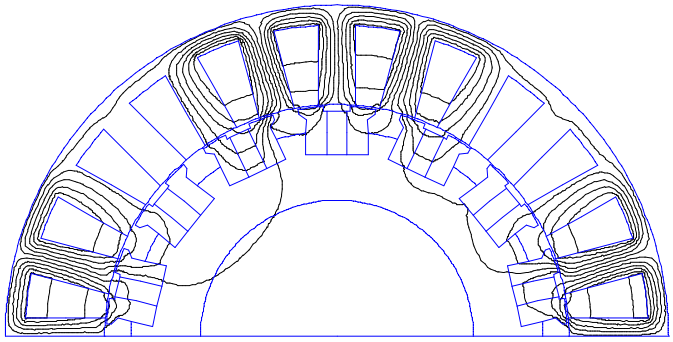


Fig. 12. Contour plot of magnetic vector potential for an example three-phase, 24-slot, 28-pole RPMFS machine with stator d-axis current set to zero and with PMs demagnetized, used to obtain saturated values of L_{q0} and L_{dq0}.

The corresponding flux linkages of all phase windings are then calculated using the obtained solution for magnetic vector potential (Fig. 11), according to (6), and flux linkages ψ_{d0} and ψ_{q0} are calculated as in (13) and (14). The saturated values of the d axis inductance and the cross-saturation inductance for one turn per stator coil are calculated as [21]:

$$L_{d0} = \frac{\psi_{d0}}{i_d}, \quad L_{qd0} = \frac{\psi_{q0}}{i_d}. \tag{16}$$

Finally, the last linear simulation is conducted by leaving the PMs demagnetized and setting the d axis current to zero ($i_d = 0$), while the q axis current can be set to an arbitrary value i_q, resulting in following stator currents [24]:

$$i_k = -i_q \sin\left[\alpha - (k-1)\frac{2\pi}{m}\right], \ (k = 1, 2, \ldots m). \tag{17}$$

The corresponding flux linkages of all phase windings are again calculated using the obtained solution for magnetic vector potential (Fig. 12), according to (6), and flux linkages ψ_{d0} and ψ_{q0} are calculated as in (13) and (14). The saturated values of the q axis inductance and the cross-saturation inductance for one turn per stator coil are calculated as [21]:

$$L_{q0} = \frac{\psi_{q0}}{i_q}, \quad L_{dq0} = \frac{\psi_{d0}}{i_q}. \tag{18}$$

It should be noted that $L_{qd0} = L_{dq0}$ [21] and $L_{d0} \approx L_{q0}$ [9], which can be confirmed by comparing the results of the last two linear simulations. The end winding leakages are neglected in this calculation, which is in most cases justified because of short end windings of the RPMFS machine. However, for some combinations of stator slots, poles and phases, which may result in distributed, rather than tooth wound stator windings, this assumption has to be tested first.

B. Stator Winding Resistance

The stator winding resistance for one turn per coil is calculated as [21]:

$$R_{s0} = \rho_{Cu75} \frac{n_{lay}^2 l_c Q_s}{m k_{Cu} A_s}, \tag{19}$$

where $\rho_{Cu75} = 0{,}0216\ \Omega\text{mm}^2/\text{m}$ is the resistivity of copper at temperature 75 °C and $l_c = 2(l_s + l_{ew})$ is the coil length. The end winding length is calculated assuming semicircular end windings and taking the coil pitch y_c into account by following equation [20]:

$$l_{ew} = \frac{\pi}{4}\left(\tau_{s1/2} + b_{ts}\right) + 1{,}8\tau_{s1/2}\left(y_c - 1\right), \tag{20}$$

where $\tau_{s1/2} = \pi(D_s + h_{st})/Q_s$ is the slot pitch measured at half of the stator tooth height.

C. Number of Turns per Coil

The number of turns per coil N_c is calculated considering the fact that the sum of the d-axis and q-axis back electromotive forces and all voltage drops at rated speed n and rated current I has to be equal to the rated voltage U. The phasor diagram for the rated operating point of the RPMFS machine is shown in Fig. 13, where currents, voltages and flux linkages are represented by their RMS values. It is assumed that the RPMFS machine is vector controlled with $I_d = 0$ and $I_q = I$, where I is the RMS value of rated current. The d and q axis components of rated stator voltage are [25]:

$$U_d = E_d + X_q I_q = \omega \Psi_{pmq} + \omega L_q I_q, \tag{21}$$

$$U_q = E_q + X_{dq} I_q + R_s I_q = \omega \Psi_{pmd} + \omega L_{dq} I_q + R_s I_q, \tag{22}$$

where $E_d = \omega \cdot \Psi_{pmq}$, $E_q = \omega \cdot \Psi_{pmd}$, $X_q = \omega \cdot L_q$ and $X_{dq} = \omega \cdot L_{dq}$. The angular frequency ω corresponds to rated rotor speed n.

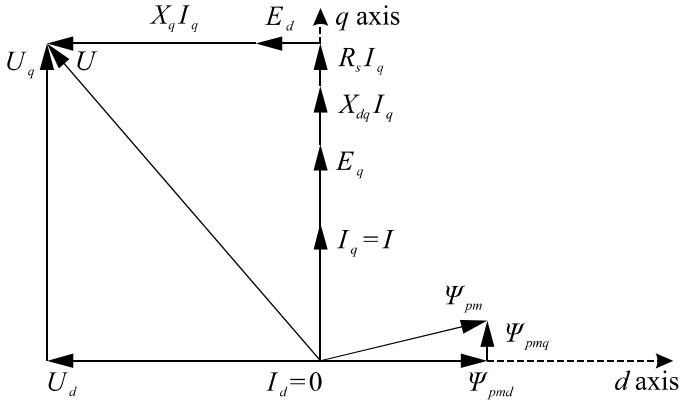


Fig. 13. Phasor diagram of the RPMFS machine which is vector controlled with $I_d = 0$ and $I_q = I$. Cross-saturation is modeled by X_{dq}, Ψ_{pmq} and E_d.

As the flux linkages are proportional to the number of turns per coil, while inductances and resistances are proportional to the square of the number of turns per coil, following equations are valid [21]:

$$\begin{aligned} \Psi_{pmd} &= N_c \Psi_{pmd0}, \\ \Psi_{pmq} &= N_c \Psi_{pmq0}, \\ L_d &= N_c^2 L_{d0}, \\ L_q &= N_c^2 L_{q0}, \\ L_{dq} &= N_c^2 L_{dq0}, \\ R_s &= N_c^2 R_{s0}. \end{aligned} \tag{23}$$

By substituting (23) into (21) and (22), we obtain:

$$U_d = \omega N_c \Psi_{pmq0} + \omega N_c L_{q0} N_c I_q , \tag{24}$$

$$U_q = \omega N_c \Psi_{pmd0} + \omega N_c L_{dq0} N_c I_q + N_c R_{s0} N_c I_q . \tag{25}$$

Taking into account that, for the amplitude invariant form of the Park transformation, following equations are valid:

$$N_c I_q = N_c I , \tag{26}$$

$$U = \sqrt{U_d^2 + U_q^2} , \tag{27}$$

we finally get the expression for calculating the number of turns per coil for given value of rated angular frequency ω, RMS value of rated voltage U and RMS value of rated ampere-turns per stator coil $N_c I$:

$$N_c = \frac{U/\omega}{\sqrt{\left(\Psi_{pmd0} + L_{dq0} N_c I + \frac{R_{s0}}{\omega} N_c I\right)^2 + \left(\Psi_{pmq0} + L_{q0} N_c I\right)^2}} . \tag{28}$$

After calculating the number of coils per turn N_c in this manner, all circuit parameters are recalculated according to (23). Also, the RMS value of rated stator current I and the number of turns per coil N_c are separated according to the value of the rated ampere-turns per stator coil $N_c I$, which is derived from (4). It should be emphasized that the equations used in the analysis presented in this Section are based on the amplitude invariant form of the Park transformation.

IV. Calculating RPMFS Machine Torque and EMF

The torque and EMF waveforms are derived by rotating the rotor in steps $\Delta\theta$ over an angle $\theta_{\max}$. For each rotor position, the simulated machine segment is analyzed using femm 4.2 magnetics solver [15], [16] and the solution for z component of magnetic vector potential is obtained by solving (6). From the solution for A_z, the flux linkages are calculated for all phase windings according to (7) and torque and EMF is calculated for each rotor position.

A. Torque Waveform

The electromagnetic torque acting upon the rotor of the RPMFS machine is calculated by employing the weighted stress tensor volume integral [15], [16], according to following equation [22]:

$$T_e = \frac{k_{Fe} l_s}{\mu_0} \int_0^{2\pi} r^2 B_n B_t d\theta , \tag{29}$$

where μ_0 is the permeability of free space, k_{Fe} is the iron stacking factor, l_s is the stator laminations axial length, r is the radius of the integration path, and B_n and B_t are the normal and tangential flux density components in the air gap, respectively. In femm 4.2 software, the torque is calculated by selecting all rotor blocks (marked red in Fig. 5) and by evaluating the integral (29) for each rotor position. The values of torque for each rotor position are then stored in an array for the purpose of post processing.

The above proposed method for torque calculation is used to obtain the torque waveform, from which the average torque and the torque ripple can both be derived. If torque ripple is not of interest, a more computationally efficient method can be used in order to calculate just the average value of torque. Based on the derivations in Section III, the average value of rated electromagnetic torque can be calculated as [21], [22]:

$$T_{avg} = 3p\left(\Psi_d I_q - \Psi_q I_d\right) = 3p\, \Psi_d I , \tag{30}$$

where the RMS value of d axis stator flux linkage is:

$$\Psi_d = \Psi_{pmd} + L_d I_d + L_{dq} I_q = \Psi_{pmd} + L_{dq} I , \tag{31}$$

and where $I_d = 0$ and $I_q = I$ is assumed. For some applications, such as torque density optimization of RPMFS machines, the second approach, based on just a few magnetostatic simulations, can be used because of its computational efficiency and acceptable accuracy. However, for applications where the torque ripple has to be optimized, the first approach, based on the torque waveform obtained from a series of magnetostatic simulations, has to be used.

B. EMF Waveform

The value of induced EMF in phase k is calculated by applying Faradays law for each rotor position θ during the simulation:

$$e_k(\theta) = \frac{p\pi}{30} n \frac{\psi_k(\theta) - \psi_k(\theta - \Delta\theta)}{\Delta\theta}, \ (k = 1, 2, \ldots m), \tag{32}$$

where n is the value of rotor speed in rpm. The phase flux linkages in (32) are calculated according to (7). The values of phase EMFs for each rotor position are again stored in an array for the purpose of post processing.

V. Presenting The Results

The outputs of the program are plots of torque and phase EMF waveforms. In the post processing part of the program, the average value of machine torque and the value of torque ripple are calculated and shown as data on these plots. The program also performs harmonic analysis of EMF waveforms and calculates the RMS value of the fundamental harmonic and the total harmonic distortion (THD) of the induced phase EMF. Machine output parameters are printed to a text file.

In order to demonstrate the form of the results, three RPMFS machines with different numbers of slots, poles and phases are simulated, according to input parameters given in Table IX. All other input parameters are adopted according to Table X and they have the same values for all three analyzed RPMFS machines. It should be noted that these machine designs are in no way optimized and that they are used for demonstration purposes only. A relatively small value of the angular step $\Delta\theta$ is adopted in order to get smooth torque and EMF waveforms (accurate value of torque ripple and EMF harmonics), but a higher value could be adopted without significant loss of accuracy in calculated average torque. It should be noted that higher values of angular step $\Delta\theta$ would result in fewer magnetostatic simulations and, thus, in shorter overall computation time. This is important when the program is used as a part of an iterative optimization procedure, where the goal is to maximize the average torque for given machine volume (volume torque density). The mesh is automatically generated for each rotor position according to femm 4.2 software default settings [15], [16], which was shown to be appropriate for machine design purposes. The values of air-gap length, stator outer diameter and stator lamination stack length are adopted from [7] and [8]. The PM material used in simulations is N36Z2G, with data: $H_c = 846625$ A/m; $\mu_r = 1.165$; $B_r = \mu_r \cdot \mu_0 \cdot H_c = 1.24$ T [7], [26].

TABLE IX
INPUT PARAMETERS FOR THREE RPMFS MACHINES

Parameter name	Symbol	M1	M2	M3
Number of stator slots	Q_s	24	30	24
Number of rotor poles	$2p$	20	28	28
Number of stator winding phases	m	3	5	6
Number of stator winding layers	n_{lay}	1	1	2

TABLE X
COMMON INPUT PARAMETERS

Parameter name	Symbol	Value
Angular step in electrical degrees	$p \cdot \Delta\theta$	4
Total angular displacement of rotor in electrical degrees	$p \cdot \theta_{\max}$	360
Rated RMS value of phase voltage, V	U	230
Rated RMS value of current density in the conductors, A/mm^2	J	5
Slot fill factor	k_{Cu}	0.68
Rotor speed, rpm	n	500
Air-gap length, mm	δ_g	0.73
Stator outer diameter, mm	D_s	269
Stator stack length, mm	l_s	83.56
Ratio of inner and outer stator diameter	d_s / D_s	0.7
Ratio of stator tooth width to slot pitch	b_{ts} / τ_s	0.6
Ratio of stator slot opening width to slot pitch	b_{os} / τ_s	0.4
Ratio of stator tooth height to difference of outer and inner stator radius	$2h_{ts} / (D_s - d_s)$	0.8
Ratio of stator tooth tip height to difference of outer and inner stator radius	$2h_{os} / (D_s - d_s)$	0
Ratio of inner and outer rotor diameter	d_r / D_r	0.7
Ratio of rotor tooth width to inner pole pitch	b_{ir} / τ_{ir}	0.5
Ratio of PM width to rotor inner pole pitch	b_{pm} / τ_{ir}	0.5
Ratio of slot opening width to outer pole pitch	b_{or} / τ_{or}	0.5
Ratio of pole width to rotor outer pole pitch	b_p / τ_{or}	0.5
Ratio of tooth tip height to difference of outer and inner rotor radius	$2h_{or} / (D_r - d_r)$	0.1

The contour plots of magnetic vector potential for all three analyzed machines are shown in Fig. 14, 15 and 16, while the output parameters for all three machines are given in Table XI. The efficiency of the machines in Table XI is calculated by taking the copper losses into account, whereas the iron and mechanical losses are neglected, which must be reconsidered for some applications. The power factor is calculated by taking the voltage harmonics into account, while the currents are sinusoidal. In Table XI it can be seen that all three machines develop approximately the same average torque. This is mainly due to the same values of machine volume, current density in the conductors and approximately the same values of flux densities. The main difference between the machines is the torque ripple, which depends on the slot/pole combinations, and it is highest for machine M1. In Table XI it can also be verified that $L_d \approx L_q$ for all three designs, and that the cross-saturation parameters L_{dq} and Ψ_{pmq} have small negative values.

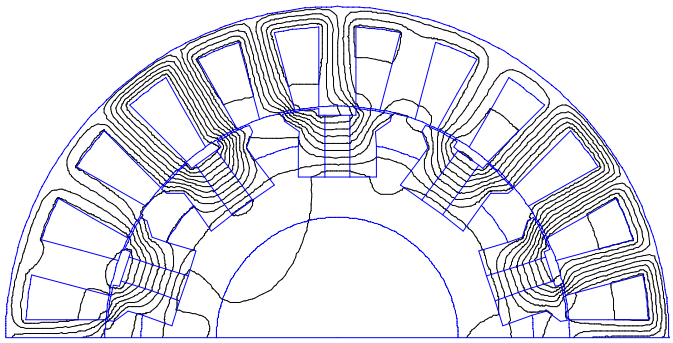


Fig. 14. Contour plot of magnetic vector potential for rated operation of machine M1 ($Q_s = 24$, $2p = 20$, $m = 3$, $n_{lay} = 1$).

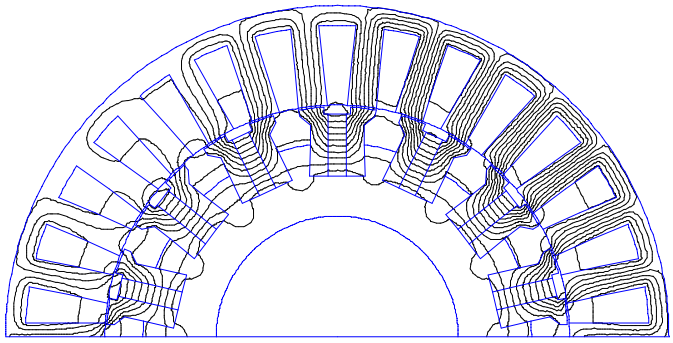


Fig. 15. Contour plot of magnetic vector potential for rated operation of machine M2 ($Q_s = 30$, $2p = 28$, $m = 5$, $n_{lay} = 1$).

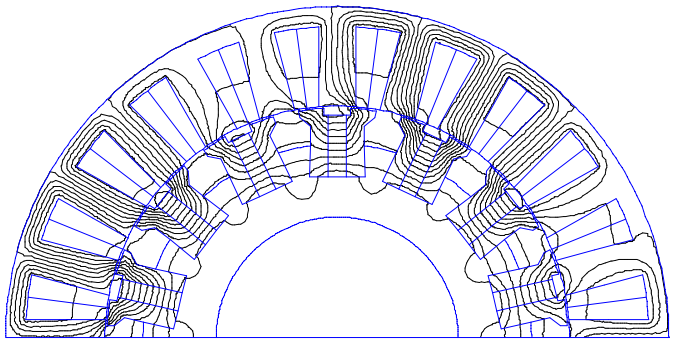


Fig. 16. Contour plot of magnetic vector potential for rated operation of machine M3 ($Q_s = 24$, $2p = 28$, $m = 6$, $n_{lay} = 2$).

TABLE XI
OUTPUT PARAMETERS FOR THREE RPMFS MACHINES

Parameter name	Symbol	M1	M2	M3
Mechanical output power, kW	P	10.5	11.2	11.3
RMS value of phase current, A	I	21	13.5	11.8
Power factor	PF	0.81	0.80	0.75
Efficiency	η	0.89	0.90	0.93
Average torque, Nm	T_{avg}	201	213	216
Torque ripple, %	T_{ripple}	7.53	1.08	2.68
Voltage harmonic distortion, %	$THD_{\%}$	12.43	9.98	4.12
Number of turns per coil	N_c	74	92	66
Stator winding resistance, Ω	R_s	1 Ω	1.3	1.1
d axis inductance, mH	L_d	14.3	16.7	20.8
q axis inductance, mH	L_q	14.0	16.1	20.5
Cross-saturation inductance, mH	L_{dq}	-0.6	-0.7	-0.8
d axis PM flux, mWb	Ψ_{pmd}	330	234	227
Cross- saturation PM flux, mWb	Ψ_{pmq}	-41	-30	-36
Tooth flux denisty, T	B_{ts}	1.85	1.89	1.60
Yoke flux density, T	B_{ys}	1.71	1.28	1.31

The value of average torque presented in Table XI is calculated by solving the weighted stress tensor volume integral in femm 4.2 software for each rotor position and by calculating the mean value for all rotor positions. It is interesting to compare this result with the one obtained by inserting the values of parameters Ψ_{pmd} and L_{dq} in (30) and (31). For example, this calculation for machine M1 yields the following result:

$$T_{avg} = 3p\left(\Psi_{pmd} I + L_{dq} I^2\right) = \\ = 3 \cdot 10 \cdot \left(0.33 \cdot 21 - 0.0006 \cdot 21^2\right) \approx 200 \text{ Nm}, \tag{33}$$

which is very close to the value given in Table XI. This means that just the parameters Ψ_{pmd} and L_{dq} have to be determined by two magnetostatic simulations and then the average torque can be calculated analytically with good accuracy. The torque waveforms for all three machines are shown in Fig. 17, where the results from table XI can be verified. The phase EMF waveforms for all three analyzed machines are shown in Fig. 18, 19 and 20. It can be concluded that all three machines have radially symmetrical stator windings.

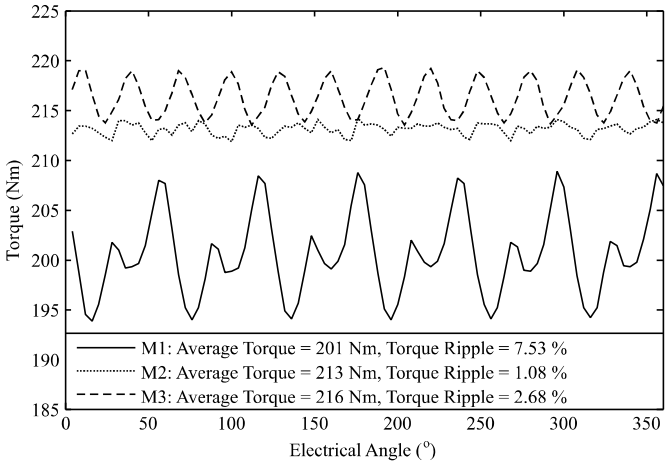


Fig. 17. Torque vs. electrical angle for analyzed RPMFS machines. Machine M1 has the lowest average value of torque and, at the same time, the highest value of torque ripple.

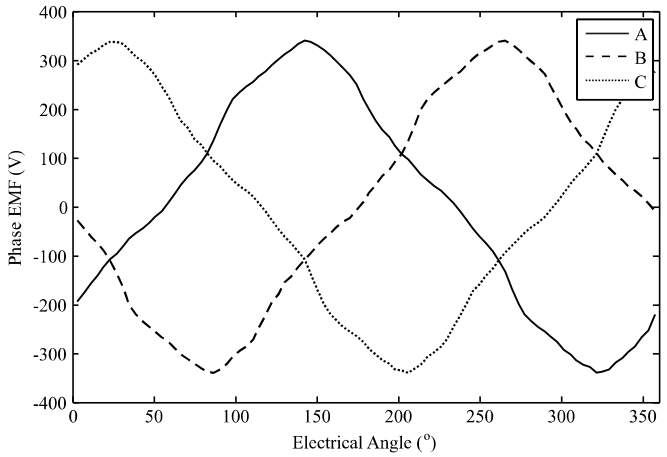


Fig. 18. Phase EMF vs. electrical angle for rated operation of machine M1 (Fundamental harmonic of phase EMF = 213.8 V, $THD_{\%}$ = 12.43 %).

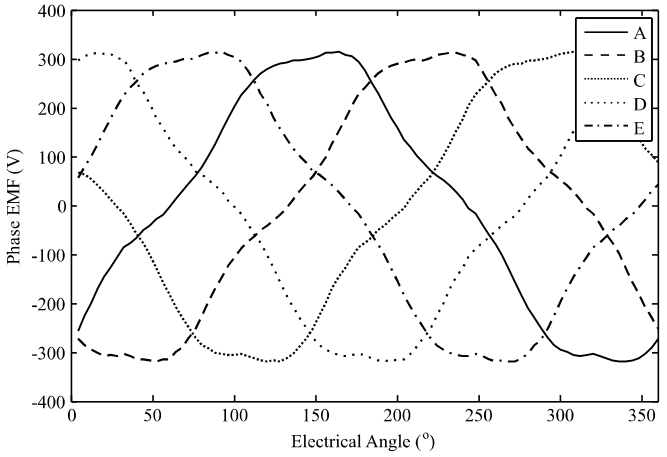


Fig. 19. Phase EMF vs. electrical angle for rated operation of machine M2 (Fundamental harmonic of phase EMF = 217.7 V, $THD_{\%}$ = 9.98 %).

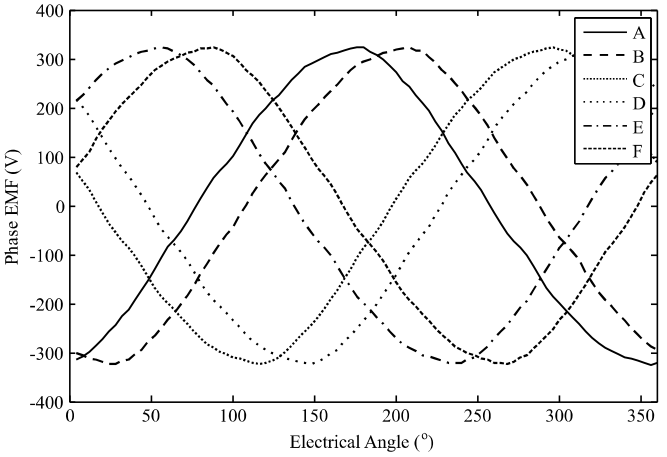


Fig. 20. Phase EMF vs. electrical angle for rated operation of machine M3 (Fundamental harmonic of phase EMF = 223.5 V, $THD_{\%}$ = 4.12 %). The phase EMFs for machine M3 are unevenly spaced in time, which is due to the fact that the stator winding is a reduced six-phase winding. The reduced six-phase system consists of two three-phase systems shifted by an angle of $\pi/6$ radians, whereas the first three-phase system consists of phases A, C and E, and the second three-phase system consists of phases B, D and F.

VI. CONCLUSION

The methodology for FE based design of RPMFS machines was presented in this paper, along with the corresponding application program, coded in Octave software FEMM toolbox. Guidelines for assembling the stator and rotor geometry, the stator winding layout, as well as calculation techniques for the machine circuit parameters, torque and EMF waveforms were developed and thoroughly explained respecting the procedures employed in the literature. The developed program enables fast and efficient analysis of RPMFS machines with different numbers of stator slots, stator phases, rotor poles and overall different dimensions. While the methodology presented in this paper is not restricted to RPMFS machines only, the program is intended to be used for geometry optimization of the RPMFS machine, with the aim of achieving maximum torque volume density and minimum torque ripple.

REFERENCES

[1] G. Bramerdorfer, J. A. Tapia, J. J. Pyrhönen and A. Cavagnino, "Modern Electrical Machine Design Optimization: Techniques, Trends, and Best Practices," *IEEE Trans. Ind. Electron.,* vol. 65, no. 10, pp. 7672 - 7684, Feb. 2018.

[2] Y. Duan and D. M. Ionel, "A Review of Recent Developments in Electrical Machine Design Optimization Methods With a Permanent-Magnet Synchronous Motor Benchmark Study," *IEEE Trans. Ind. Appl.,* vol. 49, no. 3, pp. 1268 - 1275, Mar. 2013.

[3] J. Pyrhönen, T. Jokinen and V. Hrabevcova, *Design of Rotating Electrical Machines*, Wiltshire: John Wiley & Sons, 2008.

[4] S. Salon, *Finite Element Analysis of Electrical Machines*, Troy, New York: Springer, 1995.

[5] Đ. Lekić and S. Vukosavić, "Program for Finite Element Based Design of Rotor Permanent Magnet Flux Switching Machine," in *2018 International Symposium on Industrial Electronics (INDEL)*, Banja Luka, Bosnia and Herzegovina, pp. 1-7, 1-3 Nov. 2018.

[6] Đ. Lekić and S. Vukosavić, "Calculation of Optimal Rotor Permanent Magnet Dimensions for RPMFS Machine," in *INFOTEH-JAHORINA (INFOTEH), 2018 17th International Symposium*, East Sarajevo, Bosnia-Herzegovina, pp. 1-6, 21-23 March 2018.

[7] W. Hua, P. Su, G. Zhang, M. Cheng, "A Novel Rotor-Permanent Magnet Flux-Switching Machine," in *Ecological Vehicles and Renewable Energies (EVER), 2015 Tenth International Conference on*, Monte Carlo, Monaco, pp. 1-10, 31 Mar. - 2 Apr. 2015.

[8] P. Su, W. Hua, Z. Wu, P. Han and M. Cheng, "Analysis of the Operation Principle for Rotor-Permanent-Magnet Flux-Switching Machines," *IEEE Trans. Ind. Electron.,* vol. 65, no. 2, pp. 1062 - 1073, Feb. 2018.

[9] P. Su, W. Hua, G. Zhang, Z. Chen, M. Cheng, "Analysis and Evaluation of Novel Rotor Permanent Magnet Flux-Switching Machine for EV and HEV Applications," *IET Electric Power Applications,* vol. 11, no. 9, pp. 1610-1618, Nov. 2017.

[10] P. Su and W. Hua, "Performance comparison between rotor flux-switching and stator flux-switching machines considering local demagnetization," *AIP Advances,* pp. 1-5, vol. 7, Jan. 2017.

[11] P. Su, W. Hua, C. Hou and M. Hu, "Research on the influence of rotor poles number on performances of rotor permanent-magnet flux-switching machines," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, USA, pp. 1-8, 1-5 Oct. 2017.

[12] Z. Q. Zhu and D. Howe, "Influence of Design Parameters on Cogging Torque in Permanent Magnet Machines," *IEEE Trans. Energy Convers.,* vol. 15, no. 4, pp. 407-412, Dec. 2000.

[13] M. Caruso, A. D. Tommaso, F. Marignetti, R. Miceli and G. Galluzzo, "A General Mathematical Formulation for Winding Layout Arrangement of Electrical Machines," *Energies,* vol. 11, no. 2, pp. 446-470, Feb. 2018.

[14] D. Meeker, *Finite Element Method Magnetics: OctaveFEMM Version 1.2 User's Manual,* Oct. 2006.

[15] D. Meeker, *Finite Element Method Magnetics Version 4.2 User's Manual,* Feb. 2009.

[16] D. Meeker, "Finite Element Method Magnetics," 6 Apr. 2014. [Online]. Available: http://www.femm.info. [Accessed 10 6 2018].

[17] S. Stipetić, W. Miebach and D. Žarko, "Optimization in Design of Electric Machines: Methodology and workflow," in *ACEMP-OPTIM-ELECTROMOTION 2015 Joint Conference*, Side, Turkey, pp. 1-8, 2-4 Sep. 2015.

[18] N. Bianchi, M. Dai Pre, "Use of the Star of Slots in Designing Fractional-Slot Single-Layer Synchronous Motors," *IEE Proceedings - Electric Power Applications,* vol. 153, no. 3, pp. 459 - 466, May 2006.

[19] N. Bianchi, S. Bolognani, M. Pre and G. Grezzani, "Design considerations for fractional-slot winding configurations of synchronous machines," *IEEE Trans. Ind. Appl.,* vol. 42, no. 4, pp. 997 - 1006, July 2006.

[20] N. Bianchi, M. Pre, L. Alberti and E. Fornasiero, *Theory and Design of Fractional-Slot PM Machines*, Padova, Italy: CLEUP cp, Sep. 2007.

[21] D. Žarko, D. Ban and R. Klarić, "Finite Element Approach to Calculation of Parameters of an Interior Permanent Magnet Motor," *Automatika: Journal for Control, Measurement, Electronics, Computing and Communications,* vol. 46, no. 3-4, pp. 113-122, Jan. 2006.

[22] W. Q. Chu and Z. Q. Zhu, "Average Torque Separation in Permanent Magnet Synchronous Machines Using Frozen Permeability," *IEEE Trans. Magn.,* vol. 49, no. 3, pp. 1202 - 1210, Mar. 2013.

[23] S. Stipetić, D. Žarko and M. Popescu, "Ultra-fast axial and radial scaling of synchronous permanent magnet machines," *IET Electric Power Applications*, vol. 10, no. 7, pp. 658-666, 8 2016.

[24] A. A. Rockhill, T. A. Lipo, "A Generalized Transformation Methodology for Polyphase Electric Machines and Networks," in *Electric Machines & Drives Conference (IEMDC), 2015 IEEE International*, Coeur d'Alene, Idaho, USA, pp. 1-8, 10-13 May 2015.

[25] T. Miller, *Brushless Permanent Magnet and Reluctance Motor Drives*, Oxford: Clarendon Press, 1989.

[26] Shin-Etsu Chemical Co., Ltd., "N36Z Nd-Fe-B Magnet Demagnetization Curves at Elevated Temperatures," Apr. 2016. [Online]. Available: http://www.shinetsu-rare-earth-magnet.jp/e/.

Medium Voltage Impedance-Admittance Measurement System Based on the Cascaded H-Bridge Multilevel Converter

Marko Petković, Nicolai Hildebrandt, Francisco D. Freijedo and Dražen Dujić

***Abstract*—Recent trends in power system design such as an increasing share of renewable energy sources and smart grids are creating different subsystem interactions that require proper investigation, understanding, describing and estimating global system stability through impedance-admittance measurement and identification. This paper proposes and presents the cascaded H-bridge multilevel inverter topology for perturbation injection converter and impedance-admittance measurement. The methodology of impedance-admittance measurement is explained together with different measurements requirements. Performance and suitability of this topology for impedance-admittance measurement is evaluated through simulations. Preliminary design principles are given for the converter. System level feasibility of the solution is proposed as a main result of the work.**

***Index Terms*—Cascaded H-bridge, impedance-admittance measurement, medium voltage, system identification.**

Original Research Paper
DOI: 10.7251/ELS1822105P

I. Introduction

In the wake of strong penetration of renewable energies, smart-grids and traction systems, as an example of interfacing electrical grids of different nature into traditional electrical power grids, power electronics is becoming one of the most important components of modern distributed electrical power networks. As an example, Fig. 1 shows the different components and subsystems such as solar parks, wind turbines, storage elements and different ac and dc grid interface points. More and more active loads such as power converters appear next to passive loads. Utilisation of power electronic systems inherently changes the nature of power system by introducing interactions among active components, behaviour that was not present before and is becoming increasingly complex [1], [2]. As a consequence, characterizing power systems with high penetration of power electronics is of a major interest nowadays. One of most commonly used methods to analyse the behavior and stability of a system is by characterizing small-signal impedance based models and applying the Nyquist criterion to the product between the source output impedance and load input admittance [1]–[3]. This characterization is made possible by the virtue of impedance-admittance modelling and measurement. For assessing the stability of a whole system, impedance-admittance measurement has to be performed at different nodes in the power system.

Modern complex power system may be composed of dc and ac grids of different frequencies and voltage and current levels. Stemming from this, an impedance-admittance measurement devices has to be highly modular and reconfigurable to comply with different constraints at measurement points such as system voltage and current ratings and frequency and the type of connection that can be physically made. In terms of measurements, a maximally wide possible frequency measurement range is sought for. The precision of measurements on the other side is also of utmost importance. This is due to the fact that the inclusion of switched power electronic devices, no matter how flexible, versatile and powerful in the sense of enabling the full potential of power systems, also brings some downsides such as harmonics and switching noise polluting the system voltages and currents.

The topic of impedance-admittance measurement for stability analysis of power system has established itself since last decade. In [4] an overview of impedance-admittance measurement techniques based on frequency domain identification techniques for the stability of ac systems is presented. The same work presents different practical implementations for a perturbation injection converter (PIC). Another approach is using the time-domain identification via load-stepping [5]. This method is well suitable for identification of parametrical models and its advantage is in the low number of load-stepping responses needed to identify the system. However, the drawback of this method is in the inability to characterize properly the impedances in the high-frequency range. Cross-correlation methods for extraction of small-signal impedances after injection of pseudo-random binary sequence (PRBS) are presented in [6]. Methods for measuring impedances in *dq*-domain using ac-sweep and wide bandwidth small-signal injection are presented in [7]–[9].

Different measurement devices are already commercially available for low-power low-voltage ranges for the design of power supplies and the technology is well-established [10]–[12]. However, medium voltage (MV) impedance-admittance measurement technology is still under development at the moment. Equipment such as programmable ac sources and grid emulators are commercial products that could be used for impedance-admittance measurement. They are designed in low voltage (LV) levels of up to $1\,\mathrm{kV}$ and power ratings up to $200\,\mathrm{kVA}$ [13]. These devices are well suited for perturbing

Manuscript received 24 October 2018. Received in revised form 19 December 2018. Accepted for publication 20 December 2018.

The authors are with the Power Electronics Laboratory - PEL, École Polytéchnique Fédérale de Lausanne - EPFL, Station 11, CH-1015 Lausanne, Switzerland (emails: marko.petkovic@epfl.ch, nicolai.hildebrandt@epfl.ch, francisco.freijedo@epfl.ch, drazen.dujic@epfl.ch).

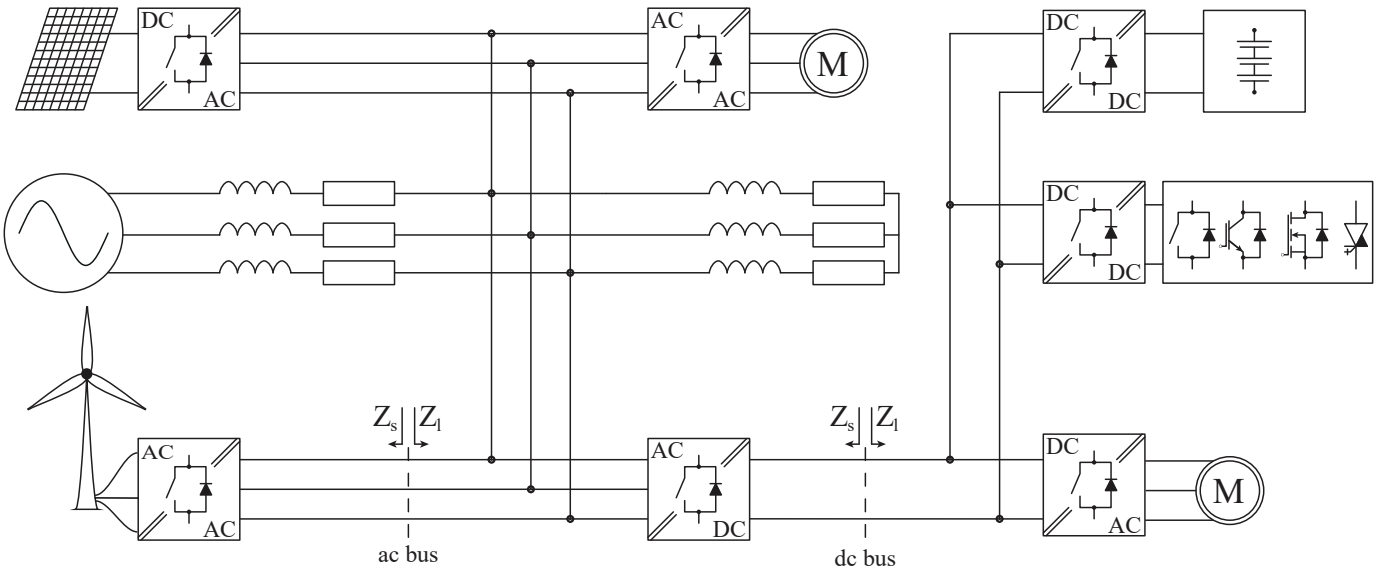


Fig. 1. Modern ac/dc distributed power system in which sources of different nature, ac or dc, and various voltage and current levels are connected through power electronics equipment. At each interface the system can be partitioned into the load and source side where each subsystem has its own characteristic impedance (or admittance) value through which the stability of the system can be assessed. Z_s — source impedance, Z_l — load impedance

systems as they are capable of delivering programmable harmonics or external waveform reference [13]–[16]. In general, this is a good solution when it comes to laboratory experiments at LV levels. However, from a close study in MV applications, we discarded this solution, since using this equipment for MV systems would require a step-up transformer which would in turn cause that the leakage inductances of the transformer damp the injected perturbation and thus limit the bandwidth of the PIC. This is even more noticeable at higher frequencies. The perturbation and measured signals should preferably be 10 times larger than the sensors accuracy which comes as a challenge and a target to meet. With a proper signal processing strategy this constraint could be relaxed and a set a more feasible requirement of having a measured signal that is 4 times larger than the sensor accuracy. These are known as "10:1" and "4:1" rules of thumb in metrology [17].

The previous discussion sets a motivation for our study. A complex research and design problem is established which includes topology identification and choice for PIC, as well as hardware and software design and integration. Besides, a complex measurement and data acquisition (DAQ) system has to be developed and accuracy and sensitivity to external disturbances of different sensors has to be assessed, considering noisy operational conditions. Once acquired, data has to be processed (online) or post-processed (offline). Then, in order to obtain reliable measurements, different system identification and calibration techniques can be considered. Combination of all of these elements presents itself as a perfect platform for research in medium voltage ac (MVAC) and medium voltage dc (MVDC) impedance-admittance measurements and system identification.

This work presents the selected topology for MVDC and MVAC PIC and investigates whether such a topology can be used for perturbation injection and subsequently impedance measurement. Main point of interest of this work is the terminal side and its performance potentials. The paper is organised in the following manner: Section II presents perturbation injection and measurement methods giving an overview of how the PIC can be interfaced to system. Section III presents the multilevel topology chosen and its different most important parts. Section IV presents one cell of the PIC. Section V presents relevant control aspects. Section VI presents details of the hardware design of the actual cell of the PIC. Section VII elaborates on the system foreseen for the acquisition and postprocessing of the results. Section VIII presents the simulations and performance of PIC in the environment of PIC, while the discussions and conclusion are provided in Section IX .

II. Pertubation injection converter and measurement methods

Different methods of connecting a perturbation devices to a power system to be identified have been researched and published as presented in Fig. 2. In all of these variants a small-signal perturbations, voltage or current, are injected into an unknown system, then current or voltage responses are measured and, consequently, from these the system impedance (or admittance) is identified. This work considers these three connection methods they offer a flexibility in terms of type of systems to be identified.

In the case of Fig. 2a the PIC is a main power source and an injection device at the same time, a perturbation signal is injected on top of a fundamental one. In this approach there is only one load and is well suited for grid emulators such as those in [13]–[16].

In Fig. 2b the PIC is connected in series between the source and the load subsystems and is used to inject small-signal voltage perturbations in the system. In this case the injected voltage has to be synchronized with the source voltage at the injection point. Advantage of this method is that the power

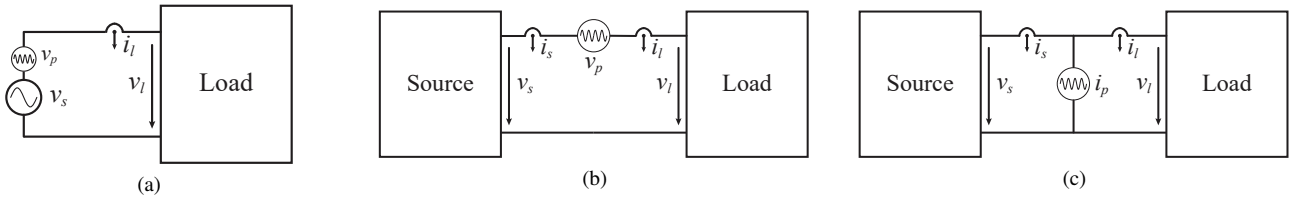


Fig. 2. Different injections methods of small signals for system identification. a) Pertubation by PIC interfacing a load and perturbing with a small voltage on top of the fundamental wave. b) Perturbation by voltage source connected in series between source and load. c) Pertubation by current source connected in shunt between source and load.

of the small-signal perturbation is low. However, this method presents itself with difficulties when it comes to PIC short-circuit protection and the PIC has to support rated system current.

Fig. 2c presents a shunt connected device between the source and load subsystems for small-signal current injection. As in the previous way, there has to exist a mean of synchronizing the injected small-signal with the system current. Advantage of this method is that the system current does not flow through the PIC unlike with the previous method, but on the other hand the PIC has to withstand the full line voltage of the system. Current perturbation injection is better suited for identifying smaller source side impedances as often larger load side impedance will force the injected current to flow in the direction of the source, thus leaving little perturbation current for the load side and making the load side measurement and identification more difficult. Another drawback is the fact that it is difficult to inject controlled harmonic current since a closed-loop control is necessary. Connecting a device between two subsystems allows the device to be an active part of a whole system and at the same time to be a perturbation device. Methods in Fig. 2 are generic ones and present a single-phase connection. Of course, they can be extended and applied to three-phase systems which are of interest in this work.

There exists a plethora of possible signal types and waveforms that could be used for injection and system perturbation. Most basic form of perturbing a system is using the ac frequency sweep where a single frequency is injected at a time which in the large frequency range of interest makes the measurement considerably slow. Another method is to use wide bandwidth signals such as swept sine in which signal frequency increases (or decreases) over a certain time. Random signals such as PRBS is introduced as white noise approximation. Even though these signals reduce measurement time, over a large frequency range their signal-to-noise ratio (SNR) decreases making the measurement more difficult. Another suitable signal is the multisine signal which contains multiple tones at the same time. The SNR of multisine signal is constant over a frequency range but is nevertheless lower compared to a single tone signal used for the ac-sweep. Evidently, a trade-off between the time and precision of measurement has to be made. One of the possible approaches to mitigate the problem of low SNR when using wide bandwidth signals is to use periodogram power spectral density methods [18], [19]. In [20] it is shown that the cross power spectral density (CPSD) estimation based on Welch periodogram spectral density estimation [21] algorithm is successfully used for identifying impedances where voltage and current measurements are affected by the noise.

When it comes to measurements themselves, in the case of Figs. 2b and 2c, source and load voltages and currents are measured while in the case of Fig. 2a, source voltage and load current are measured. Voltage and current transducers must have a sufficient accuracy. Not only magnitude but also the phase accuracy has to be high enough as the phase characteristics of sensors will also influence the impedance calculation results [7]. It goes without saying that not only high enough bandwidth is a must for these transducers, but also they need to measure reliably low-bandwidth signals. Possible candidates for transducers are voltage dividers for line voltage measurements and Rogowski and closed loop Hall current sensors for line current measurements.

Concerning voltage and current injection devices, different devices are reported in [22]–[24]. Reference [25] provides results in the MVAC grids and it describes a single phase impedance measurement unit in which three voltage source switching cells are connected in either parallel or series configuration and each of them fed from a dc-link. However, for this work, a highly scalable and modular solution, in terms of voltage and power levels, that can be employed for different applications is sought after. To this end, multilevel topologies appear as a possible candidate for the application. When directly interfacing an MV grid, multilevel converters provide a much reduced short-circuit impedance than solutions based on LV power electronics in combination with step-up transformers. We consider that cascaded H-bridge (CHB) with multiwinding transformer match a realistic / cost effective scenario. On one side these topologies are scalable and versatile. They can be used as a main source and as a perturbation source at the same time or can be used as an external device that solely serves the purposes of injecting a perturbation voltage or current. This multifunctionality can be achieved by physical reconfiguration of the converter cell connections. On the other side, in terms of control, multilevel topologies achieve a higher bandwidth (modulation and control) than topologies capable of delivering two level or three level outputs for the same output voltage and power rating. Having a higher bandwidth immediately allows higher perturbation frequencies and allows to identify the system up to a higher frequency. Thanks to the multilevel topology, there is no isolating transformer on the output side, where measurements are performed, thus no reduction in the output bandwidth that is now determined by implementation of the converter stages. Due to the advantages that this solution possesses, a multilevel CHB inverter topol-

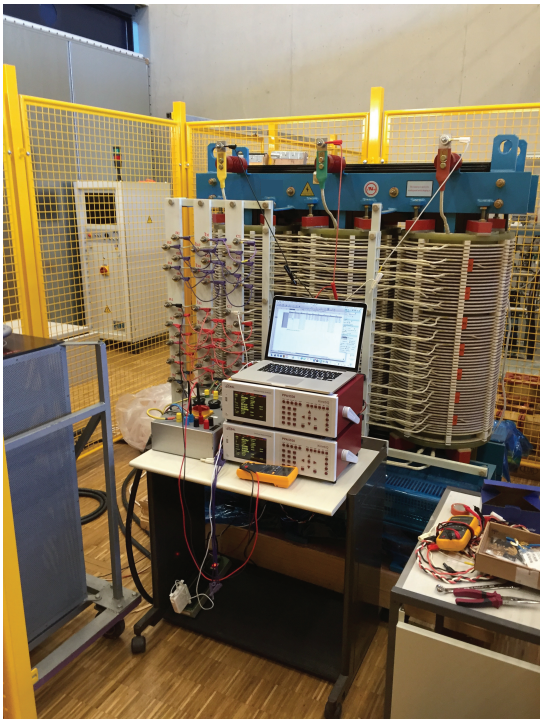


Fig. 3. 1 MVA multi-winding transformer.

ogy supplied by a multi-winding transformer is proposed and investigated for PIC application.

III. Cascaded H-Bridge Based Impedance-Admittance Measurement Unit

Different perturbation injection devices have been reported in the literature and they suffer from one common downside, the switching noise. When the switching noise is present, together with its side harmonics it becomes much more difficult to identify system response and separate it from the noise induced by the switched operation. However, one solution to alleviate this problem, at least to some extent, is to use a CHB multilevel inverter topology. The CHB multilevel inverter topologies output waveform contain have lower total harmonic distortion (THD) than 2-level topologies and the harmonics are contained in high frequency range which is not of interest to us [26]. As mentioned in Section II, base for the development of this solution is the multi-winding transformer in Fig. 3. Details about the transformer characteristics and modelling for electric circuit simulations are presented in [27] and Table I. The transformer itself shall be interfaced with a multilevel CHB converter (see Fig. 4) and five secondary winding of one single phase are connected to cells which are connected in series or in parallel at the output, depending on the type of injection performed. Moreover, depending on the type of injection a different output filter is required. This results in an 11-level CHB inverter topology which is the key element of the PIC. Having such a high number of voltage levels in combination with phase-shifted carrier PWM (PSC-PWM) gives a less distorted waveform which in return gives less noise pollution and better system response to be identified.

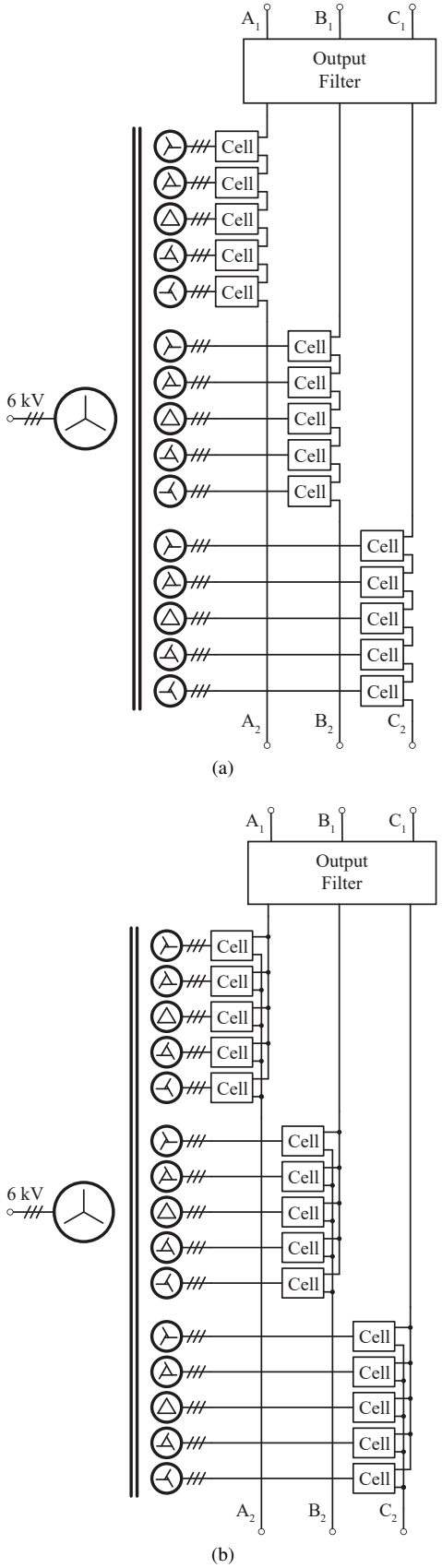


Fig. 4. CHB topology with isolated cell supply transformer with a) cell outputs connected in series for shunt current injection and b) cell outputs connected in parallel for series voltage injection.

TABLE I
MULTI-WINDING TRANSFORMER PARAMETERS

Parameter	Value
Apparent Power Rating	1 MVA
Primary Side Line Voltage	6.3 kV
Secondary Side Line Voltage	710 V
Grid frequency	50 Hz
Star Primary Windings	1
Extended Delta Secondary Windings	15
Phase Shift of the Secondaries	$-18°$, $-6°$, $6°$, $18°$, $30°$

The PIC shall be capable of providing all three connection modes as indicated in Fig. 2. In the series voltage injection mode the cells are connected in parallel, while in shunt current injection mode the cells are connected in series. As the PIC has to be connected in two different ways, the whole system has to be modular and cell connections have to be reconfigurable. The simplest and cheapest way of achieving this reconfigurability is mechanically through the system of bus bars. Most of the reported injection devices are unidirectional and are capable of creating an unidirectional perturbation whereas the topology reported in this work is a four-quadrant one and is capable of sinking current and reversing the voltage polarity which leaves open a question of influence of these methods on impedance-admittance measurement and system identification. A clear advantage is the fact that the PIC is a grid emulator and a measurement device at the same time, which allows for measurement at different grid operating points.

A. Output Waveform Filtering

The PIC is required to inject clean high-frequency small-signal voltage and current perturbations up to 10 kHz. Due to this requirement, the inverter end has to comprise a filter to eliminate the pulse-width modulation (PWM) harmonics to some extent. The inverter rectangular shaped voltages can be filtered in two ways, using the dv/dt and sine wave filters.

The first method filters only high frequency components to reduce the voltage slope of the PWM rectangle outputs. Since fast switching silicon carbide (SiC) MOSFETs are used to synthetize the output waveform dv/dt can reach high values. In any case of connection to a system seen in Fig. 2 the output voltage slope has to be limited in order not to provoke a damage to the system being identified. This requires protection equipment to be installed. The damped filter resonant frequency f_d of this filter is chosen to be higher than both the output frequency f_{out} and the switching frequency, i.e. $f_{\text{out}} \ll f_{\text{sw}} \ll f_d$.

The second approach is used to filter out the switching frequency components to obtain a sinusoidal output waveform. Three factors determine the choice of the sinusoidal filter. The first is the tolerance of the voltage distortion level of the output filter, the second one is the maximum allowable voltage drop on the filter and the third depends on the switching frequency of the inverter switches [28]. The first two factors are directly sets the requirements on the output waveform of the PIC. Third factor reflects on the damped resonant frequency which is required to be larger than the output frequency but smaller than the switching frequency, i.e. $f_{\text{out}} \ll f_d \ll f_{\text{sw}}$.

With respect to injection methods presented in Fig. 2, the PIC may require three different output filter configurations which may result in converter loss budget savings and volume savings for both the converter and the filter. Factors that determine the choice of filter are the power losses, in the converter and the filter respectively, and voltage and current ratings that the PIC has to withstand. Two types of filters to be considered are LC and L filter (see Fig. 5). The L filter is used for the current injection, while the LC filter is used for voltage injection, i.e. L to provide a current source and LC for a voltage source. This type of output filter provides a transformerless solution at the output stage for perturbation injection. Transfer functions $G_{LC}(s)$ and $G_L(s)$ of these filters are well known:

$$G_{LC}(s) = \frac{v_p(s)}{v_{\text{inv}}(s)} = \frac{1}{s^2 L_f C_f + 1} \tag{1}$$

$$G_L(s) = \frac{i_p(s)}{v_{\text{inv}}(s)} = \frac{1}{sL_f} \tag{2}$$

The LC filter will present a damped resonance at resonance frequency f_d, after which all frequency components are attenuated at a rate of $-40\,\text{dB/dec}$.

$$f_d = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{3}$$

The L filter presents no resonance and acts as a first order low-pass filter with $-20\,\text{dB/dec}$ attenuation rate.

IV. SINGLE CASCADED H-BRIDGE CELL

The single cell of the CHB converter is presented in Fig. 6 and it comprises an input filter, active front-end (AFE) and an H-bridge (HB) inverter. The injection converter shall be designed to support 6 kV line-to-line ac voltages and 100 A currents with up to 1 MVA output power [29]. The 1 MVA converter is built of 15 cells which means that each cell has a nominal power of 66.7 kVA. The PIC is required to inject only a portion of system voltage or current, namely 5–10 %, in the range of 1 Hz–10 kHz. As a rule of thumb, this means that the apparent switching frequency should be 100 kHz. Since the presence of only five secondary windings per phase implies relatively low multiplication factor ($N = 5$) for the apparent switching frequency, it means that the switches inside a HB should be switched at least at 20 kHz. Due to the high switching frequency SiC devices are considered for the HB stage [29]. Table II summarizes the cell parameters.

A. Input Filtering

As the cell is interfaced to the transformer secondary it is naturally connected to the transformer secondary leakage inductance. Following from this, different input filter configurations can be used for this application. Different options for the input filter are presented in Fig. 7. Choice of filter type and position of voltage and current transducers directly influences control strategy for the cell.

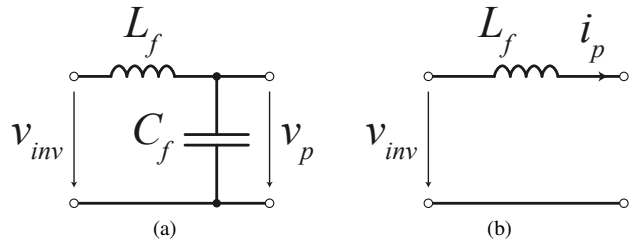


Fig. 5. a) LC and b) L output filter configuration circuits. v_{inv} — inverter ouput voltage, v_p — perturbation voltage, i_p — perturbation current.

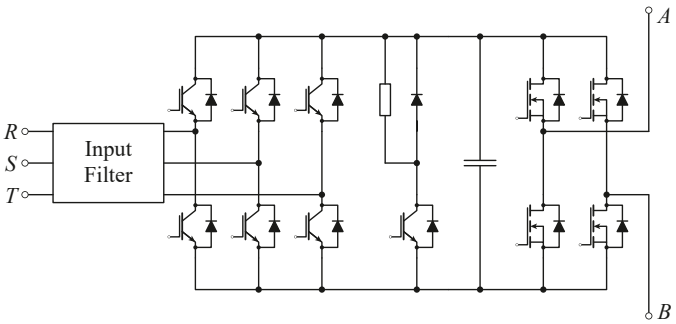


Fig. 6. Regenerative cell with an input filter, AFE stage (left) and inverter HB stage (right).

B. Active Front-End

In order to investigate the influence of having a four-quadrant topology for perturbation generation front-end is silicon IGBT based AFE. Switching frequency is set at $10\,\mathrm{kHz}$. Transformer secondaries provide a multiple of $60°/N$ phase shift. Due to this, the current control bandwidth of AFE is rather low. On the other side, having a high dc-link voltage control bandwidth and lower filtering effort of AFE switching harmonics is sought after. This requirement is filled by increasing the AFE switching frequency. Power modules of the $1.7\,\mathrm{kV}$ voltage class are chosen for this application, and for simplicity reasons two-level switching cells are chosen. Reason for choosing this voltage class modules is the nominal dc-link voltage which derives from the line voltages of transformer secondaries. Package type chosen for the semiconductor module is the standard $62\,\mathrm{mm}$ package. This is a standard package with many alternative sources which is easy to integrate with the existing gate drivers on one hand and reduces thermal management effort on the other hand. In order to decrease the voltage overshoots due to stray inductances, a snubber capacitor rated for $1.2\,\mathrm{kV}$ is connected across each IGBT. Amongst many commercially available power modules, SEMIKRON SKM150GB17E4G $1.7\,\mathrm{kV}$ IGBT power module with body diode was one of the suitable candidates for the application and was therefore chosen [29].

C. Voltage limiting circuit and dc-link

The bandwidth requirements and realization for the AFE and the HB are not the same. In case of sudden energy flow reversal and in order to prevent transient overvoltages in the dc-link, a voltage limiting circuit is also present in the cell as a protective mean. The dc-links in the cells are independent between themselves and each dc-link is controlled independently. In this way, the problem of dc-link voltage unbalance is eliminated. The purpose of the dc-link capacitor is dual. On one side it serves to maintain the desired dc-link voltage and reduce the voltage ripple, thus enabling proper dc operation point for the converter, while on the other it serves as a storage for reactive energy during low frequency injection. Unlike the usual design where low frequencies would not be considered, in this case the dc-link design needs to take into account the lowest injection frequency that needs to be achieved while at the same time taking into account the maximum allowable voltage ripple. The dc capacitor can be calculated with respect to the maximum allowed voltage ripple for the lowest injection frequency point [20]. Trying to fulfill all conditions of having highest possible small-signal voltage and current injection and lowest frequency would result in capacitance values far too big for any practical implementation which in turns forces us to make certain trade-offs, e.g. derating for lower frequency injection. For this application the dc-link nominal voltage $1200\,\mathrm{V}$ and the capacitance of $5\,\mathrm{mF}$ is set. Capacitors used for the application are film type because of high frequency injection and low output filter impedance and are rated for $1.32\,\mathrm{kV}$.

TABLE II
CELL PARAMETERS

Parameter	Value
Apparent Power Rating	$66.7\,\mathrm{kVA}$
AFE Nominal Current	$54\,\mathrm{A}$
Inverter HB Nominal Current	$96\,\mathrm{A}$
Nominal dc-link voltage	$1200\,\mathrm{V}$
Semiconductor blocking voltage	$1700\,\mathrm{V}$
Inverter HB Modulation	PSC-PWM

D. H-Bridge Inverter

As higher switching frequencies are required at the inverter end, SiC MOSFET devices are chosen for this application. The inverter nominal current is $96\,\mathrm{A}$ so power modules with at least $150\,\mathrm{A}$ current rating are chosen. The MOSFET package is identical to the one of the IGBT. Type of modules that will be used will be $62\,\mathrm{mm}$ SiC $1.7\,\mathrm{kV}$ MOSFET power modules due to the ease of integration with the AFE.

V. CONTROL

A. Active Front End Control

There exist multiple ways of controlling the AFE unit. We have chosen that the input rectification stage and dc-link voltage are controlled by the synchronous reference frame (SRF) decoupled current control. The control diagram is presented in figure Fig. 8. i_d^*, i_q^*, i_d and i_q is the *d*- and *q*-axis current references and measurements respectively, v_g the secondary side voltage of the transformer, i_c the AFE ac input current, v_{dc}^* and v_{dc} the dc-link voltage reference and measurement. The i_d^* is obtained through the cascaded proportional-integral (PI) control of the dc-link voltage. The i_q^* is usually set to zero as there is no reactive power demand. The modulation type used is the space vector modulation (SVM).

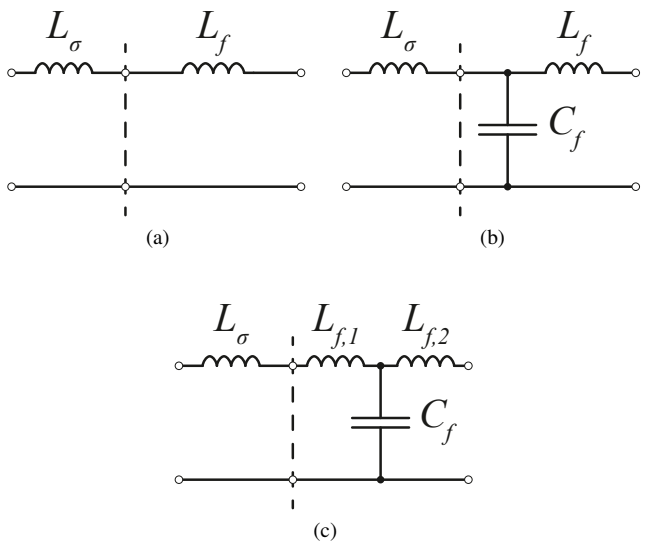


Fig. 7. Different input filter configurations: a) L input filter in combination with transformer secondary side leakage inductance forming LL filter, b) CL input filter in combination with secondary side leakage inductance forming LCL filter, c) LCL input filter in combination with secondary side leakage inductance forming LLCL filter. Dashed line represents the connection point between the transformer and input filter.

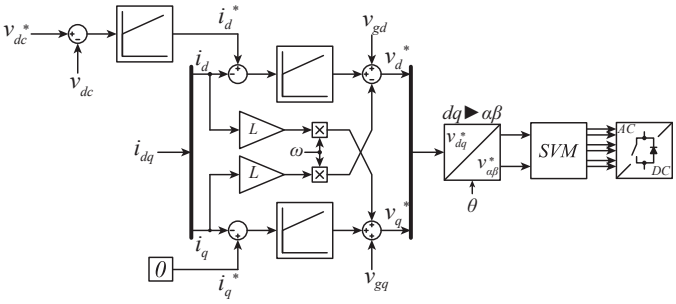


Fig. 8. AFE control diagram.

The angle θ is obtaned with the SRF-phase-locked loop (PLL) by measuring primary transformer voltages and applying phase shift corresponding to each secondary.

B. CHB Multilevel Inverter Output Control

Due to the versatility requirement that multiple types of injections are possible, current or voltage ones, different control strategies can be applied for each case and these strategies directly depend on the type of output filters used. As mentioned in Subsection III-A, the LC filter is used for voltage injection, thus the voltage v_p on the capacitor is controlled, which needs to be synchronized with the system it is being injected in. In the case of current injection, the current i_p in the inductor is controlled and this current also has to be synchronized with the system current. For the injection type as the one presented in Fig. 2a, no synchronization is needed.

VI. Preliminary Hardware Construction and Prototyping

A preliminary 3D CAD representation of the cell is shown in Fig. 9. The cell layout mainly depends on the cooling system, choice of power modules packaging type, gate drivers, dc-link capacitors, snubber capacitor and insulation coordination standards that have to be respected. Due to the possible size of the input filter, it is physically placed outside the cell.

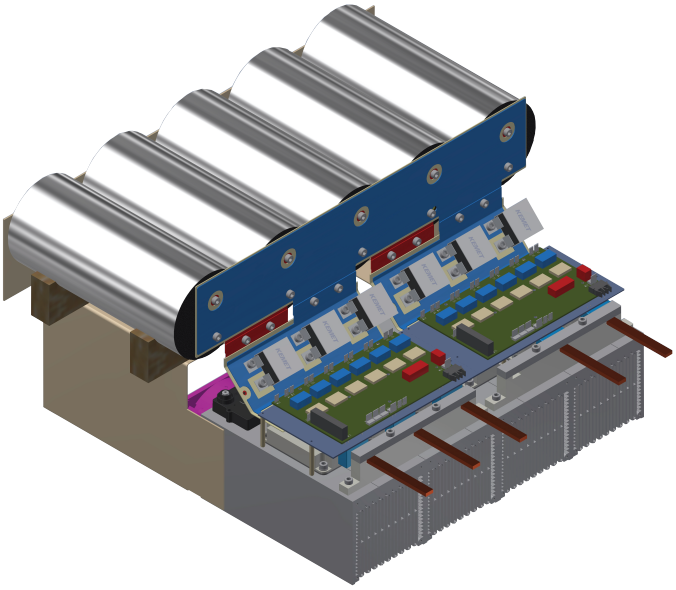


Fig. 9. 3D CAD representation of the cell. AFE is to positioned to the left side and HB inverter to the right.

Both the AFE and HB inverter are mounted on a heatsink of the same type. This arrangement of switching devices simplifies the integration between the AFE and HB as the whole structure becomes symmetrical. This also means that the cooling system for the HB inverter is oversized for the minimal switching frequency of 20 kHz, which in turn allows for the switching frequency to be pushed even further if required. Type of heatsink used is an aluminium hollow fins heatsink which is combined with forced air cooling system. The dimensions of the heatsinks are $240\,\mathrm{mm} \times 120\,\mathrm{mm} \times 250\,\mathrm{mm}$.

The copper busbar system carries the current from the input terminals through the current transducers to the power modules, the dc-link and further to the HB inverter. The current transducers are placed beneath the gate driver interface board, thus easing the connection to the dedicated current measurement connectors. The dc side busbars are designed as to reduce the overall stray inductance using wide parallel copper plates and aligning connections with the main current flow. The standard UL 840 is followed when designing the busbars in order to have proper creepage / clearance distances. Each dc plate is $1\,\mathrm{mm}$ thick which is enough to carry the nominal current. Insulating layer is made from flame retardant polypropylene electrical insulation material. The layer thickness is $30\,\mathrm{mil}$ ($0.762\,\mathrm{mm}$). The dc-link is realized with five parallel film capacitors which are mounted behind the cooling system.

Gate driver circuits are placed directly on top of the power modules on their dedicated interface board as the fast switching is required and the gate signal paths should be kept as short as possible. Moreover, a metallic shielding is needed between the gate driver circuits and power modules and around the

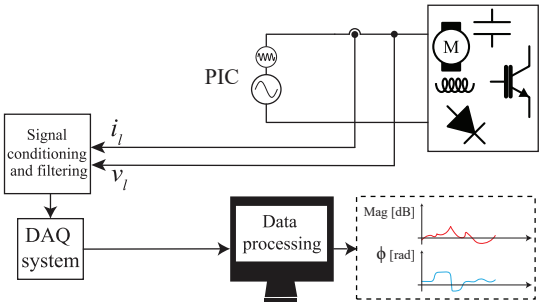


Fig. 10. Complete system block diagram.

gate drivers. In this way the EMI effect on the gate drivers is reduced and it provides a physical protection of the circuits beneath.

The overall size of the system are given by two elements, dc-link and the cooling system. The overall size of the cell is $600\,\mathrm{mm}\times500\,\mathrm{mm}\times350\,\mathrm{mm}$. The cooling system and the dc-link account for $30\,\%$ of the overall cell volume.

VII. Measurement, Data Acquisition System and System Identification Chain

A complete system level diagram is presented in Fig. 10. It includes a PIC used for perturbation injection to an unknown system that can be composed of various components, passive and active ones, voltage and current measurements on the source and the load side, signal conditioning for DAQ instrument and finally data processing to which the system identification methods are applied.

A. Measurement system

For proper impedance identification a proper measurement system is indispensable. The measurements are implemented via voltage and current sensors placed on the source and on the load side. Both the line-to-line voltages and currents are measured. Due to the maximum injection frequency sought for, voltage and currents up to $10\,\mathrm{kHz}$ need to be measured at the MV level. Measurement devices need to measure the full range voltages and currents while having a constant gain and almost no phase delay in the frequency range of interest, otherwise it will affect the computed impedance value. Moreover, each measurement has to be conditioned, i.e. filtered and scaled for the DAQ instrument, for which a dedicated measurement conditioning system needs to be designed. The challenge regarding the sensor design is the fact that they need to measure the full range quantities, even though only the perturbation portion is of interest in the end.

B. Data Acquisition System

Next step is feeding the conditioned measurement to DAQ instrument. The DAQ system needs to be equipped with enough acquisition channels to acquire synchronously all voltage and current measurements needed. In the DAQ instruments, the analog measurements are sampled using a high enough sampling rate and converted to their digital counterparts.

C. Data Processing and System Identification

Final step in the chain is the data processing and application of system identification methods in order to compute the impedance. The signal processing is performed in an external PC and relies on the methods such as those in [20]. Another important part in the chain is the visualization of results over the full frequency range.

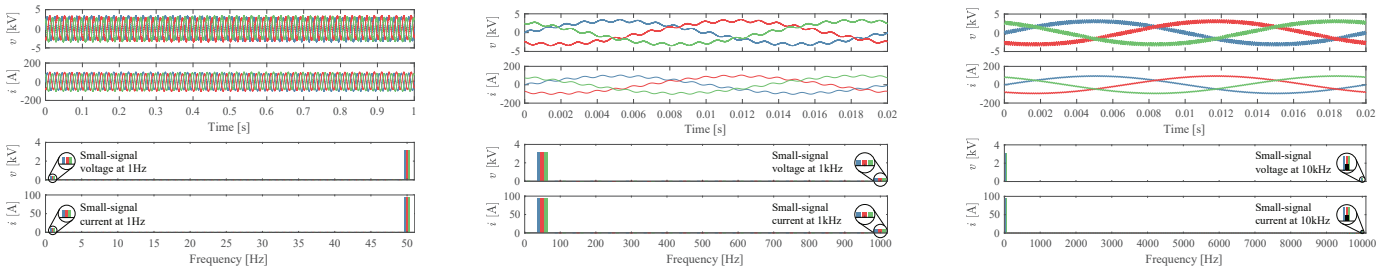
VIII. Perturbation Injection Converter Performance

Three different configurations presented in Fig. 2 were simulated. PIC is connected to a load of $R_{\mathrm{load}} = 36\,\Omega$ and $L_{\mathrm{load}} = 1\,\mathrm{mH}$. Fundamental output line-to-line voltage is $5.4\,\mathrm{kV}$ and small-signal voltage is $600\,\mathrm{V}$, i.e. $10\,\%$ of maximum line-to-line voltage. In this configuration power output of the PIC is $1\,\mathrm{MW}$.

Fig. 11 presents results for the case in which the PIC is the main source and perturbation source, as in Fig. 2a.

Fig. 12 presents load voltage and currents in the case where the small-signal voltage perturbation is injected in series with a source between the source and the load, as in Fig. 2b. Again, the source voltage is $5.4\,\mathrm{kV}$ while the small-signal voltage is $600\,\mathrm{V}$ and the load characteristic is the same.

Fig. 13 presents source voltage and currents in the case where the current perturbation is injected in shunt at a point between the source and the load, as in Fig. 2c. In this case the source voltage is $6\,\mathrm{kV}$ and the load characteristic is the same. Current injected by the PIC is $9.6\,\mathrm{A}$. In all three configurations perturbations at $1\,\mathrm{Hz}$, $1\,\mathrm{kHz}$ and $10\,\mathrm{kHz}$ are injected.

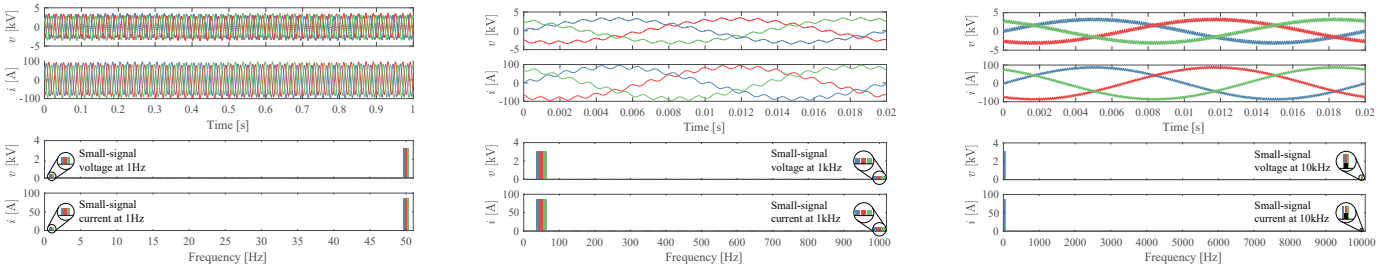


(a) Case of a $1\,\mathrm{Hz}$ source voltage injection on top of a $50\,\mathrm{Hz}$ fundamental wave

(b) Case of a $1\,\mathrm{kHz}$ source voltage injection on top of a $50\,\mathrm{Hz}$ fundamental wave

(c) Case of a $10\,\mathrm{kHz}$ source voltage injection on top of a $50\,\mathrm{Hz}$ fundamental wave

Fig. 11. Simulation waveforms for the configuration in Fig. 2a. *a*, *b* and *c* phase voltages and currents are visible in blue, red and green.

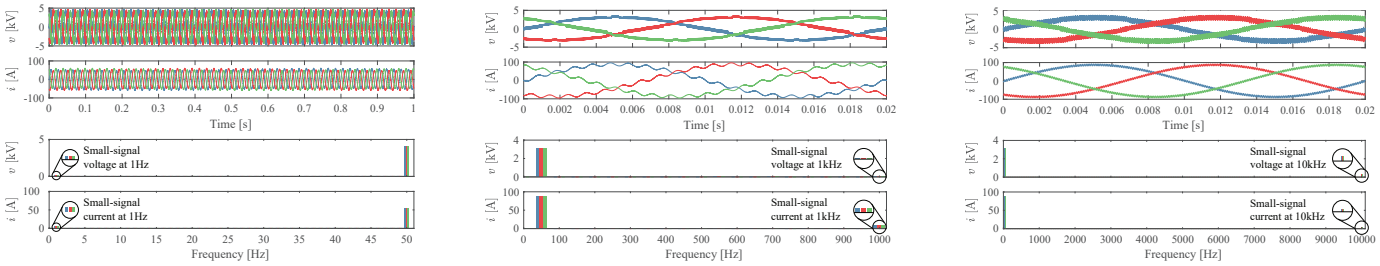


(a) Case of a 1 Hz source voltage injection on top of a 50 Hz fundamental wave

(b) Case of a 1 kHz source voltage injection on top of a 50 Hz fundamental wave

(c) Case of a 10 kHz source voltage injection on top of a 50 Hz fundamental wave

Fig. 12. Load side simulation waveforms for the configuration in Fig. 2b. *a*, *b* and *c* phase voltages and currents are visible in blue, red and green.



(a) Case of a 1 Hz source voltage injection on top of a 50 Hz fundamental wave

(b) Case of a 1 kHz source voltage injection on top of a 50 Hz fundamental wave

(c) Case of a 10 kHz source voltage injection on top of a 50 Hz fundamental wave

Fig. 13. Source side simulation waveforms for the configuration in Fig. 2c. *a*, *b* and *c* phase voltages and currents are visible in blue, red and green.

IX. Conclusion

This paper focused on the CHB topology employed as a PIC whose objective usage is impedance-admittance measurement and system identification. The use of multilevel topology in combination with fast switching devices allows higher apparent switching frequencies and consecutively high frequency output voltage and current which also means a higher bandwidth and better system characterization. Moreover, versatility of the proposed solution provides a capability of having a main source and a perturbation source in the same device, a possibility of connecting the device in three different configurations at various interfaces in the system. Owing to the scalability, the proposed topology can be used at different voltage and current levels.

References

[1] X. Wang and F. Blaabjerg, "Harmonic stability in power electronic based power systems: Concept, modeling, and analysis," *IEEE Transactions on Smart Grid*, pp. 1–1, 2018.

[2] U. Javaid, F. D. Freijedo, D. Dujic, and W. Van Der Merwe, "Dynamic assessment of source–load interactions in marine MVDC distribution," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 6, pp. 4372–4381, 2017.

[3] R. D. Middlebrook, "Input filter considerations in design and application of switching regulators," *IEEE Industry Applications Society Annual Meeting*, 1976.

[4] Y. A. Familiant, J. Huang, K. A. Corzine, and M. Belkhayat, "New techniques for measuring impedance characteristics of three-phase ac power systems," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1802–1810, 2009.

[5] V. Valdivia, A. Lázaro, A. Barrado, P. Zumel, C. Fernández, and M. Sanz, "Impedance identification procedure of three-phase balanced voltage source inverters based on transient response measurements," *IEEE Transactions on Power Electronics*, vol. 26, no. 12, pp. 3810–3816, Dec. 2011.

[6] D. Martin, E. Santi, and A. Barkley, "Wide bandwidth system identification of ac system impedances by applying pertubations to an existing converter," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, IEEE, 2011, pp. 2549–2556.

[7] G. Francis, "An algorithm and system for measuring impedance in dq coordinates," PhD thesis, Virginia Polytechnic Institute and State University, 2010.

[8] Z. Shen, "Online measurement of three-phase ac power system impedance in synchronous coordinates," PhD thesis, Virginia Polytechnic Institute and State University, 2013.

[9] G. Francis, R. Burgos, D. Boroyevich, F. Wang, S. Zhiyu, P. Mattavelli, K. Karimi, and S.-w. J. Fu, *Algorithm and implementation system for measuring impedance in the dq domain*, US Patent 9,140,731, Sep. 2015.

[10] Ridley Engineering. (2016). AP300 Analyzer, [Online]. Available: http://old.ridleyengineering.com/analyzer.html.

[11] Omicron Lab. (2017). Fast and easy measurements with the Bode 100, [Online]. Available: https://www.omicron-lab.com/bode-100/product-description.html.

[12] Keysight Technologies. (2018). Impedance Analyzers, [Online]. Available: https://www.keysight.com/en/pc-1000000382%3Aepsg%3Apgr/impedance-analyzers?cc=US&lc=eng.

[13] EGSTON, *COMPISO P-HIL System*, https://egston.com/01-power-electronics/?lang=en.

[14] Regatron, *TopCon TC.ACS - Full 4-quadrant grid simulator*, https://www.regatron.com/en/products-topcon/18-english-categories/products/94-topcon-tc-acs-full-4-quadrant-grid-simulator.

[15] Cinergia, *GE - Grid Emulator series*, http://www.cinergia.coop/cinergia-product/ge-grid-emulator-series.

[16] Spitzberger and Spies. (2012). PAS series of 4-Quadrant Amplifi ers, [Online]. Available: www.spitzenberger.de/download.ashx?weblink=1002.

[17] RFM. (2017). Ten to One or One to Ten Rule, [Online]. Available: https://rfminc.net/resource-center/metrology-tips/ten-to-one-to-ten/.

[18] M. K. Steven *et al.*, "Modern spectral estimation: Theory and application," *Signal Processing Series*, 1988.

[19] P. Stoica, R. L. Moses, *et al.*, *Spectral analysis of signals*. Pearson Prentice Hall Upper Saddle River, NJ, 2005, vol. 1, pp. 22–55.

[20] M. D. Jaksic, "Identification of small-signal dq impedances of power electronics converters via single-phase wide-bandwidth injection," PhD thesis, Virginia Polytechnic Institute and State University, 2015.

[21] P. Welch, "The use of fast fourier transform for the estimation of power spectra: A method based on time averaging over short, modified periodograms," *IEEE Transactions on audio and electroacoustics*, vol. 15, no. 2, pp. 70–73, 1967.

[22] Y. L. Familiant, K. A. Corzine, J. Huang, and M. Belkhayat, "Ac impedance measurement techniques," in *IEEE International Conference on Electric Machines and Drives, 2005.*, May 2005, pp. 1850–1857.

[23] M. Jaksic, Z. Shen, I. Cvetkovic, D. Boroyevich, R. Burgos, and P. Mattavelli, "Wide-bandwidth identification of small-signal dq impedances of ac power systems via single-phase series voltage injection," in *17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Sep. 2015, pp. 1–10.

[24] Z. Shen, M. Jaksic, P. Mattavelli, D. Boroyevich, J. Verhulst, and M. Belkhayat, "Three-phase ac system impedance measurement unit (IMU) using chirp signal injection," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2013, pp. 2666–2673.

[25] M. Jakšić, Z. Shen, I. Cvetković, D. Boroyevich, R. Burgos, C. DiMarino, and F. Chen, "Medium-voltage impedance measurement unit for assessing the system stability of electric ships," *IEEE Transactions on Energy Conversion*, vol. 32, no. 2, pp. 829–841, Jun. 2017.

[26] D. Grahame Holmes and Thomas A. Lipo, "Carrier Based PWM of Multilevel Inverters," in *Pulse Width Modulation for Power Converters: Principles and Practice*. IEEE, 2003, pp. 452–464.

[27] M. Luo, D. Dujic, and J. Allmeling, "Leakage flux modeling of medium-voltage phase-shift transformers for system-level simulations," *IEEE Transactions on Power Electronics*, pp. 1–1, 2018, (early access).

[28] J. Guzinski, H. Abu-Rub, and P. Strankowski, *Variable speed AC drives with inverter output filters*. John Wiley & Sons, 2015, pp. 65–93.

[29] N. Hildebrandt, M. Petković, and D. Dujić, "Evaluation of 1.7 kV SiC MOSFETs for a regenerative cascaded H-bridge multilevel converter cell," in *2018 IEEE International Conference on Industrial Technology (ICIT)*, Feb. 2018, pp. 718–723.

Preparation of Papers for Electronics (September 2011)

First A. Author, Second B. Author, and Third C. Author

***Abstract*—These instructions give you guidelines for preparing papers for ELECTRONICS journal. Use this document as a template if you are using Microsoft *Word* 6.0 or later. Otherwise, use this document as an instruction set. The electronic file of your paper will be formatted further. Define all symbols used in the abstract. Do not cite references in the abstract. Do not delete the blank line immediately above the abstract; it sets the footnote at the bottom of this column.**

***Index Terms*—About four key words or phrases in alphabetical order, separated by commas.**

Paper Classification
DOI: 10.7251/ELSxxxxxxxx

I. Introduction

THIS document is a template for Microsoft *Word* versions 6.0 or later.

When you open the file, select "Page Layout" from the "View" menu in the menu bar (View | Page Layout), which allows you to see the footnotes. Then, type over sections of file or cut and paste from another document and use markup styles. The pull-down style menu is at the left of the Formatting Toolbar at the top of your *Word* window (for example, the style at this point in the document is "Text"). Highlight a section that you want to designate with a certain style, then select the appropriate name on the style menu. The style will adjust your fonts and line spacing. **Do not change the font sizes or line spacing to squeeze more text into a limited number of pages.** Use italics for emphasis; do not underline. The length of the manuscript is limited to the maximum of 15 pages.

To insert images in *Word,* position the cursor at the insertion point and either use Insert | Picture | From File or copy the image to the Windows clipboard and then Edit | Paste Special | Picture (with "float over text" unchecked).

We will do the final formatting of your paper.

Manuscript received 15 September 2011 (write the date when you have first sent the manuscript for review). Received in revised form 20 October 2011 (write the date when you have sent the manuscript in its revised form if revisions required for your paper after review).

(Place here any sponsor and financial support acknowledgments).

F. A. Author is with the Faculty of Electrical Engineering, University of Banja Luka, Banja Luka, Bosnia and Herzegovina (corresponding author to provide phone: +387-51-222-333; fax: +387-51-111-222; e-mail: author@et-fbl.net).

S. B. Author was with Faculty of Technical Sciences, University of Novi Sad, Novi Sad, Serbia. He is now with the Institute "Mihailo Pupin", Belgrade, Serbia (e-mail: author@pupin.rs).

T. C. Author is with the School of Electrical Engineering, University of Belgrade, Belgrade, Serbia, on leave from the Faculty of Electronic Engineering, University of Niš, Niš, Serbia (e-mail: author@elfak.ni.ac.rs).

II. Procedure for Paper Submission

A. Review Stage

The manuscripts are to be submitted using the Electronics Journal online submission system – accessible from Journal's homepage. Prepare it in two-column format as shown in this template. Place all figures and tables at the end of the paper (after the references) on separate page(s). Figures and tables must have the same caption names as referenced in the text. Only PDF format of the manuscript is allowed at the review stage. Please, check if all fonts are embedded and subset and that the quality of diagrams, illustrations, and graphics is satisfactory. Failing to provide above listed requirements is a valid reason for rejection.

B. Final Stage

When you submit your final version (after your paper has been accepted), prepare it in two-column format, including figures and tables in accordance with this template. Pack all of your files (manuscript source file in *Word*, figures, and manuscript PDF form) within one archive file (you may use any of the available file compression tools: *WinZip*, *WinRAR*, *7-Zip*, etc.). Do not forget to provide the manuscript converted in PDF format that will be used as a reference for final formatting of your paper. Figures should be named as referenced in the manuscript (e.g. *fig1.eps*, *fig2.tif*, etc.)

C. Figures and Tables

Format and save your graphic images using a suitable graphics processing program and adjusts the resolution settings. We accept images in the following formats: PS, EPS, TIFF, GIF, and PNG. Additionally, it is allowed to use images generated by using one of the following software tools: Microsoft Word, Microsoft PowerPoint, or Microsoft Excel. The resolution of a RGB color file should be 400 dpi. Please note that JPG and other lossy-compressed image formats are not allowed. Use available software tools to convert these images to appropriate format.

Image quality is very important to how yours graphics will reproduce. Even though we can accept graphics in many formats, we cannot improve your graphics if they are poor quality when we receive them. If your graphic looks low in

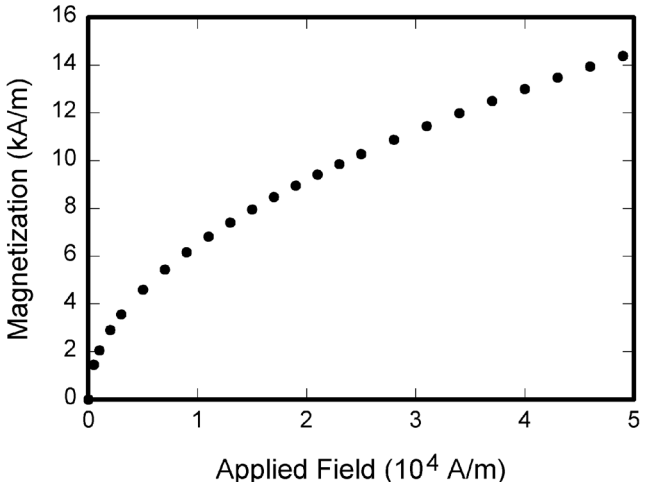


Fig. 1. Magnetization as a function of applied field. Note that "Fig." is abbreviated. There is a period after the figure number, followed by two spaces. It is good practice to explain the significance of the figure in the caption.

quality on your printer or monitor, please keep in mind that cannot improve the quality after submission.

If you are importing your graphics into this Word template, please use the following steps:

Under the option EDIT select PASTE SPECIAL. A dialog box will open, select paste picture, then click OK. Your figure should now be in the Word Document.

If you are preparing images in TIFF, EPS, or PS format, note the following. High-contrast line figures and tables should be prepared with 600 dpi resolution and saved with no compression, 1 bit per pixel (monochrome).

Photographs and grayscale figures should be prepared with 300 dpi resolution and saved with no compression, 8 bits per pixel (grayscale).

Most charts graphs and tables are one column wide (3 1/2 inches or 21 picas) or two-column width (7 1/16 inches, 43 picas wide). We recommend that you avoid sizing figures less than one column wide, as extreme enlargements may distort your images and result in poor reproduction. Therefore, it is better if the image is slightly larger, as a minor reduction in size should not have an adverse affect the quality of the image.

III. Math

If you are using *Word,* use either the Microsoft Equation Editor or the *MathType* add-on (http://www.mathtype.com) for equations in your paper (Insert | Object | Create New | Microsoft Equation *or* MathType Equation). "Float over text" should *not* be selected.

IV. Units

Use either SI (MKS) or CGS as primary units. (SI units are strongly encouraged.) English units may be used as secondary units (in parentheses). **This applies to papers in data storage.** For example, write "15 Gb/cm^2 (100 Gb/in^2)." An exception is when English units are used as identifiers in trade, such as "3½-in disk drive." Avoid combining SI and CGS units, such as current in amperes and magnetic field in oersteds. This often leads to confusion because equations do not balance dimensionally. If you must use mixed units, clearly state the units for each quantity in an equation.

The SI unit for magnetic field strength H is A/m. However, if you wish to use units of T, either refer to magnetic flux density B or magnetic field strength symbolized as $\mu_0 H$. Use the center dot to separate compound units, e.g., "A·m^2."

TABLE I
Units for Magnetic Properties

Symbol	Quantity	Conversion from Gaussian and CGS EMU to SI [a]
Φ	magnetic flux	1 Mx $\rightarrow 10^{-8}$ Wb = 10^{-8} V·s
B	magnetic flux density, magnetic induction	1 G $\rightarrow 10^{-4}$ T = 10^{-4} Wb/m^2
H	magnetic field strength	1 Oe $\rightarrow 10^3/(4\pi)$ A/m
m	magnetic moment	1 erg/G = 1 emu $\rightarrow 10^{-3}$ A·m^2 = 10^{-3} J/T
M	magnetization	1 erg/(G·cm^3) = 1 emu/cm^3 $\rightarrow 10^3$ A/m
$4\pi M$	magnetization	1 G $\rightarrow 10^3/(4\pi)$ A/m
σ	specific magnetization	1 erg/(G·g) = 1 emu/g $\rightarrow$ 1 A·m^2/kg
j	magnetic dipole moment	1 erg/G = 1 emu $\rightarrow 4\pi \times 10^{-10}$ Wb·m
J	magnetic polarization	1 erg/(G·cm^3) = 1 emu/cm^3 $\rightarrow 4\pi \times 10^{-4}$ T
χ, κ	susceptibility	1 $\rightarrow 4\pi$
χ_ρ	mass susceptibility	1 cm^3/g $\rightarrow 4\pi \times 10^{-3}$ m^3/kg
μ	permeability	1 $\rightarrow 4\pi \times 10^{-7}$ H/m = $4\pi \times 10^{-7}$ Wb/(A·m)
μ_r	relative permeability	$\mu \rightarrow \mu_r$
w, W	energy density	1 erg/cm^3 $\rightarrow 10^{-1}$ J/m^3
N, D	demagnetizing factor	1 $\rightarrow 1/(4\pi)$

Vertical lines are optional in tables. Statements that serve as captions for the entire table do not need footnote letters.

[a]Gaussian units are the same as cgs emu for magnetostatics; Mx = maxwell, G = gauss, Oe = oersted; Wb = weber, V = volt, s = second, T = tesla, m = meter, A = ampere, J = joule, kg = kilogram, H = henry.

V. Helpful Hints

A. Figures and Tables

Because we will do the final formatting of your paper, you do not need to position figures and tables at the top and bottom of each column. In fact, all figures, figure captions, and tables can be at the end of the paper. Large figures and tables may span both columns. Place figure captions below the figures; place table titles above the tables. If your figure has two parts, include the labels "(a)" and "(b)" as part of the artwork. Please verify that the figures and tables you mention in the text actually exist. **Please do not include captions as part of the figures. Do not put captions in "text boxes" linked to the figures. Do not put borders around the outside of your figures.** Use the abbreviation "Fig." even at the beginning of a sentence. Do not abbreviate "Table." Tables are numbered with Roman numerals.

Color printing of figures is not available Do not use color unless it is necessary for the proper interpretation of your figures.

Figure axis labels are often a source of confusion. Use words rather than symbols. As an example, write the quantity "Magnetization," or "Magnetization *M*," not just "*M*." Put units in parentheses. Do not label axes only with units. As in Fig. 1, for example, write "Magnetization (A/m)" or "Magnetization ($A \cdot m^{-1}$)," not just "A/m." Do not label axes with a ratio of quantities and units. For example, write "Temperature (K)," not "Temperature/K."

Multipliers can be especially confusing. Write "Magnetization (kA/m)" or "Magnetization (10^3 A/m)." Do not write "Magnetization (A/m) x 1000" because the reader would not know whether the top axis label in Fig. 1 meant 16000 A/m or 0.016 A/m. Figure labels should be legible, approximately 8 to 12 point type.

B. References

Number citations consecutively in square brackets [1]. The sentence punctuation follows the brackets [2]. Multiple references [2], [3] are each numbered with separate brackets [1]–[3]. When citing a section in a book, please give the relevant page numbers [2]. In sentences, refer simply to the reference number, as in [3]. Do not use "Ref. [3]" or "reference [3]" except at the beginning of a sentence: "Reference [3] shows ... ." Please do not use automatic endnotes in *Word*, rather, type the reference list at the end of the paper using the "References" style.

Number footnotes separately in superscripts (Insert | Footnote).[1] Place the actual footnote at the bottom of the column in which it is cited; do not put footnotes in the reference list (endnotes). Use letters for table footnotes (see Table I).

Please note that the references at the end of this document are in the preferred referencing style. Give all authors' names; do not use "*et al*." unless there are six authors or more. Use a space after authors' initials. Papers that have not been published should be cited as "unpublished" [4]. Papers that have been accepted for publication, but not yet specified for an issue should be cited as "to be published" [5]. Papers that have been submitted for publication should be cited as "submitted for publication" [6]. Please give affiliations and addresses for private communications [7].

Capitalize only the first word in a paper title, except for proper nouns and element symbols. For papers published in translation journals, please give the English citation first, followed by the original foreign-language citation [8]. All references **must be** written in Roman alphabet.

C. Abbreviations and Acronyms

Define abbreviations and acronyms the first time they are used in the text, even after they have already been defined in the abstract. Abbreviations such as IEEE, SI, ac, and dc do not have to be defined. Abbreviations that incorporate periods should not have spaces: write "C.N.R.S.," not "C. N. R. S." Do not use abbreviations in the title unless they are unavoidable (for example, "IEEE" in the title of this article).

D. Equations

Number equations consecutively with equation numbers in parentheses flush with the right margin, as in (1). First use the equation editor to create the equation. Then select the "Equation" markup style. Press the tab key and write the equation number in parentheses. To make your equations more compact, you may use the solidus (/), the exp function, or appropriate exponents. Use parentheses to avoid ambiguities in denominators. Punctuate equations when they are part of a sentence, as in

$$\int_0^{r_2} F(r,\varphi)\,\mathbf{d}\,d\varphi = [\sigma r_2/(2\mu_0)] \cdot \int_0^{\infty} \exp(-\lambda\,|z_j - z_i|)\,\lambda^{-1} J_1(\lambda r_2)\,J_0(\lambda r_i)\,d\lambda\,. \tag{1}$$

Be sure that the symbols in your equation have been defined before the equation appears or immediately following. Italicize symbols (*T* might refer to temperature, but T is the unit tesla). Refer to "(1)," not "Eq. (1)" or "equation (1)," except at the beginning of a sentence: "Equation (1) is ... ."

E. Other Recommendations

Use one space after periods and colons. Hyphenate complex modifiers: "zero-field-cooled magnetization." Avoid dangling participles, such as, "Using (1), the potential was calculated." [It is not clear who or what used (1).] Write instead, "The potential was calculated by using (1)," or "Using (1), we calculated the potential."

Use a zero before decimal points: "0.25," not ".25." Use "cm^3," not "cc." Indicate sample dimensions as "0.1 cm x 0.2 cm," not "0.1 x 0.2 cm^2." The abbreviation for "seconds" is "s," not "sec." Do not mix complete spellings and abbreviations of units: use "Wb/m^2" or "webers per square meter," not "webers/m^2." When expressing a range of values, write "7 to 9" or "7-9," not "7~9."

A parenthetical statement at the end of a sentence is punctuated outside of the closing parenthesis (like this). (A parenthetical sentence is punctuated within the parentheses.) In American English, periods and commas are within quotation marks, like "this period." Other punctuation is "outside"! Avoid contractions; for example, write "do not" instead of "don't." The serial comma is preferred: "A, B, and C" instead of "A, B and C."

If you wish, you may write in the first person singular or plural and use the active voice ("I observed that ..." or "We observed that ..." instead of "It was observed that ..."). Remember to check spelling. If your native language is not English, please get a native English-speaking colleague to carefully proofread your paper.

[1] It is recommended that footnotes be avoided (except for the unnumbered footnote with the receipt date and authors' affiliations on the first page). Instead, try to integrate the footnote information into the text.

VI. Some Common Mistakes

The word "data" is plural, not singular. The subscript for the permeability of vacuum μ_0 is zero, not a lowercase letter "o." The term for residual magnetization is "remanence"; the adjective is "remanent"; do not write "remnance" or "remnant." Use the word "micrometer" instead of "micron." A graph within a graph is an "inset," not an "insert." The word "alternatively" is preferred to the word "alternately" (unless you really mean something that alternates). Use the word "whereas" instead of "while" (unless you are referring to simultaneous events). Do not use the word "essentially" to mean "approximately" or "effectively." Do not use the word "issue" as a euphemism for "problem." When compositions are not specified, separate chemical symbols by en-dashes; for example, "NiMn" indicates the intermetallic compound $Ni_{0.5}Mn_{0.5}$ whereas "Ni–Mn" indicates an alloy of some composition Ni_xMn_{1-x}.

Be aware of the different meanings of the homophones "affect" (usually a verb) and "effect" (usually a noun), "complement" and "compliment," "discreet" and "discrete," "principal" (e.g., "principal investigator") and "principle" (e.g., "principle of measurement"). Do not confuse "imply" and "infer."

Prefixes such as "non," "sub," "micro," "multi," and "ultra" are not independent words; they should be joined to the words they modify, usually without a hyphen. There is no period after the "et" in the Latin abbreviation "*et al.*" (it is also italicized). The abbreviation "i.e.," means "that is," and the abbreviation "e.g.," means "for example" (these abbreviations are not italicized).

An excellent style manual and source of information for science writers is [9].

VII. Editorial Policy

Each manuscript submitted is subjected to the following review procedure:

- It is reviewed by the editor for general suitability for this publication
- If it is judged suitable, two reviewers are selected and a single-blinded review process takes place
- Based on the recommendations of the reviewers, the editor then decides whether the particular paper should be accepted as is, revised or rejected.

Do not submit a paper you have submitted or published elsewhere. Do not publish "preliminary" data or results. The submitting author is responsible for obtaining agreement of all coauthors and any consent required from sponsors before submitting a paper. It is the obligation of the authors to cite relevant prior work.

Every paper submitted to "Electronics" journal are single-blind reviewed. For conference-related papers, the decision to accept or reject a paper is made by the conference editors and publications committee; the recommendations of the referees are advisory only. Undecipherable English is a valid reason for rejection.

VIII. Publication Principles

The contents of "Electronics" are peer-reviewed and archival. The "Electronics" publishes scholarly articles of archival value as well as tutorial expositions and critical reviews of classical subjects and topics of current interest.

Authors should consider the following points:

1) Technical papers submitted for publication must advance the state of knowledge and must cite relevant prior work.
2) The length of a submitted paper should be commensurate with the importance, or appropriate to the complexity, of the work. For example, an obvious extension of previously published work might not be appropriate for publication or might be adequately treated in just a few pages.
3) Authors must convince both peer reviewers and the editors of the scientific and technical merit of a paper; the standards of proof are higher when extraordinary or unexpected results are reported.
4) Because replication is required for scientific progress, papers submitted for publication must provide sufficient information to allow readers to perform similar experiments or calculations and use the reported results. Although not everything need be disclosed, a paper must contain new, useable, and fully described information. For example, a specimen's chemical composition need not be reported if the main purpose of a paper is to introduce a new measurement technique. Authors should expect to be challenged by reviewers if the results are not supported by adequate data and critical details.
5) Papers that describe ongoing work or announce the latest technical achievement, which are suitable for presentation at a professional conference, may not be appropriate for publication in "Electronics".

IX. Conclusion

A conclusion section is not required. Although a conclusion may review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions.

Appendix

Appendixes, if needed, appear before the acknowledgment.

Acknowledgment

The preferred spelling of the word "acknowledgment" in American English is without an "e" after the "g." Use the singular heading even if you have many acknowledgments. Avoid expressions such as "One of us (S.B.A.) would like to thank ... ." Instead, write "F. A. Author thanks ... ." **Sponsor and financial support acknowledgments are placed in the unnumbered footnote on the first page, not here.**

References

[1] G. O. Young, "Synthetic structure of industrial plastics (Book style with paper title and editor)," in *Plastics*, 2nd ed. vol. 3, J. Peters, Ed. New York: McGraw-Hill, 1964, pp. 15–64.

[2] W.-K. Chen, *Linear Networks and Systems* (Book style). Belmont, CA: Wadsworth, 1993, pp. 123–135.

[3] H. Poor, *An Introduction to Signal Detection and Estimation*. New York: Springer-Verlag, 1985, ch. 4.

[4] B. Smith, "An approach to graphs of linear forms (Unpublished work style)," unpublished.

[5] E. H. Miller, "A note on reflector arrays (Periodical style—Accepted for publication)," *IEEE Trans. Antennas Propagat.*, to be published.

[6] J. Wang, "Fundamentals of erbium-doped fiber amplifiers arrays (Periodical style—Submitted for publication)," *IEEE J. Quantum Electron.*, submitted for publication.

[7] C. J. Kaufman, Rocky Mountain Research Lab., Boulder, CO, private communication, May 1995.

[8] Y. Yorozu, M. Hirano, K. Oka, and Y. Tagawa, "Electron spectroscopy studies on magneto-optical media and plastic substrate interfaces (Translation Journals style)," *IEEE Transl. J. Magn.Jpn.*, vol. 2, Aug. 1987, pp. 740–741 [*Dig. 9th Annu. Conf. Magnetics* Japan, 1982, p. 301].

[9] M. Young, *The Techincal Writers Handbook.* Mill Valley, CA: University Science, 1989.

[10] J. U. Duncombe, "Infrared navigation—Part I: An assessment of feasibility (Periodical style)," *IEEE Trans. Electron Devices*, vol. ED-11, pp. 34–39, Jan. 1959.

[11] S. Chen, B. Mulgrew, and P. M. Grant, "A clustering technique for digital communications channel equalization using radial basis function networks," *IEEE Trans. Neural Networks*, vol. 4, pp. 570–578, Jul. 1993.

[12] R. W. Lucky, "Automatic equalization for digital communication," *Bell Syst. Tech. J.*, vol. 44, no. 4, pp. 547–588, Apr. 1965.

[13] S. P. Bingulac, "On the compatibility of adaptive controllers (Published Conference Proceedings style)," in *Proc. 4th Annu. Allerton Conf. Circuits and Systems Theory*, New York, 1994, pp. 8–16.

[14] G. R. Faulhaber, "Design of service systems with priority reservation," in *Conf. Rec. 1995 IEEE Int. Conf. Communications,* pp. 3–8.

[15] W. D. Doyle, "Magnetization reversal in films with biaxial anisotropy," in *1987 Proc. INTERMAG Conf.*, pp. 2.2-1–2.2-6.

[16] G. W. Juette and L. E. Zeffanella, "Radio noise currents n short sections on bundle conductors (Presented Conference Paper style)," presented at the IEEE Summer power Meeting, Dallas, TX, Jun. 22–27, 1990, Paper 90 SM 690-0 PWRS.

[17] J. G. Kreifeldt, "An analysis of surface-detected EMG as an amplitude-modulated noise," presented at the 1989 Int. Conf. Medicine and Biological Engineering, Chicago, IL.

[18] J. Williams, "Narrow-band analyzer (Thesis or Dissertation style)," Ph.D. dissertation, Dept. Elect. Eng., Harvard Univ., Cambridge, MA, 1993.

[19] N. Kawasaki, "Parametric study of thermal and chemical nonequilibrium nozzle flow," M.S. thesis, Dept. Electron. Eng., Osaka Univ., Osaka, Japan, 1993.

[20] J. P. Wilkinson, "Nonlinear resonant circuit devices (Patent style)," U.S. Patent 3 624 12, July 16, 1990.

[21] IEEE Criteria for Class IE Electric Systems (Standards style), IEEE Standard 308, 1969.

[22] Letter Symbols for Quantities, ANSI Standard Y10.5-1968.

[23] R. E. Haskell and C. T. Case, "Transient signal propagation in lossless isotropic plasmas (Report style)," USAF Cambridge Res. Lab., Cambridge, MA Rep. ARCRL-66-234 (II), 1994, vol. 2.

[24] E. E. Reber, R. L. Michell, and C. J. Carter, "Oxygen absorption in the Earth's atmosphere," Aerospace Corp., Los Angeles, CA, Tech. Rep. TR-0200 (420-46)-3, Nov. 1988.

[25] (Handbook style) *Transmission Systems for Communications,* 3rd ed., Western Electric Co., Winston-Salem, NC, 1985, pp. 44–60.

[26] *Motorola Semiconductor Data Manual,* Motorola Semiconductor Products Inc., Phoenix, AZ, 1989.

[27] (Basic Book/Monograph Online Sources) J. K. Author. (year, month, day). *Title* (edition) [Type of medium]. Volume (issue). Available: http://www.(URL)

[28] J. Jones. (1991, May 10). Networks (2nd ed.) [Online]. Available: http://www.atm.com

[29] (Journal Online Sources style) K. Author. (year, month). Title. *Journal* [Type of medium]. Volume(issue), paging if given. Available: http://www.(URL)

[30] R. J. Vidmar. (1992, August). On the use of atmospheric plasmas as electromagnetic reflectors. *IEEE Trans. Plasma Sci.* [Online]. *21(3).* pp. 876–880. Available: http://www.halcyon.com/pub/journals/21ps03-vidmar

Information for Authors

Editorial objectives

In the journal ”Electronics”, the scientific papers from different fields of electronics and electrical engineering in the broadest sense are published. Main topics are electronics, automatics, telecommunications, computer techniques, power engineering, nuclear and medical electronics, analysis and synthesis of electronic circuits and systems, new technologies and materials in electronics etc. The main emphasis of papers should be on methods and new techniques, or the application of existing techniques in a novel way.

The reviewing process

Each manuscript submitted is subjected to the following review procedures:

- It is reviewed by the editor for general suitability for this publication;
- If it is judged suitable, two reviewers are selected and a double-blind review process takes place;
- Based on the recommendations of the reviewers, the editor then decides whether the particular paper should be accepted as it is, revised or rejected.

Submissions Process

The manuscripts are to be submitted using the Electronics Journal online submission system – accessible from Journal’s homepage.

Manuscripts have to be prepared in accordance with the instructions given in the template for paper preparation that can be found on the journal’s web page (www.els-journal.etf.unibl.org).

Authors should note that proofs are not supplied prior to publication and ensure that the paper submitted is complete and in its final form.

Copyright

Articles submitted to the journal should be original contributions and should not be under consideration for any other publication at the same time. Authors submitting articles for publication warrant that the work is not an infringement of any existing copyright and will indemnify the publisher against any breach of such warranty. For ease of dissemination and to ensure proper policing of use, papers and contributions become the legal copyright of the publisher unless otherwise agreed.

ELECTRONICS, VOL. 22, NO. 2, DECEMBER 2018

ISSN 1450-5843
UDK 621.38