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Editor's Column

Mladen Knezic

> The first principle is that you must not fool yourself and you are the easiest person to fool.
>
> *Richard P. Feynman*

Editorial Letter
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THE December issue of *Electronics* journal in 2019 contains five regular papers that present recent advancements in the field of electronics, audio signal processing and control theory applied to power grids balancing.

The paper "A Novel Domino Logic with Modified Keeper in 16nm CMOS Technology", authored by S. Singhal, A. Mehra, and U. Tripathi, proposes a novel domino logic aimed at improving the power dissipation and reducing consumed area of the circuit. A comparison with previous techniques is provided in the paper as well as simulation results obtained using Ngspice simulator.

The paper "Single-Stage Operational Transconductance Amplifier Design in UTBSOI Technology Based on g_m/I_d Methodology" by R. U. Ahmed, E. A. Vijaykumar, and P. Saha adopts the g_m/I_d methodology for designing the single-stage Operational Transconductance Amplifier (OTA). Simulation results, obtained with Cadence-Spectre, confirms that UTBSOI (Ultra-Thin-Body Silicon-On-Insulator) transistor in sub-micron regime (180nm) can be successfully used to design analog circuits. It is also shown that UTBSOI-OTA introduces some improvements in terms of DC gain and power consumption in comparison to the CMOS-OTA realization.

The paper "Dual Output Sinusoidal Oscillator Using Second Generation Controlled Conveyor" by S. Zahiruddin, A. Srinivasulu, and M. Sarada presents a dual-output sinusoidal oscillator realized using the second generation current-controlled conveyor (CCCII). The authors proposed a circuit realized using commercially available CCCII and provided results obtained using PSPICE simulator. Additionally, the correct operation of the circuit was confirmed experimentally.

The paper "Contribution to Time and Frequency Analysis of Irregular Sleep Snoring" by M. Rezki and A. Alimohad gives a summary analysis of human hearing focusing on acute snoring. The author proposed VAD (Voice Activity Detection) technique for detecting apnea episodes in the snoring signal.

The paper "PI Regulator with Tracking Anti-Windup Based Modified Power Balance Theory for SAPF under Unbalanced Grid Voltage Unbalance Non Linear Loads" by K. Kamel, Z. Laid, and B. Amar presents a modified power balance theory for extracting the reference compensating currents to shunt active power filter (SAPF) which is applied to illuminate current harmonics and compensate reactive power under unbalanced voltages and unbalancing non-linear loads. The authors developed a MATLAB/Simulink model of the control system to verify the performance of the proposed technique. The presented simulation results imply that low percentage of THD (Total Harmonic Distortion) can be achieved even in the case of unbalanced grid voltage.

I thank the authors for their contribution to this issue of the journal and to all the reviewers who participated in the editorial process by providing valuable comments in timely manner to the editors and the authors.

A Novel Domino Logic with Modified Keeper in 16nm CMOS Technology

Smita Singhal, Anu Mehra, and Upendra Tripathi

***Abstract*—Domino logic is a clocked CMOS (*Complementary Metal-Oxide Semiconductor*) logic with fewer transistors than static CMOS logic. A PMOS (P-type Metal-Oxide Semiconductor) transistor, known as "keeper", is included in the design to improve the noise tolerance performance and to reduce the leakage current. The aspect ratio i.e. W/L of the keeper (W=width and L=length) is kept low for the correct functionality of the domino logic. This paper proposes a domino logic with modified keeper in order to improve the circuit with respect to power and area as compared to various existing techniques of domino logic i.e. *clock delayed domino logic* (CDD), *high speed domino logic* (HSD), *multi threshold high speed domino logic* (MHSD), *clock delayed sleep mode domino logic* (CDSMD), *sleep switch domino logic* (SSDD), *PMOS* only sleep switch domino logic (PSSDD), *reduced delay variations domino logic* (RDVD) and *Foot Driven Stack Transistor Domino Logic* (FDSTDL). The proposed as well as existing domino logics, for 8-input as well as 16-input OR gate in 16nm CMOS technology, are simulated for different values of W/L of keeper with W/L ratio ranging from 1 to 6. The *power-delay-product*(PDP) of proposed design has improved as compared to the existing designs. For 8-input OR gate and W/L=6, PDP had improved to maximum of 99.99% for CDD and minimum of 38.09% for SSDD.**

***Index Terms*—Domino, dynamic, static power, CMOS, keeper.**

Original Research Paper
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I. Introduction

With the growing trend of wireless communication and portable computing, power dissipation has become one of the critical factors in the development of semiconductor industry. The number of transistors on an integrated circuit are continously growing according to Moore's law [1]. Examples are latest cell phone application processors. The transistor count has increased from 1 billion transistors in processor A5 to 2 billions in processor A6 and then to 3 billion in processor A6X [2]. To meet this high transistor density and to increase the performance, CMOS (*Complementary Metal-Oxide Semiconductor*) technology has to continue to scale. Technology scaling has lead to shrinking of parameters like supply voltage, threshold voltage, gate oxide thickness in order to increase the performance of the circuit [3]. But this has resulted in higher power dissipation. Minimizing power dissipation calls for conscious effort at each abstraction level and at each phase of design process [4].

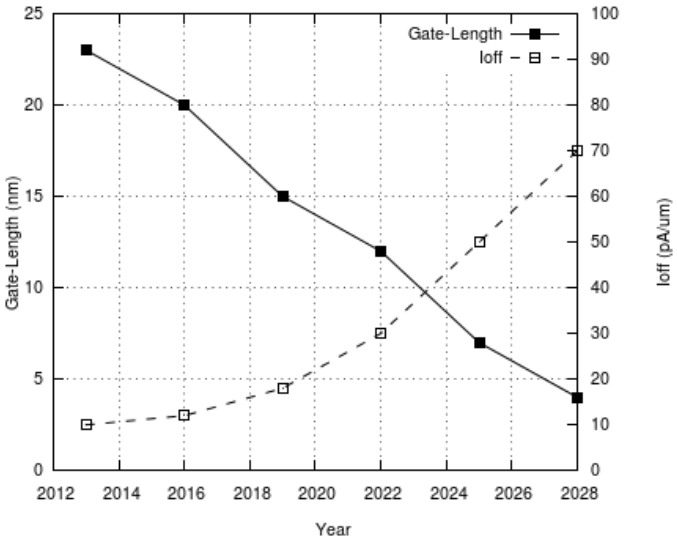

Fig. 1. Trends of changes in gate-length and I_{off} according to ITRS 2013.

The power dissipation in a CMOS circuit comprises of mainly two components – dynamic power and static power. Dynamic power occurs due to the switching activities of circuits i.e. charging and discharging of load capacitances, short-circuit current from supply voltage to ground and glitches in the output waveforms. Static power dissipation is related to the logical state of the circuit rather than the switching activities. In CMOS circuits, static power dissipation occurs due to leakage current that flows when the inputs, and thus the outputs, of the gate are not changing. Fig. 1 shows the changes in gate-length and I_{off} according to *Intenational Technology Roadmap For Semiconductors* (ITRS) 2013. Current I_{off} contributes to static power.

Static CMOS is a logic circuit in which output is strongly driven because it is directly connected to either to V_{DD} or ground (GND). Fig. 2 shows the static CMOS logic which comprises of pull up network and pull down network. In case of pull-up, a connection is made from V_{DD} to *out* when *out* = 1. In case of pull-down, a connection is made from GND to *out* when *out* = 0. The number of gates are required are *2N* where N is the fan-in. In order to reduce the number of gates, logics like pseudo-NMOS, where NMOS is N-type metal-oxide semiconductor, pass transistor logic have been implemented [5]. But these circuits have large static power

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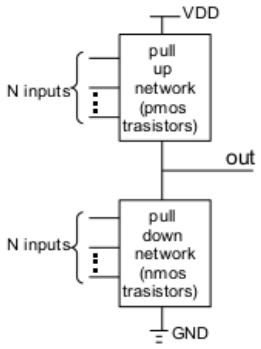

Fig. 2. A static CMOS logic.

dissipation. To reduce the static power dissipation, dynamic logic or clocked logic has been introduced. Dynamic logic uses only pull down network consisting of NMOS transistors to implement its logic. The block diagram of dynamic logic is shown in Fig. 3(a). It can be seen that the number of transistors are *N+2* which is less than the static CMOS. The main advantage of dynamic logic is that since the inputs are connected only to NMOS transistors, the input capacitance is less and thus dynamic logic operates faster than their static counterparts [6]. In dynamic logic, clock is distributed throughout and can lead to erroneous values in case of different timings of the clock in different parts of logic. If several stages of CMOS dynamic logic are cascaded using a single clock, a *race condition* can occur [7]. This can be solved with the help of domino logic which has an extra CMOS inverter at the output node as shown in Fig. 3(b).

Domino CMOS logic is used in variety of applications due to their high speed and low transistor count. But, due to leakage current and charge sharing, this logic has low noise immunity as compared to complementary CMOS logic [8]. Thus a PMOS (P-type Metal-Oxide Semiconductor) keeper is added in domino logic to compensate for the leakage current as shown in Fig. 4. But, the PMOS keeper has the disadvantage for degrading the performance of the device and contention currrent as explained in Section II.

Many logic techniques have been proposed earlier to improve the domino circuits in terms of performance, delay and area of the circuit.

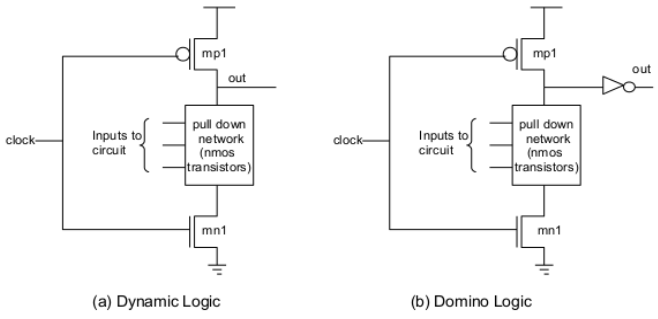

Fig. 3. Block diagrams of dynamic and domino logic.

For a given technology and gate topology, the product of power consumption and propagation delay is generally constant [5]. This product i.e. *power-delay-product* (PDP) is often used as a quality measure for a switching device. This paper also uses PDP as the metric to compare domino logic designs and to find the one that is fast and consume little energy.

A. Contribution

In this paper, a domino logic with modified keeper is proposed to improve the power dissipation and area of the circuit. The proposed design is compared with previous techniques of domino logic for six different values of aspect ratio of the keeper i.e W/L=1 to W/L=6. The design is improved as compared to existing designs for all the values of aspect ratio. The static power dissipation of the proposed design is reduced with respect to the previous techniques. For an 8-input OR gate and W/L=6, static power has reduced to 99.99% as compared to CDD and to 8.99% as compared to FDSTDL. The area of the circuit is also reduced making the design suitable for low power applications.

B. Organization of paper

Section II describes the functionality of domino logic and existing techniques of domino logic. Section III describes the proposed domino logic technique while Section IV discusses the results of the simulations performed on existing and proposed domino logic. Section V concludes the results of the proposed technique.

II. Literature Review

A. Domino Logic

Fig. 4 shows an 8-input OR-gate standard domino logic module. It consists of a clocked PMOS device *mp1*, pull down network consisting of only NMOS transistors, clocked NMOS device *mn1* and a static inverter producing non-inverting output, *out* [5]. A PMOS transistor *mp2* known as *keeper* is added to improve noise margins and to hold the value of output node *X* to *high* state during evaluation phase. The pull down network is built exactly as that in complementary CMOS. The domino module works in two phases – *precharge* and *evaluation*. Signal *clock* controls the mode of operation of domino as shown below:

$$clock = \begin{cases} 0, & \text{precharge phase} \\ 1, & \text{evaluation phase} \end{cases} \quad (1)$$

During *precharge* phase domino node *X* is charged to V_{DD} by PMOS transistor *mp1*. The clocked NMOS transistor *mn1* is *off* during this phase. Since the value of *out* becomes '0', keeper transistor *mp2* turns *on* which charges the value of node *X* to V_{DD}.

During *evaluation* phase, transistor *mp1* is *off* while *mn1* is in *on* state. If the input values *i1-i8* are such that pull down network conducts, then node *X* discharges to '0'. This will make the value of *out* to '1' and thus keeper turns *off*. If pull

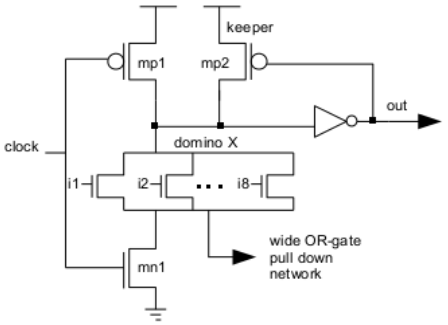

Fig. 4. Standard Domino Logic.

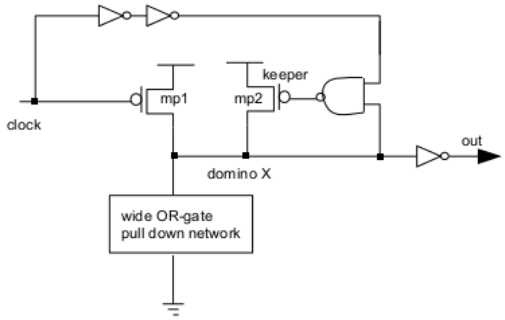

Fig. 5. Clock Delayed Domino Logic (CDD) [10].

down network is non-conducting then node *X* will retain the value of V_{DD} with the help of keeper transistor.

During the beginning of evaluation, keeper is *on* charging the node *X* to V_{DD}. If the input values makes pull down network in conducting state then node *X* discharges. This condition is called *contention* where one device tries to charge the node while other device tries to discharge it. In this case, there will be a direct path from V_{DD} to ground, thus, the circuit will suffer from large power dissipation. The size of the keeper is thus reduced to lower the contention current and to increase the evaluation speed [9]. But, lowering the size of the keeper will reduce the noise margin of the ciruit. Many techniques have been proposed in order to eliminate this speed-noise margin trade-off and thus to reduce the contention current.

B. Existing domino logic techniques

Wide fan-in domino logics are used in VLSI circuits and high performance microprocessors. A small PMOS keeper is required in domino logic to maintain the robustness of the circuit. If the number of inputs of domino logic increases, a large sized PMOS keeper is required. But, this in turn increases the contention current between PMOS keeper and NMOS pull down network, which degrades the performance of the circuit and increases the dynamic power loss. To eliminate this problem, a *clock delayed domino logic* (CDD) with keeper circuit is presented in [10]. Fig. 5 shows the concept of CDD, where *mp1* is the clock gated PMOS transistor and *mp2* is the keeper. Although this concept eliminates the contention current between PMOS keeper and NMOS pull down network [11], it has more power dissipation and area due to the additional nand gate.

In order to solve the trade-off between performance and noise-margin, a *high speed domino logic* (HSD) has been developed in [9] as shown in Fig. 6. In this technique, output signal *out* is connected to the keeper *mp2* via NMOS transistor *mn1* and PMOS transistor *mp3*. The gates of *mn1* and *mp3* are connected to delayed clock signal. This design reduces 60% of energy consumption as compared to standard domino logic [9].

A multi-V_{th} implementation of *high-speed domino logic* named here as MHSD was presented to reduce the power loss [9]. Its design is similar to that of HSD except that the source of keeper *mp2* is connected to signal $\overline{sleep}$ instead of

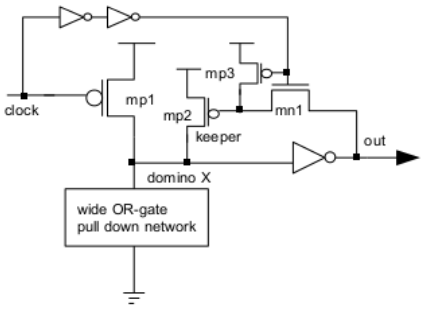

Fig. 6. High-Speed Domino Logic (HSD) [9].

V_{DD}. The signal *sleep* is '0' for active mode while it is '1' for standby mode of operation. Fig. 7 shows the circuit for MHSD logic where high V_{th} transistors are represented with a thick line in the channel region.

In order to further reduce the power dissipation, [11] have developed another domino logic named *clock delayed sleep mode* (CDSMD) domino logic. Fig. 8 shows the CDSMD logic which use sleep mode control circuitry and an odd number of inverters for the delayed clock. In CDSMD sleep signal is provided at the gate of transistors *mn2*, *mp4* and *mn5*.

The circuit shown in Fig. 9 is proposed in [12] for reducing the subthreshold leakage of domino logic circuits. This

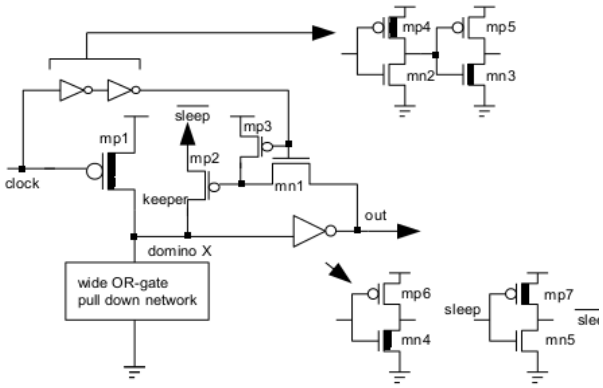

Fig. 7. Multi-V_{th} High Speed Domino Logic (MHSD) [9].

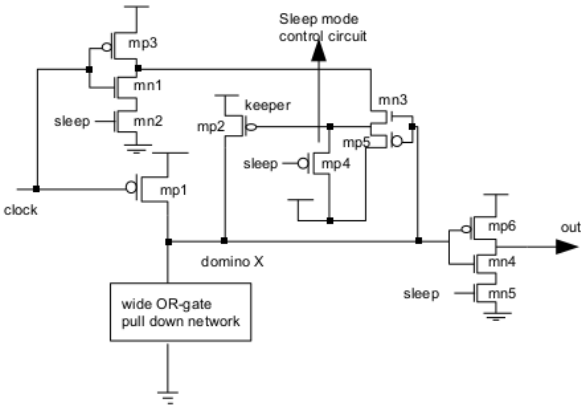

Fig. 8. Clock Delayed Sleep Mode Domino Logic (CDSMD) [11].

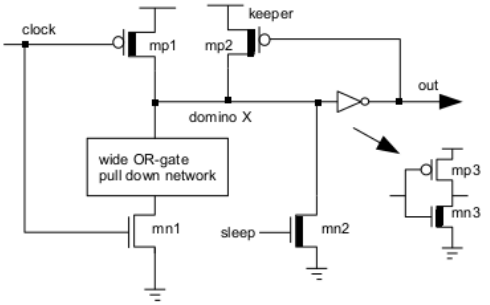

Fig. 9. Sleep Switch Dual-V_{th} Domino logic (SSDD) [12].

technique i.e *sleep switch dual domino* (SSDD), uses sleep switches and a dual threshold voltage in order to place an idle domino logic circuit into a low-leakage state. In Fig. 9 high V_{th} transistors *mp1*, *mp2*, *mn2* and *mn3* are represented with a thick line in the channel region. Another technique *PMOS only sleep switch dual-domino* (PSSDD) as shown in Fig. 10 uses PMOS only sleep switch transistors i.e. *mp4*, *mp5* and *mp7* to further reduce the leakage current in domino logic circuits [13]. In [14], work has been done to reduce the delay variation of the circuit which occur due to the feedback loop from output to input. Fig. 11 shows the circuit for *reduced delay variations domino logic* (RDVD). It uses a stack of PMOS transistors *mp2* and *mp3* as a modified keeper. Fig. 12 shows the configuration of *Foot Driven Stack Transistor Domino Logic* (FDSTDL). This circuit uses stack of NMOS transistors mn2 and mn3 to reduce the leakage current of the circuit.

In all the above designs, keeper is turned *off* during precharge phase in order to eliminate the contention current. During evaluation phase two condition exixts - pull down network is conducting or pull down network is non-conducting. If pull down network conducts, keeper is *off*. If pull down network is non-conducting, keeper is turned *on* and domino node *X* will maintain the value of V_{DD} with the help of keeper. Domino logic using CDD, HSD and CDSM have used single threshold voltage while Designs using MHSD,

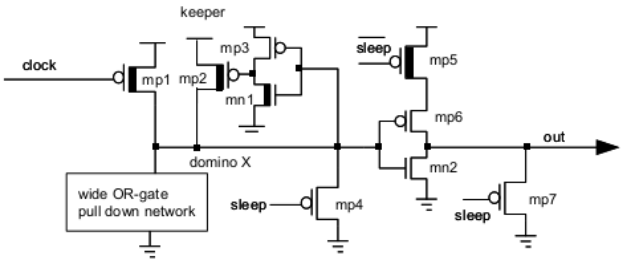

Fig. 10. PMOS Only Sleep Switch Dual-V_{th} Domino Logic (PSSDD) [13].

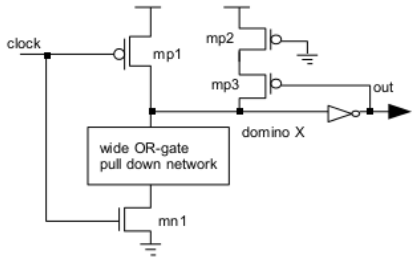

Fig. 11. Domino Logic with Reduced Delay Variations (RDVD) [14].

SSDD and PSSDD are dual threshold voltage designs. MHSD, SSDD, PSSDD and CDSM domino logic uses sleep mode control circuit which increases the area of the circuit and thus increases the power dissipation.

III. Proposed Domino Logic with Modified Keeper

Fig. 13 shows the the proposed domino logic with modified keeper circuit. The keeper consists of an NMOS transistor *mn2* which is connected in series to PMOS transistor *mp2*. The gate of *mn2* is connected to the clock while gate of *mp2* is connected to the output terminal i.e. *out*. During the precharge phase (*clock='0'*), *mp1* is *on*, which charges domino node *X*. Since transistor *mn2* is *off*, keeper is *off* at the beginning of evaluation. This will eliminate the contention current.

During evaluation phase (*clock='1'*), if pull down network conducts, node *X* will get discharged through *mn1*. In this case, since *out* is '1', *mp2* is *off* and thus keeper is *off*. If pull down network is non-conducting then, *out* is '0', *mp2* is *on* while since *clock* is '1' *mn2* is also *on*. Due to the presence of NMOS transistor in the keeper, node *X* will be retained to V_{DD}-V_{th}. But, since the domino node *X* is connected to the

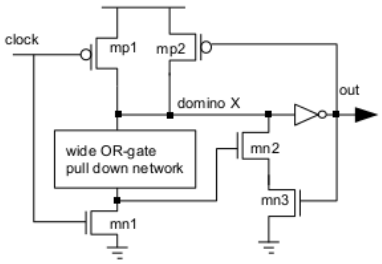

Fig. 12. Foot Driven Stack Transistor Domino Logic (FDSTDL) [15].

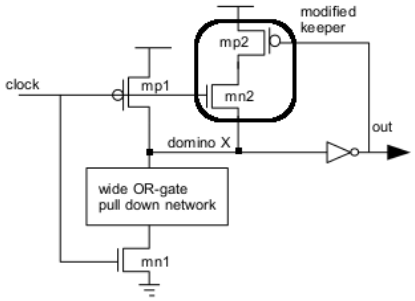

Fig. 13. Proposed domino logic.

input of the CMOS inverter, which is a noise robust device, the output of the domino logic will not be effected.

The proposed circuit is similar to standard domino logic except an addition of NMOS transistor in the modified keeper. This NMOS transitor is used in the proposed design to keep the keeper *off* at the beginning of evaluation and thus to eliminate the contention current and to reduce the power dissipation. The proposed design uses single threshold voltage without any sleep signal which reduces the area as compared to above mentioned designs.

Fig. 14 shows the output waveforms of the proposed domino logic. Here, v(vclk) is the voltage of input *clock*, v(v1) is input *i1*, v(vx) is the domino node *X* and v(vout) is the voltage of terminal *out*. The values of remaining inputs *i2-i8* is '0' and are not shown in the waveforms. The inputs (clock and i1) are taken such that to present the dynamic and static behavior of the proposed design. The rise time, fall time and delay of the input *i1* is 7.77×10^{-10} s, 7.77×10^{-10} s and 1×10^{-9} s respectively. The rise time, fall time and delay of output *out* is 4.35×10^{-9} s, 4.12×10^{-9} s and 3.65×10^{-9} s respectively.

IV. Results and Discussion

The Ngspice circuit simulator is used for simulating purpose. The 16nm PTM (predictive technology model) (level=54, version=4.0),is used to simulate the proposed technique as well as existing techniques of domino logic. The threshold voltages used during the simulation are mentioned in Table I. The supply voltage for all the designs is 0.9V. The width of PMOS transistor is 250nm while the width of NMOS transistors is 100nm. The width of the keeper transistor is kept at a lower value than that of width of NMOS transitors used in the design. The aspect ratio i.e. W/L of keeper is lowered from 6 to 1. The maximum width of keeper is 96nm while the minimum width is 16nm. The 8-input and 16-input OR gates has been chosen as the verifying circuits, because domino logic is usually used for wide fan-in OR gates. Every domino logic circuit is simulated to find dynamic power dissipation, static power dissipation, propagation delay and PDP for each value of W/L of keeper.

A. Results for 8-bit OR gate

Table II shows the dynamic power dissipation for various domino logic techniques. Fig. 15 shows the graphical representation of the dynamic power for the proposed and existing domino logic techniques. Table III shows the percentage comparison of dynamic power of proposed technique with respect to existing techniques. Positive percentage in Table III means that the existing technique has more dynamic power dissipation than the proposed technique. A negative percentage means that the existing technique have less dynamic power dissipation than the proposed technique. The dynamic power of the proposed technique is reduced significantly as compared to CDD, HSD and MHSD logics. There is a small increase in dynamic power in proposed technique as compared to CDSMD, SSDD, PSSDD and RDVD and FDSTDL logics. It is increased to a maximum of 8.00% as compared to CDSMD for W/L=6. It is also observed that dynamic power dissipation for a domino logic is almost constant for different W/L ratio of the keeper transistor.

TABLE I
Values of V_{TH} used during simulation

	NMOS	PMOS
Single V_{th} Designs	0.68V	-0.68V
Dual V_{th} Designs	0.68V, 0.48V	-0.68V, -0.43V

Table IV shows the average static power dissipation for various domino logic techniques. Fig. 16 shows the graphical representation of the static power for the proposed and existing domino logic techniques. Table V shows the percentage comparison of static power of proposed technique with respect to existing techniques. The static power dissipation of the proposed technique is reduced as compared to the existing domino logic techniques. For W/L=6, the static power is reduced to 99.99% as compared to CDD while to 8.99% as compared to FDSTDL. For W/L=1, the static power is reduced to 99.99% as compared to CDD while to -22.69% as compared to RDVD.

Table VI shows the propagation delay for various domino logic techniques. Fig. 17 shows the graphical representation of the delay for the proposed and existing domino logic techniques. Table VII shows the percentage comparison of delay of proposed technique with respect to existing techniques. For W/L=6, the delay of the proposed technique is reduced by 38.11% as compared to FDSTDL and it is increased to 23.38% as compared to SSDD. The delay of the proposed technique is increased as compared to the MHSD, SSDD and PSSDD techniques. This is because these techniques are dual threshold voltage techniques and thus have better performance than the proposed technique. The delay of proposed technique is reduced as compared to the rest of the techniques.

Table IX shows the PDP for various domino logic techniques. Fig. 18 shows the graphical representation of ppd for the proposed and existing domino logic techniques. Table X shows the percentage comparison of PDP of proposed technique with respect to existing techniques. It can be seen that PDP of the proposed technique is least as compared to the other techniques. For W/L=6, PDP is reduced to 99.99% as compared to CDD while it is reduced to 38.09% as compared to SSDD. PDP values of RDVD and FDSTDL are very close to the PDP values of proposed technique. Fig. 19 shows the

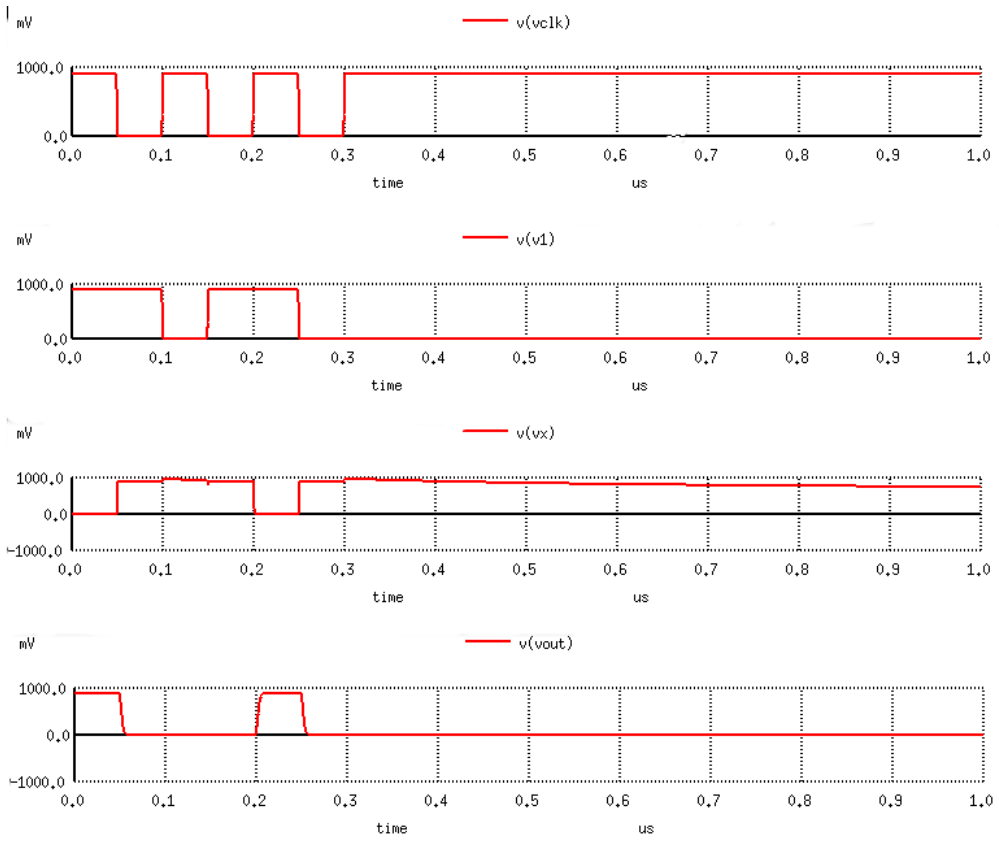

Fig. 14. Output waveforms of proposed domino logic for *i2-i8*='0'.

TABLE II
DYNAMIC POWER (WATTS) OF VARIOUS DOMINO LOGIC TECHNIQUES FOR 8-BIT OR GATE

Dyn. Power	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL	Proposed
W/L=6	2.78×10^{-14}	1.34×10^{-15}	1.29×10^{-15}	8.25×10^{-16}	8.85×10^{-16}	9.09×10^{-16}	9.12×10^{-16}	5.15×10^{-16}	8.91×10^{-16}
W/L=5	2.78×10^{-14}	1.04×10^{-15}	1.23×10^{-15}	8.25×10^{-16}	8.76×10^{-16}	9.08×10^{-16}	8.86×10^{-16}	3.94×10^{-16}	8.81×10^{-16}
W/L=4	2.78×10^{-14}	9.50×10^{-16}	1.17×10^{-15}	8.25×10^{-16}	8.67×10^{-16}	9.06×10^{-16}	8.67×10^{-16}	3.61×10^{-16}	8.69×10^{-16}
W/L=3	2.78×10^{-14}	9.04×10^{-16}	1.10×10^{-15}	8.25×10^{-16}	8.58×10^{-16}	9.05×10^{-16}	8.52×10^{-16}	3.47×10^{-16}	8.57×10^{-16}
W/L=2	2.78×10^{-14}	8.70×10^{-16}	1.01×10^{-15}	8.25×10^{-16}	8.50×10^{-16}	9.04×10^{-16}	8.39×10^{-16}	3.37×10^{-16}	8.43×10^{-16}
W/L=1	2.78×10^{-14}	8.54×10^{-16}	9.67×10^{-16}	8.24×10^{-16}	8.45×10^{-16}	9.04×10^{-16}	8.27×10^{-16}	3.33×10^{-16}	8.31×10^{-16}

TABLE III
PERCENTAGE COMPARISON OF DYNAMIC POWER FOR 8-BIT OR GATE W.R.T. PROPOSED TECHNIQUE

Dynamic Power	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL
W/L=6	96.79%	33.51%	30.93%	-8.00%	-0.68%	1.98%	2.30%	-73.01%
W/L=5	96.83%	15.29%	28.37%	-6.79%	-0.57%	2.97%	0.56%	-123.60%
W/L=4	96.87%	8.53%	25.73%	-5.33%	-0.23%	4.08%	-0.23%	-140.72%
W/L=3	96.92%	5.20%	22.09%	-3.88%	0.12%	5.30%	-0.59%	-146.97%
W/L=2	96.97%	3.10%	16.53%	-2.18%	0.82%	6.75%	-0.48%	-140.15%
W/L=1	97.01%	2.69%	14.06%	-0.85%	1.66%	8.08%	-0.48%	-149.55%

TABLE IV
STATIC POWER(WATTS) OF VARIOUS DOMINO LOGIC TECHNIQUES FOR 8-BIT OR GATE

Static Power	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL	Proposed
W/L=6	8.55×10^{-6}	8.41×10^{-9}	5.33×10^{-9}	1.04×10^{-9}	1.44×10^{-9}	3.99×10^{-9}	1.19×10^{-9}	7.96×10^{-10}	7.24×10^{-10}
W/L=5	8.55×10^{-6}	6.89×10^{-9}	5.28×10^{-9}	1.05×10^{-9}	1.44×10^{-9}	3.99×10^{-9}	8.79×10^{-10}	7.81×10^{-10}	7.10×10^{-10}
W/L=4	8.55×10^{-6}	5.42×10^{-9}	5.27×10^{-9}	1.05×10^{-9}	1.44×10^{-9}	3.99×10^{-9}	7.96×10^{-10}	7.66×10^{-10}	6.97×10^{-10}
W/L=3	8.55×10^{-6}	4.05×10^{-9}	5.25×10^{-9}	1.06×10^{-9}	1.43×10^{-9}	3.99×10^{-9}	7.11×10^{-10}	7.52×10^{-10}	6.76×10^{-10}
W/L=2	8.55×10^{-6}	2.77×10^{-9}	5.29×10^{-9}	1.05×10^{-9}	1.43×10^{-9}	3.99×10^{-9}	6.27×10^{-10}	7.36×10^{-10}	6.75×10^{-10}
W/L=1	8.55×10^{-6}	2.15×10^{-9}	5.28×10^{-9}	1.06×10^{-9}	1.43×10^{-9}	3.98×10^{-9}	5.42×10^{-10}	7.22×10^{-10}	6.65×10^{-10}

TABLE V
PERCENTAGE COMPARISON OF STATIC POWER FOR 8-BIT OR GATE W.R.T. PROPOSED TECHNIQUE

Static Power	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL
W/L=6	99.99%	91.39%	86.40%	30.48%	49.72%	81.85%	39.08%	8.99%
W/L=5	99.99%	89.70%	86.55%	32.12%	50.69%	82.18%	19.23%	9.09%
W/L=4	99.99%	87.14%	86.76%	33.65%	51.43%	82.51%	12.38%	8.95%
W/L=3	99.99%	83.31%	87.12%	35.92%	52.73%	83.04%	4.92%	10.05%
W/L=2	99.99%	75.63%	87.23%	35.90%	52.80%	83.06%	-7.74%	8.29%
W/L=1	99.99%	69.07%	87.41%	37.12%	53.50%	83.29%	-22.69%	7.89%

TABLE VI
DELAY(S) OF VARIOUS DOMINO LOGIC TECHNIQUES FOR 8-BIT OR GATE

Delay	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL	Proposed
W/L=6	4.76×10^{-9}	7.41×10^{-9}	3.84×10^{-9}	5.80×10^{-9}	3.78×10^{-9}	4.27×10^{-9}	4.84×10^{-9}	7.53×10^{-9}	4.66×10^{-9}
W/L=5	4.49×10^{-9}	5.40×10^{-9}	3.81×10^{-9}	5.80×10^{-9}	3.75×10^{-9}	4.26×10^{-9}	4.68×10^{-9}	5.40×10^{-9}	4.59×10^{-9}
W/L=4	4.43×10^{-9}	4.84×10^{-9}	3.79×10^{-9}	5.79×10^{-9}	3.71×10^{-9}	4.25×10^{-9}	4.57×10^{-9}	4.83×10^{-9}	4.53×10^{-9}
W/L=3	4.39×10^{-9}	4.60×10^{-9}	3.75×10^{-9}	5.79×10^{-9}	3.68×10^{-9}	4.24×10^{-9}	4.48×10^{-9}	4.60×10^{-9}	4.46×10^{-9}
W/L=2	4.36×10^{-9}	4.45×10^{-9}	3.70×10^{-9}	5.79×10^{-9}	3.64×10^{-9}	4.23×10^{-9}	4.40×10^{-9}	4.45×10^{-9}	4.39×10^{-9}
W/L=1	4.34×10^{-9}	4.38×10^{-9}	3.67×10^{-9}	5.79×10^{-9}	3.62×10^{-9}	4.23×10^{-9}	4.33×10^{-9}	4.38×10^{-9}	4.33×10^{-9}

TABLE VII
PERCENTAGE COMPARISON OF DELAY FOR 8-BIT OR GATE W.R.T. PROPOSED TECHNIQUE

Delay	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL
W/L=6	2.10%	37.11%	-21.35%	19.66%	-23.28%	-9.13%	3.72%	38.11%
W/L=5	-2.23%	15.00%	-20.47%	20.86%	-22.40%	-7.75%	1.92%	15.00%
W/L=4	-2.26%	6.40%	-19.53%	21.76%	-22.10%	-6.59%	0.88%	6.21%
W/L=3	-1.59%	3.04%	-18.93%	22.97%	-21.20%	-5.19%	0.45%	3.04%
W/L=2	-0.69%	1.35%	-18.65%	24.18%	-20.60%	-3.78%	0.23%	1.35%
W/L=1	0.23%	1.14%	-17.98%	25.22%	-19.61%	-2.36%	0.00%	1.14%

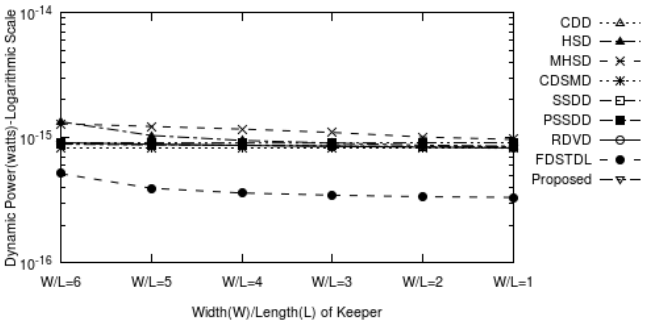

Fig. 15. Dynamic Power of various domino logic techniques for 8-bit OR gate.

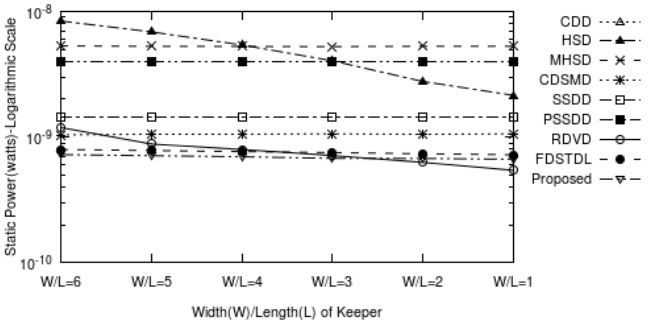

Fig. 16. Static Power of various domino logic techniques for 8-bit OR gate.

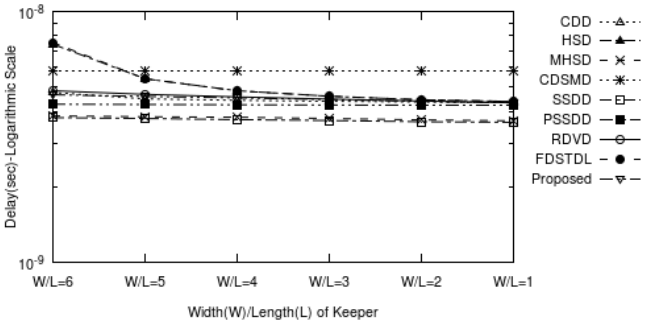

Fig. 17. Delay of various domino logic techniques for 8-bit OR gate.

comparison of PDP values RDVD, FDSTDL and proposed domino logic techniques.

Table XI shows the total number of transistors per domino logic module. The no. of transistors in the pull down network are not considered. There are six transistors in the proposed design which is minimum as compared to the existing techniques.

Rise time, fall time, delay, minimum output level (Min O/P) and maximum output level (Max O/P) of various domino logic techniques are shown in table VIII. The minimum input level is 0 V and maximum input level is 0.9 V. The parameter *delay* is the delay time from $t = 0ns$. All the parameters in Table VIII are for $W/L = 6$.

TABLE VIII
PARAMETERS OF OUTPUT WAVEFORM FOR VARIOUS DOMINO LOGIC CIRCUIT FOR 8-BIT OR GATE

Parameter	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL	Proposed
Rise Time *(s)*	3.74×10^{-9}	4.21×10^{-9}	1.59×10^{-9}	3.74×10^{-9}	1.52×10^{-9}	6.03×10^{-9}	3.82×10^{-9}	4.04×10^{-9}	4.35×10^{-9}
Fall Time *(s)*	4.12×10^{-9}	4.12×10^{-9}	4.12×10^{-9}	9.52×10^{-9}	4.12×10^{-9}	2.11×10^{-9}	4.12×10^{-9}	4.13×10^{-9}	4.12×10^{-9}
Delay *(s)*	3.95×10^{-9}	3.99×10^{-9}	3.28×10^{-9}	3.65×10^{-9}	3.24×10^{-9}	3.23×10^{-9}	3.76×10^{-9}	4.01×10^{-9}	3.65×10^{-9}
Min O/P *(V)*	-1.25×10^{-4}	1.58×10^{-6}	1.32×10^{-4}	-9.55×10^{-5}	1.71×10^{-4}	7.49×10^{-5}	-1.43×10^{-4}	-1.77×10^{-4}	-8.77×10^{-5}
Max O/P *(V)*	0.9	0.9	0.9	0.9	0.89	0.9	0.9	0.9	0.9

TABLE IX
PDP(WATTS-S) OF VARIOUS DOMINO LOGIC TECHNIQUES FOR 8-BIT OR GATE

PDP	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL	Proposed
W/L=6	4.07×10^{-14}	6.23×10^{-17}	2.04×10^{-17}	6.04×10^{-18}	5.44×10^{-18}	1.70×10^{-17}	5.75×10^{-18}	5.99×10^{-18}	3.37×10^{-18}
W/L=5	3.89×10^{-14}	3.72×10^{-17}	2.01×10^{-17}	6.07×10^{-18}	5.40×10^{-18}	1.70×10^{-17}	4.11×10^{-18}	4.22×10^{-18}	3.26×10^{-18}
W/L=4	3.79×10^{-14}	2.62×10^{-17}	1.99×10^{-17}	6.08×10^{-18}	5.32×10^{-18}	1.69×10^{-17}	3.63×10^{-18}	3.69×10^{-18}	3.16×10^{-18}
W/L=3	3.75×10^{-14}	1.86×10^{-17}	1.97×10^{-17}	6.11×10^{-18}	5.26×10^{-18}	1.69×10^{-17}	3.18×10^{-18}	3.46×10^{-18}	3.01×10^{-18}
W/L=2	3.73×10^{-14}	1.23×10^{-17}	1.95×10^{-17}	6.10×10^{-18}	5.20×10^{-18}	1.68×10^{-17}	2.75×10^{-18}	3.27×10^{-18}	2.96×10^{-18}
W/L=1	3.71×10^{-14}	9.42×10^{-18}	1.94×10^{-17}	6.12×10^{-18}	5.18×10^{-18}	1.68×10^{-17}	2.35×10^{-18}	3.16×10^{-18}	2.88×10^{-18}

TABLE X
PERCENTAGE COMPARISON OF PDP FOR 8-BIT OR GATE W.R.T. PROPOSED TECHNIQUE

PDP	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL
W/L=6	99.99%	94.59%	83.52%	44.21%	38.09%	80.22%	41.42%	43.74%
W/L=5	99.99%	91.24%	83.79%	46.26%	39.63%	80.80%	20.75%	22.70%
W/L=4	99.99%	87.95%	84.16%	48.05%	40.64%	81.34%	13.08%	14.53%
W/L=3	99.99%	83.84%	84.71%	50.72%	42.80%	82.19%	5.50%	12.93%
W/L=2	99.99%	75.99%	84.86%	51.45%	43.13%	82.44%	-7.38%	9.62%
W/L=1	99.99%	69.52%	85.19%	53.13%	44.56%	82.95%	-22.29%	9.25%

TABLE XI
NO. OF TRANSISTORS PER DOMINO LOGIC MODULE FOR VARIOUS TECHNIQUES

CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL	Proposed
12	10	12	11	6	11	6	7	6

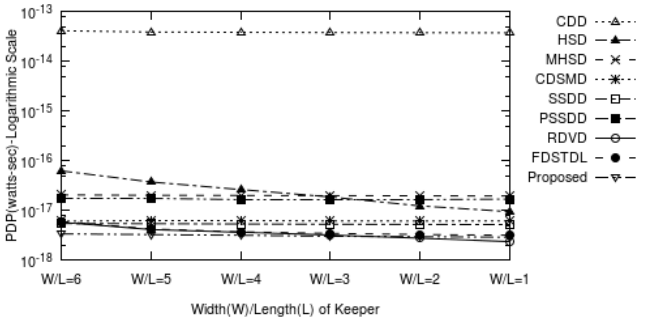

Fig. 18. Power-Delay-Product(PDP) of various domino logic techniques for 8-bit OR gate.

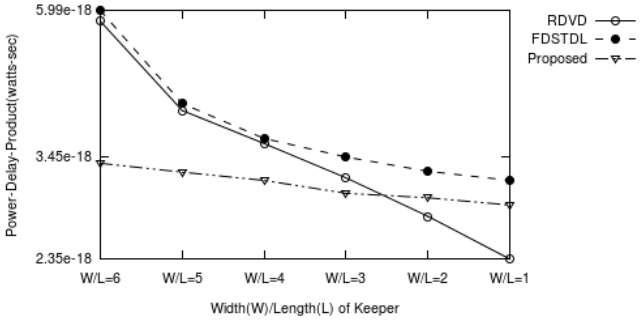

Fig. 19. Power-Delay-Product(PDP) of RDVD, FDSTDL and Proposed technique for 8-bit OR gate.

B. Results for 16 bit OR gate

Simulation have been carried out for existing and proposed techniques for 16 bit OR gate. Table XII shows the results for PDP values for 16-bit OR gate. Table XIII shows the comparsion of proposed techniques with respect to the existing techniques. For W/L=6, PDP is reduced to 99.99% as compared to CDD while it is reduced to 33.46% as compared to CDSMD.

C. Monte Carlo Simulation and Noise Analysis

An unavoidable process variations may occur during the integrated circuit fabrication, which may impact the static and dynamic characteristics of the circuit. In Monte Carlo analysis, various parameters are selected at random so as to check the performance of the circuit during variations. Various parameters varied for MOS transistors during *Monte Carlo* simulation are threshold voltage, mobility, oxide thickness,

TABLE XII
PDP(WATTS-S) OF VARIOUS DOMINO LOGIC TECHNIQUES FOR 16-BIT OR GATE

PDP	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL	Proposed
W/L=6	4.15×10^{-14}	6.31×10^{-17}	3.03×10^{-17}	4.15×10^{-18}	5.49×10^{-18}	1.68×10^{-17}	4.81×10^{-18}	6.19×10^{-18}	2.76×10^{-18}
W/L=5	3.87×10^{-14}	3.74×10^{-17}	3.01×10^{-17}	4.17×10^{-18}	5.42×10^{-18}	1.67×10^{-17}	4.25×10^{-18}	4.38×10^{-18}	2.62×10^{-18}
W/L=4	3.82×10^{-14}	2.65×10^{-17}	3.01×10^{-17}	4.19×10^{-18}	5.38×10^{-18}	1.66×10^{-17}	3.76×10^{-18}	3.83×10^{-18}	2.49×10^{-18}
W/L=3	3.80×10^{-14}	1.89×10^{-17}	3.04×10^{-17}	4.21×10^{-18}	5.34×10^{-18}	1.66×10^{-17}	3.31×10^{-18}	3.58×10^{-18}	2.35×10^{-18}
W/L=2	3.76×10^{-14}	1.25×10^{-17}	3.10×10^{-17}	4.23×10^{-18}	5.28×10^{-18}	1.65×10^{-17}	2.88×10^{-18}	3.40×10^{-18}	2.23×10^{-18}
W/L=1	3.75×10^{-14}	9.61×10^{-18}	3.18×10^{-17}	4.25×10^{-18}	5.25×10^{-18}	1.65×10^{-17}	2.46×10^{-18}	3.29×10^{-18}	2.11×10^{-18}

TABLE XIII
PERCENTAGE COMPARISON OF PDP W.R.T. PROPOSED TECHNIQUE FOR 16-BIT OR GATE

PDP	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL
W/L=6	99.99%	95.63%	90.88%	33.46%	49.69%	83.53%	42.61%	55.44%
W/L=5	99.99%	92.99%	91.30%	37.19%	51.70%	84.28%	38.38%	40.13%
W/L=4	99.99%	90.62%	91.74%	40.63%	53.73%	85.02%	33.80%	34.95%
W/L=3	99.99%	87.58%	92.27%	44.21%	55.98%	85.83%	28.92%	34.35%
W/L=2	99.99%	82.23%	92.81%	47.27%	57.77%	86.52%	22.55%	34.35%
W/L=1	99.99%	78.05%	93.36%	50.45%	59.82%	87.24%	14.28%	35.81%

TABLE XIV
RESULTS FOR MONTE CARLO ANALYSIS FOR PROPOSED CIRCUIT

Parameters	8-bit OR gate	16-bit OR gate
Mean (μ)(nW)	0.538	0.533
Standard Deviation (σ)(nW)	0.274	0.330
Variability (σ/μ)	0.510	0.561

TABLE XV
UNITY NOISE GAIN FOR VARIOUS DOMINO LOGIC TECHNIQUES FOR 16-BIT OR GATE

Technique	Unity Noise Gain (*Volts*)
CDD	0.705
HSD	0.761
MHSD	0.456
CDSMD	0.645
SSDD	0.349
PSSDD	0.340
RDVD	0.675
FDSTDL	0.755
Proposed	0.510

width and length. Generated random values for most of the parameters are nominal value plus variation drawn from Gaussian distribution with mean 0 and standard deviation 0.1 (relative to nominal), divided by sigma 3.

Fig. 20 shows the transient output for 50 runs of simulation for 8-bit OR gate and 16-bit OR gate. For the proposed domino logic the worst case is chosen with $0.9V_{DD}$ and 130°C and best case is chosen with $1.1V_{DD}$ at -30°C. Table XIV shows the results of monte carlo simulation for the proposed circuit. It can be seen that proposed circuit have lower variability and standard deviation. Thus the proposed circuit is reliable and robust.

The proposed design is suitable for low power applications with low power dissipation, low area and a little loss in performance. In order to perform the noise analysis, Unity Noise Gain (UNG) [15] is calculated. UNG is the amount of DC noise at all inputs that result in the same amount of noise at the output node [16]. Table XV shows the UNG of various domino logic techniques. A higher value of UNG shows better noise immunity.

Table XVI shows the comparison of the results (in percentages) showing the advantages and disadvantages of the proposed technique in relation to each of the existing ones. Here, the percentage shows the increase in performance of the proposed technique and is calulated using equation below:

$$Increase\ in\ Performance(\%) = \frac{PARAM_{existing} - PARAM_{\text{proposed}}}{PARAM_{proposed}} \cdot 100\% \quad (2)$$

where, $\text{PARAM}_{\text{existing}}$ is the parameter of the existing technique and $\text{PARAM}_{\text{proposed}}$ is the parameter of the proposed technique. In table XVI parameter *Pdyn* is the dynamic power, *Pstat* is the static power, *Delay* is the propagation delay, *Trise* is the rise time and *Tfall* is the fall time for 8-bit OR gate for W/L=6.

Below is the list which gives the summary of various techniques for domino logic.

- **CDD:** Low power dissipation. Large area due to nand gate.
- **HSD:** Reduces the tradeoff between performance and noise margin.
- **MHSD:** Dual threshold voltages are used in the design to reduce the leakage as well as delay.
- **CDSMD:** Sleep mode control circuitry is used thus, area is increased. High noise immunity.
- **SSDD:** Sleep switches as well as dual threshld voltages are used. More power, area and delay efficient. Low noise immunity.
- **PSSDD:** PMOS sleep transistors and a dual-threshold voltage CMOS technology are used to place an idle domino logic circuit into a low leakage state. Low noise immunity.
- **RDVD:** A modified keeper with a stack of two PMOS transistors are used. Less area with improved performance.
- **FDSTDL:** A stack of two NMOS transistors are used for reducing leakage. High noise immunity.

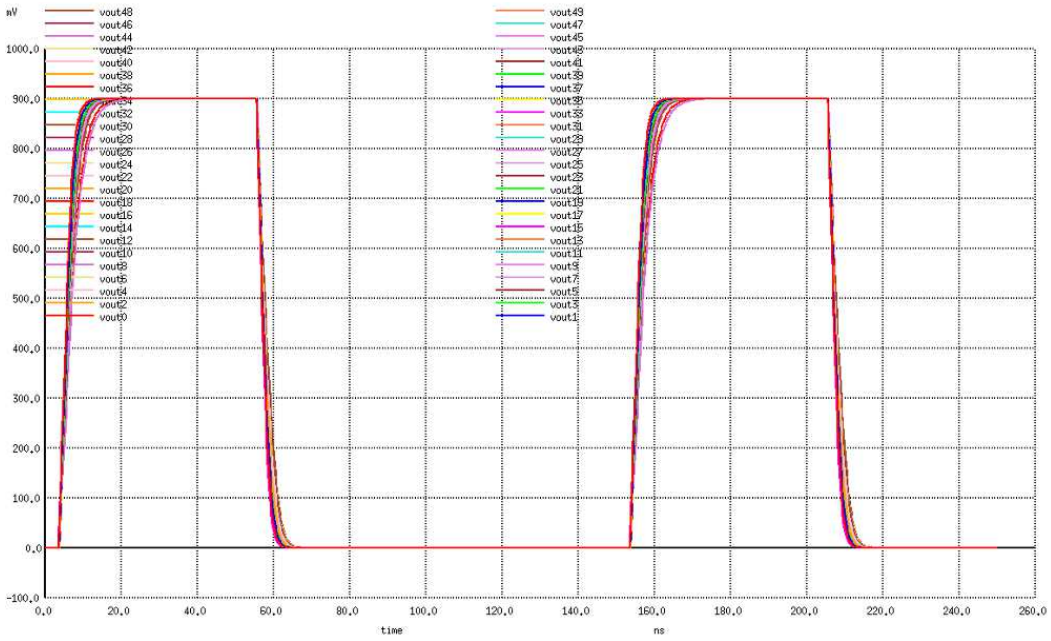

Fig. 20. Output of the Proposed Domino Logic during *Monte Carlo* Simulation.

TABLE XVI
COMPARISON OF PROPOSED TECHNIQUE WITH OTHER TECHNIQUES IN PERCENTAGES

Percentage(%)	Pdyn	Pstat	Delay	Trise	Tfall	PDP	Area	UNG
CDD	302009	118180117	215	-14	0	120770480	100	38
HSD	5039	106171	5901	-3	0	174810	67	49
MHSD	4478	63549	-1760	-63	0	50676	100	-10
CDSMD	741	4385	2446	-14	131	7924	83	26
SSDD	-67	9889	-1888	-65	0	6152	0	-31
PSSDD	202	45110	-837	38	-49	40556	83	33
RDVD	236	6415	386	-12	0	7069	0	32
FDSTDL	-4220	987	6159	-7	0	6931	17	48

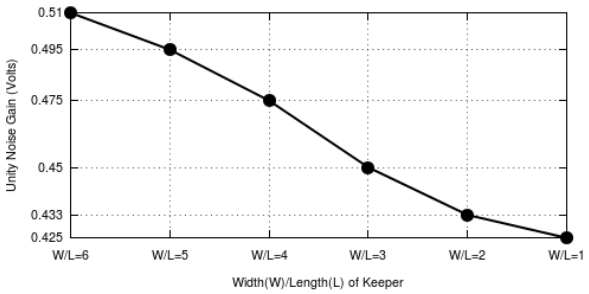

Fig. 21. Noise Analysis of Proposed technique for 16-bit OR gate.

- **Proposed:** A stack of one PMOS and one NMOS transistor is used as a modified keeper. Low leakage current.

V. CONCLUSION

The low power circuit has the feature of low power but with reduced speed. The proposed domino logic is best suited for low power applications without any area overhead. Proposed domino logic with modified keeper consists of NMOS and PMOS transistor in series. The gate of the NMOS transistor is connected to the clock while the gate of PMOS transistor is connected to the output terminal. This configuration will eliminate the contention current and reduces the power dissipation of the circuit. The PDP is improved as compared to *clock delayed domino logic* (CDD), *high speed domino logic* (HSD), *multi threshold high speed domino logic* (MHSD), *clock delayed sleep mode domino logic* (CDSMD), *sleep switch domino logic* (SSDD), *PMOS* only sleep switch domino logic (PSSDD), *reduced delay variations domino logic* (RDVD) and *Foot Driven Stack Transistor Domino Logic* (FDSTDL). Results have been calculated for different values of the W/L of keeper in order to check the behavior of the designs for lower widths of the keeper. For all values of W/L ranging for 1 to 6, the proposed design shows significant improvement in PDP. Thus, the proposed domino logic in an improved design with lesser area as compared to previous existing designs.

REFERENCES

[1] R. R. Schaller, "Moore's law: past, present and future," *IEEE spectrum*, vol. 34, no. 6, pp. 52–59, 1997.
[2] ITRS, "International technology roadmap for semiconductors 2.0 executive report," 2015.
[3] S. Singhal and A. Mehra, "A novel technique for static leakage reduction in 16 nm cmos design," *International Journal of Electronics Letters*, pp. 1–14, 2018.

[4] K. Roy and S. C. Prasad, *Low-power CMOS VLSI circuit design*. John Wiley & Sons, 2009.

[5] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolic, *Digital integrated circuits*. Prentice hall Englewood Cliffs, 2002, vol. 2.

[6] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low-power cmos digital design," *IEICE Transactions on Electronics*, vol. 75, no. 4, pp. 371–382, 1992.

[7] M. R. Nandini, P. Mor, and J. Keller, "Performance analysis of different dynamic cmos logics," *International Journal of Electronics, Electrical and Computational System*, vol. 6, 2017.

[8] S. M. Sharroush, Y. S. Abdalla, A. A. Dessouki, and E.-S. A. El-Badawy, "Compensating for the keeper current of cmos domino logic using a well designed nmos transistor," in *Proceedings of 26th National Radio Science Conference (NRSC2009)*, 2009, pp. 1–8.

[9] M. W. Allam, M. H. Anis, and M. I. Elmasry, "High-speed dynamic logic styles for scaled-down cmos and mtcmos technologies," in *Proceedings of the 2000 international symposium on Low power electronics and design*. ACM, 2000, pp. 155–160.

[10] A. Alvandpour, P. Larsson-Edefors, and C. Svensson, "A leakage-tolerant multi-phase keeper for wide domino circuits," in *Electronics, Circuits and Systems, 1999. Proceedings of ICECS'99. The 6th IEEE International Conference on*, vol. 1. IEEE, 1999, pp. 209–212.

[11] K.-I. Oh and L.-S. Kim, "A clock delayed sleep mode domino logic for wide dynamic or gate," in *Low Power Electronics and Design, 2003. ISLPED'03. Proceedings of the 2003 International Symposium on*. IEEE, 2003, pp. 176–179.

[12] V. Kursun and E. G. Friedman, "Sleep switch dual threshold voltage domino logic with reduced standby leakage current," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 12, no. 5, pp. 485–496, 2004.

[13] Z. Liu and V. Kursun, "Pmos-only sleep switch dual-threshold voltage domino logic in sub-65-nm cmos technologies," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, no. 12, pp. 1311–1319, 2007.

[14] G. Palumbo, M. Pennisi, and M. Alioto, "A simple circuit approach to reduce delay variations in domino logic gates," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 10, pp. 2292–2300, 2012.

[15] S. Garg and T. K. Gupta, "Low power domino logic circuits in deep-submicron technology using cmos," *Engineering Science and Technology, an International Journal*, 2018.

[16] F. Moradi, H. Mahmoodi, and A. Peiravi, "A high speed and leakage-tolerant domino logic for high fan-in gates," in *Proceedings of the 15th ACM Great Lakes symposium on VLSI*. ACM, 2005, pp. 478–481.

Single-Stage Operational Transconductance Amplifier Design in UTBSOI Technology Based on g_m/I_d Methodology

Rekib Uddin Ahmed, Eklare Akshay Vijaykumar, and Prabir Saha

***Abstract*—The downscaling of complementary metal-oxide-semiconductor (CMOS) technology is approaching its limits imposed by short-channel effects (SCE), thereby multi-gate MOSFETs have been proposed to extend the scalability. Ultra-thin-body silicon-on-insulator (UTBSOI) transistor is one of the dual-gated devices which offers better immunity towards SCEs. In this paper, two designs have been proposed for single-stage operational transconductance amplifiers (OTA) using the CMOS and UTBSOI. The CMOS based OTA (CMOS-OTA) has been designed where sizing (W/L) of the constituting MOSFETs have been evaluated through g_m/I_d methodology and the same OTA topology has been simulated using UTBSOI (UTBSOI-OTA) considering the same W/L. The DC simulation is carried out over the BSIM3v3 model to store the operating point parameters in the form of graphical models. The mathematical expressions for performance specifications have been applied over the graphical models to evaluate the required W/L. Individual comparisons between the two proposed designs have also been carried out for further applications. Based on simulation results at the schematic level, the UTBSOI-OTA has higher DC gain of $\approx$ 33.26% and lesser power consumption of $\approx$ 2.81% over the CMOS-OTA. Moreover, comparative analysis of performance parameters like DC gain and common-mode rejection ratio (CMRR), have been compared with the best-reported paper so far. In addition to this, the UTBSOI-OTA has been applied to practical integrator circuits for further verification.**

***Index Terms*—BSIM-IMG, g_m/I_d methodology, single-stage OTA, UTBSOI.**

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I. Introduction

THE demand for analog integrated circuit (IC) design will never diminish since the input signals fed to the transducers of any systems are analog in nature. CMOS analog design is a skill that develops upon experiences and intuition as there exists no specific set of rules which can be followed to design some analog blocks like OTA. In OTAs, the W/L of constituting MOSFETs moderately depend upon its performance parameters like DC gain, unity-gain bandwidth (UGB), slew rate (SR), input common-mode range (V_{iCMR}), common-mode rejection ratio (CMRR), and power. Conventional sizing procedure [1] calculated the W/L using the square-law model which was a tedious hand calculation design approach. On the other hand, more accurate and complex models [2] have been incorporated in the modern simulators. There exists a huge discrepancy between square-law and the models in simulators which prevents the possibility to meet the desired performance of the circuit. Though many advanced topologies for the single-stage OTA [3]–[10] have been reported so far but their sizing (W/L) procedure has not been discussed. In brief, although the circuit analysis for the OTAs is available, an elaborate description of the sizing procedure is lacking in the literature. The transconductance-to-drain current ratio (g_m/I_d) methodology [11] is an effective sizing procedure which can be applied to design any analog circuits.

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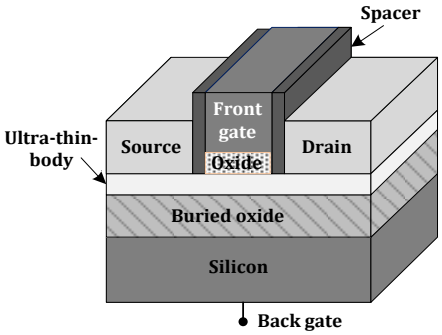

Fig. 1. Schematics showing 3-D view of the UTBSOI transistor.

Moreover, the process variation parameters of the non-classical MOSFETs have become a major cause in degrading the performance of such analog circuits. The short-channel effects (SCE) are becoming prone as the device dimension is scaled down to the nanoscale regime [12], [13]. Thus, a large abnormality is observed in the circuits produced by the present manufacturing process. Thereby, multi-gate MOSFETs like double-gate MOSFET, FinFET, and ultra-thin-body silicon-on-insulator (UTBSOI) have been proposed to overcome the limitations of SCEs [13]. The UTBSOI MOSFET as shown in Fig. 1 is a dual gated transistor has better scalability and superior controllability of gates over the shorter channel region. The superior gate controllability increases the transconductance, results in higher current drivability which in turn enhances the device speed. The UTBSOI also offers the flexibility of multiple threshold voltage control through its back-gate bias [14]. In low-power and high performance systems, the MOSFETs with different threshold voltages are

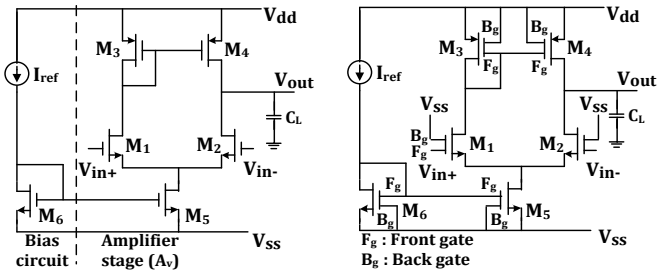

Fig. 2. Design of single-stage OTA using (a) CMOS, (b) UTBSOI.

TABLE I
DESIRED SINGLE-STAGE OTA SPECIFICATIONS

Specifications	Value
Technology	180 nm
Supply voltage	1.8 V
UGB	20 MHz
Open-loop DC gain (A_{vdc})	40 dB
PM	90°
CMRR	90 dB
SR	20 V/μs
$V_{iCM,min}$	-0.1 V
$V_{iCM,max}$	0.8 V
Reference current (I_{ref})	20 μA
Load capacitor	5 pF

required in the same circuit. The multiple threshold voltages in classical MOSFETs were achieved through using different channel doping concentrations. Whereas, in the UTBSOI, the same can be achieved by the use of back-gate bias instead of channel doping [15]. To utilize the benefits of UTBSOI, an accurate and fast computation model for device is required. BSIM-IMG [16] is the industry standard model for the UTB-SOI which have been validated with the hardware silicon based data from multiple technologies. However, the layout of UTBSOI is not possible till date due to the non-availability of the process-design kit in present simulators like Cadence-spectre [17].

In this paper, the g_m/I_d methodology has been adopted to design the single-stage OTA as shown in Fig. 2(a). This methodology considers intrinsic-gain (g_m/g_{ds}) versus g_m/I_d and normalized drain current (I_d/W) versus g_m/I_d graphs as the fundamental design tools to precisely calculate transistor's W/L [18], [19]. The relationship between g_m/g_{ds}, I_d/W and g_m/I_d are obtained by solving the mathematical expressions of performance parameters. The presented work in this paper improves the OTA designed in [19] with new set of specifications especially in terms of DC gain, PM, UGB, and CMRR. In addition to this, the UTBSOI- OTA [Fig. 2(b)] has been simulated at schematic level by utilizing the BSIM-IMG model. The design process has been performed in two phases: 1) The operating points parameters of both n- and p-type MOSFETs (BSIM3v3) obtained through DC simulation in spectre are stored in the form of a database, 2) This database corresponds to distinct parameters like drain current (I_d), g_m/g_{ds}, I_d/W with respect to g_m/I_d and have been used in MATLAB in the form of graphical models [Fig. 3$-$5] to calculate the W/L. The OTAs are simulated in Cadence-spectre using the generic process design kit (gpdk) 180-nm technology to extract the performance parameters. The use of UTBSOI in OTA has resulted improvements in terms of higher DC gain by $\approx 33.26\%$ and reduced power consumption by $\approx 2.81\%$ over that of CMOS-OTA.

II. PROPOSED DESIGN PROCEDURE

A single-stage five transistor OTA has got many uses in complex, analog, and mixed-signal systems. Despite its simplicity, the OTA has the frequency response in a desired limit. The transfer function of the OTA is expressed in terms of the operating point parameters as [21], [22]

$$A_v(s) = \frac{g_{m1,2}R_o}{1 + sC_LR_o} \tag{1}$$

where $g_{m1,2}$ is transconductance of the input pair ($M_{1,2}$), C_L is the load capacitance, and R_o =1/($g_{ds3} + g_{ds4}$) is the output resistance. The OTA has only one left-half plane (LHP) pole and no zero which ensures stability of the circuit. The PM is 90° due to a single pole.

The design procedure begins with information like power supply, technology, temperature, and the desired specifications. The required information, as given in Table I, have been taken from different sources [1], [19] and the g_m/I_d methodology has been employed to evaluate the sizing of such OTA. The DC simulation is performed on both n- and p-type MOSFETs where the drain-to-source voltage (V_{ds}) is set to ($V_{dd} - V_{ss}$)/3 and gate-to-source voltage (V_{gs}) sweep from -0.6 to 1 V is used. Since it is customary to use large channel width (W) in analog circuits, so the W is kept constant at 10 μm [19] and generally OTAs use long channel length (L) in order to achieve high DC gain [20], so parametric sweep of L = 180 nm to 2.58 μm has been used.

A. Design Procedure of Input Pair ($M_{1,2}$)

The transconductance of the input pair ($g_{m1,2}$) is calculated from the UGB and C_L specifications as follows [1]

$$UGB = \frac{g_{m1,2}}{2\pi C_L} \tag{2}$$

The OTA's internal capacitance is neglected as the load capacitance is much larger than the lumped parasitic capacitance [21]. Substituting the required values from Table I in (2) yields $g_{m1,2} \approx 628.31$ μS. Since, the desired SR is 20 V/μs, the current consumption of the OTA will be

$$I_{d5} = SR \times C_L \tag{3}$$

where I_{d5} (= 100 μA) is the current flowing through M_5. I_{d5} divides equally between M_1 and M_2 i.e. $I_{d1} = I_{d2}$ = 50 μA. The g_m/I_d of the input pair is calculated as

$$\left(\frac{g_m}{I_d}\right)_{1,2} \approx 13\ S/A \tag{4}$$

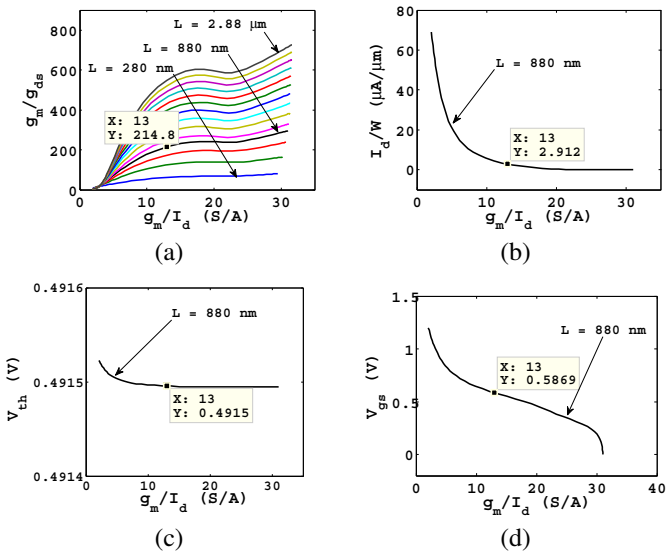

Fig. 3. Different parameters versus g_m/I_d of n-type input pair M_1, M_2 as a function of channel lengths (L = 280 nm: 200 nm: 2.88 μm) (a) intrinsic gain (g_m/g_{ds}), (b) normalized drain current (I_d/W), (c) V_{th}, (d) V_{gs}.

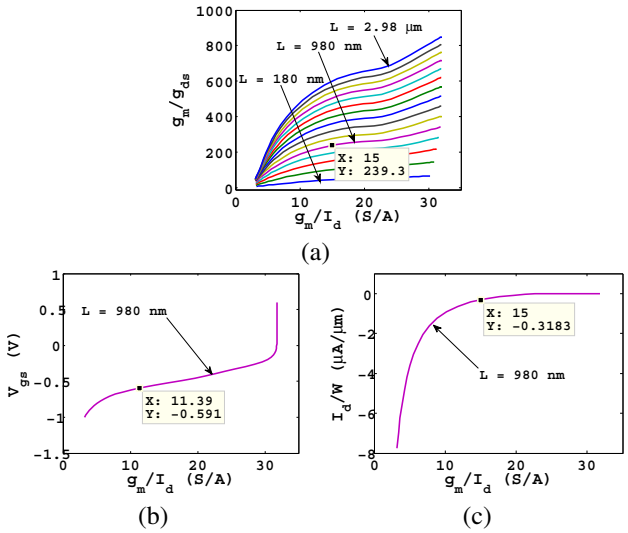

Fig. 4. Different parameters versus g_m/I_d of p-type current mirror load M_3, M_4 as a function of channel lengths (L = 180 nm: 200 nm: 2.98 μm) (a) intrinsic gain (g_m/g_{ds}), (b) V_{gs}, (c) normalized drain current (I_d/W).

The following relation gives the DC gain of the OTA [1]

$$A_{vdc} = \frac{g_{m1,2}}{g_{ds2} + g_{ds4}} \tag{5}$$

Substituting $g_{m1,2}$ and A_{vdc} in (5), the upper bound for the output conductance of M_2 and M_4 is obtained

$$g_{ds2} + g_{ds4} \leq 6.28\ \mu S \tag{6}$$

The inequality (6) splits equally between M_2 and M_4, which implies $g_{ds2} = g_{ds4} \leq 3.14\ \mu$S. The following equation gives the lower limit of intrinsic gain of input pair

$$\left(\frac{g_m}{g_{ds}}\right)_{1,2} \geq 200 \tag{7}$$

The graphical model in Fig. 3(a) shows the g_m/g_{ds} vs g_m/I_d plots for different channel lengths. At $(g_m/I_d)_{1,2}$ = 13 S/A, the plot for $L_{1,2}$ = 880 nm gives $(g_m/g_{ds})_{1,2} \approx 214.9$ which satisfies (7). For the selected $L_{1,2}$ (880 nm), the $W_{1,2}$ is calculated from the I_d/W vs g_m/I_d plot [Fig. 3(b)]. The current density $(I_d/W)_{1,2}$ = 2.91 μA/μm will give the required value of $W_{1,2}$ from the following relation

$$W_{1,2} = \frac{I_{d1,2}}{(I_d/W)_{1,2}} \approx 17.07\ \mu m \tag{8}$$

B. Design Procedure of Current Mirror Load ($M_{3,4}$)

The p-type MOSFETs, M_3 and M_4 are matched pair, so the output conductance of current mirror load are equal.

$$g_{ds3} = g_{ds4} \leq 3.14\ \mu S \tag{9}$$

In order to use the g_m/g_{ds} vs g_m/I_d graph, a large value of $(g_m/I_d)_{3,4}$ is required which is also essential from the power-efficient point of view [18], [20]. Selecting $(g_m/I_d)_{3,4}$ = 15 S/A results in $g_{m3,4}$ = 750 μ and thus the lower limit for intrinsic gain of current mirror load is obtained as

$$\left(\frac{g_m}{g_{ds}}\right)_{3,4} \geq 238.8 \tag{10}$$

From Fig. 4(a), the plot for $L_{3,4}$ = 980 nm satisfies the condition (10). The $(g_m/I_d)_{3,4}$ is also constrained by the maximum common-mode input ($V_{iCM,max}$) specification [1]. Applying KVL across the series of branch (M_3-M_1-M_5) of Fig. 2(a) will generate the constrained equation

$$V_{iCM,max} \leq V_{dd} + V_{gs3,4} + V_{th1,2} \tag{11}$$

$V_{th1,2}$ is extracted from the V_{th} vs g_m/I_d plot shown in Fig. 3(c), which is $\approx$ 0.4915 V. Substituting V_{dd}, $V_{th1,2}$, and $V_{iCM,max}$ in (11), the lower bound of $V_{gs3,4}$ is found as

$$V_{gs3,4} \geq -0.591\ V \tag{12}$$

By using V_{gs} vs g_m/I_d plot in Fig. 4(b), the valid range of $(g_m/I_d)_{3,4}$ due to the $V_{iCM,max}$ specification is found as

$$\left(\frac{g_m}{I_d}\right)_{3,4} \geq 11.39\ S/A \tag{13}$$

As a compromise, $(g_m/I_d)_{3,4}$ = 15 S/A is selected which satisfies (13) with adequate margin. $W_{3,4}$ is selected from the I_d/W vs g_m/I_d plot shown in Fig. 4(c), where $(I_d/W)_{3,4} \approx 0.3185$ μA/μm, thus $W_{3,4} \approx 156.96$ μm.

C. Design Procedure of Biased Current Sink ($M_{5,6}$)

The CMRR and minimum common-mode input ($V_{iCM,min}$) specifications decide the W/L of the biased current sink [1]. The CMRR is given by

$$CMRR(dB) = A_{vdc}(dB) - A_{vdc,CM}(dB) \tag{14}$$

where $A_{vdc,CM}$ is the common-mode DC gain. Substituting the required values in the following relation will give the limit of g_{ds5} [19].

$$A_{vdc,CM} = \frac{2g_{m1,2}g_{ds5}}{2g_{m1,2} + g_{ds5}} \cdot \frac{1}{2g_{m3,4}} \leq -50\ dB \tag{15}$$

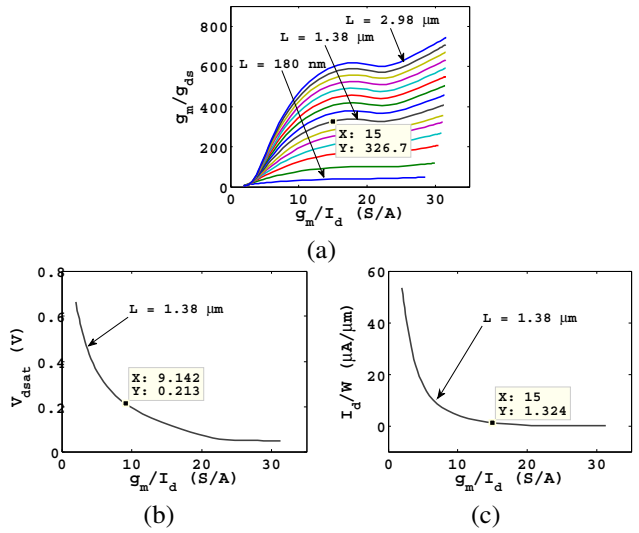

Fig. 5. Different parameters versus g_m/I_d of n-type biased current sink M_5 as a function of channel lengths ($L = 180$ nm: 200 nm: 2.98 μm) (a) intrinsic gain (g_m/g_{ds}), (b) V_{dsat}, (c) normalized drain current (I_d/W).

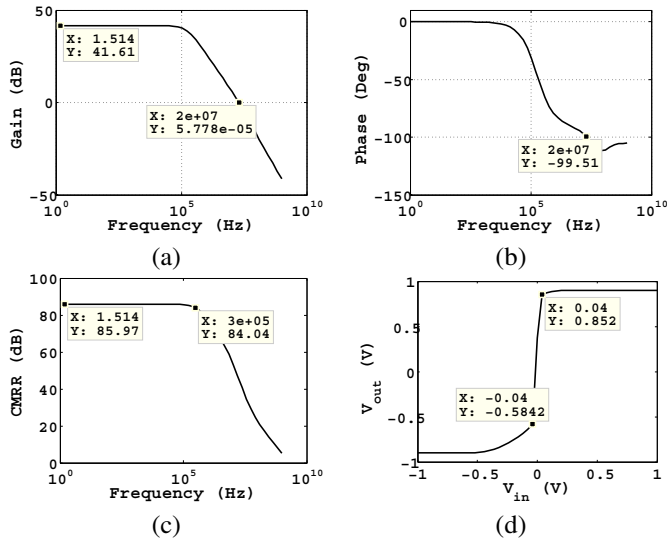

Fig. 6. Simulation results of the open-loop configuration of CMOS-OTA (a) DC gain, (b) phase, (c) CMRR, (d) output-voltage swing

$$\Rightarrow g_{ds5} \leq 4.76 \tag{16}$$

Similar to Section II-B, a large value for $(g_m/I_d)_5 = 15$ S/A is assumed which results in $g_{m5} = 1500$ μS and $g_m/g_{ds} \geq 315$. From Fig. 5(a), choosing $L_5 = 1.38$ μm satisfies this requirement. The $V_{iCM,min}$ that can be applied before driving the M_5 into saturation region is constrained by

$$V_{iCM,min} \geq V_{gs1,2} + V_{dsat5} + V_{ss} \tag{17}$$

Substituting the required values in (17), the constraint on V_{dsat5} is obtained as

$$V_{dsat5} \leq 0.213\ V \tag{18}$$

By using V_{dsat} vs g_m/I_d plot in Fig. 5(b), the valid range of $(g_m/I_d)_5$ due to the $V_{iCM,min}$ specification is obtained as

$$\left(\frac{g_m}{I_d}\right)_5 \geq 9.14\ S/A \tag{19}$$

As a compromise, $g_m/I_d = 15$ S/A is selected which satisfies (19) with a desired limit. The W_5 is selected from I_d/W vs g_m/I_d plot in Fig. 5(c), where $(I_d/W)_5 \approx 1.321$ μA/μm, thus, $W_5 \approx 75.66$ μm and $W_6 \approx 75.66/5 = 15.13$ μm.

TABLE II
SUMMARY OF TRANSISTOR'S SIZING AND CURRENT FLOWING THROUGH EACH OF THEM

Transistors	L (μm)	W (μm)	CMOS-OTA (μA)	UTBSOI-OTA (μA)
M_1, M_2	0.880	17.07	49.19, 49.20	47.77
M_3, M_4	0.980	156.96	49.19, 49.20	47.77
M_5, M_6	1.38	75.66, 15.13	98.40, 20.0	95.66, 19.88

III. Results and Discussions

Table II summarizes size of the MOSFETs and current flowing through each of them. The CMOS and UTBSOI-OTAs have been simulated under a supply voltage of 1.8 V ($V_{dd} = 0.9$ V, $V_{ss} = -0.9$ V) and characteristics of the open-loop and unity-gain configurations [1] are examined.

A. Simulation Results

Fig. 6 shows the simulated results obtained from the open-loop configuration of CMOS-OTA. Through the AC analysis simulation, the DC gain and UGB are $\approx$ 41.61 dB and 20.42 MHz, respectively as per the specified requirements. The other extracted parameters from AC analysis are PM and CMRR, simulated as 80.49° and 85.97 dB, respectively. The output-swing and power consumption have been extracted from DC analysis. The valid range of output-swing is ≈ -0.58 to 0.85 V as shown in Fig 6(d). In UTBSOI-OTA, the back gates of p- and n-type devices are connected to V_{dd} and V_{ss} respectively [Fig. 2(b)] so as to obtain static threshold voltage. The DC gain, UGB, PM, and CMRR of UTBSOI-OTA are simulated as 55.45 dB, 18.61 MHz, 74.6°, and 85.2 dB, respectively [Fig. 7]. The DC gain has seen to be improved in case of UTBSOI-OTA, whereas the UGB, PM, and CMRR are degraded within a tolerable limit. The valid output-swing is obtained as -0.73 to 0.86 V as shown in Fig. 7(d). The power consumption in case of CMOS-OTA is obtained as 0.213 mW and that of UTBSOI-OTA it is obtained as 0.207 mW.

The SR and V_{iCMR} have been extracted from the unity-gain (buffer) configuration. The valid buffer input range for the OTAs is obtained from the V_{out} vs V_{in} plots shown in Fig. 8(a) and (b). The SR of both the OTAs have been calculated from the unity-gain transient response as shown in Fig. 8(c) and (d). The SR is calculated using the relation: $(SR_+ + SR_-)/2$ which are obtained as 16.13 V/μs for CMOS and 15.74 V/μs for UTBSOI-OTAs. A summary of the

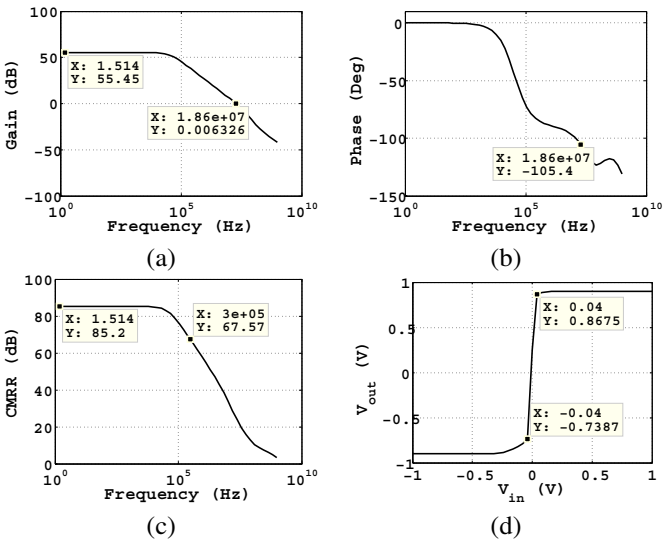

Fig. 7. Simulation results of the open-loop configuration of UTBSOI-OTA (a) DC gain, (b) phase, (c) CMRR, (d) output-voltage swing

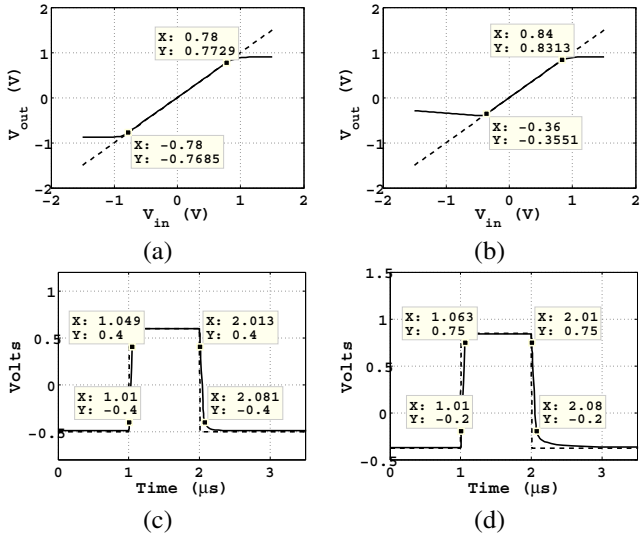

Fig. 8. Buffer input range of (a) CMOS-OTA, (b) UTBSOI-OTA and unity-gain transient response of (c) CMOS-OTA, (d) UTBSOI-OTA. (The V_{in} and V_{out} waveforms are represented by dashed and solid lines respectively).

simulation results of the OTAs is listed in Table III. Various performance parameters like DC gain, UGB, SR, PM, and power consumption are compared with prior reported works.

B. Layout Extraction of the CMOS-OTA

The layout design of the CMOS-OTA is shown in Fig. 9. In order to observe the impact of the extracted layout parasitics (resistance and capacitance) on the CMOS-OTA, the open-loop and unity-gain configurations of the OTA are simulated accordingly. Some deviations have been observed between the pre-layout [Table III], and post-layout simulation results, and the errors have been analyzed. The reason for the errors is related to inaccuracies associated with the parasitic components of the layout. Regarding the post layout simulation of the CMOS-OTA, the performance parameters like UGB, PM, DC gain, SR, CMRR, and power are degraded by 2.59%, 0.70%, 0.29%, 2.23%, 3.67%, and 2.34%, respectively as given in Table IV. The area of the CMOS-OTA extracted from the layout design is 2.78×10^{-3} mm^2.

TABLE III
PERFORMANCE COMPARISON WITH PRIOR REPORTED WORKS

Specifications	[6]	[7]	[19]	CMOS-OTA	UTBSOI-OTA
Technology (nm)	180	180	180	180	180
Supply voltage (V)	1.8	0.36	1.8	1.8	1.8
Load capacitor (pF)	200	-	5	5	5
UGB (MHz)	86.5	0.98	5	20.42	18.61
PM (°)	50	-	90	80.49	74.6
DC gain (dB)	72	18.4	33.5	41.61	55.45
Slew-rate (V/μs)	74.1	-	-	16.13	15.74
$V_{iCM,min}$ (V)	-	-	0.14	-0.179	-0.0015
$V_{iCM,max}$ (V)	-	-	1.12	0.778	0.997
CMRR (dB) @ DC	-	-	73.6	85.97	85.2
@ 300 KHz	-	45.3	-	84.04	67.57
Power (mW)	11.9	0.0154	-	0.213	0.207

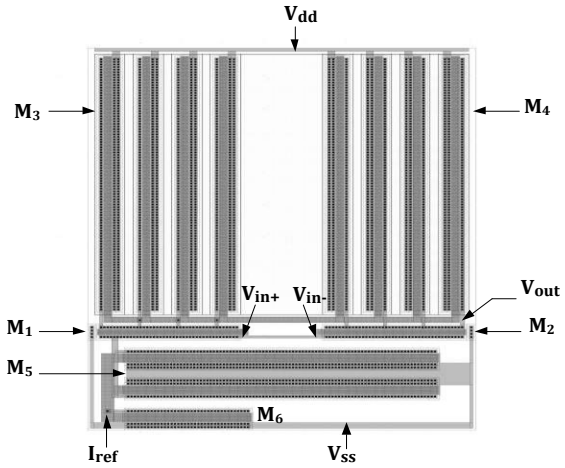

Fig. 9. Extracted layout view of the CMOS-OTA.

TABLE IV
SUMMARY OF POST-LAYOUT SIMULATED RESULTS OF CMOS-OTA

Specifications	Pre-layout results [Table III]	Post-layout results	Error (%)
UGB (MHz)	20.42	19.89	-2.59
PM (°)	80.49	79.92	-0.70
DC gain (dB)	41.61	41.49	-0.29
Slew-rate (V/μs)	16.13	15.77	-2.23
CMRR (dB) @ DC	85.97	82.81	-3.67
Power (mW)	0.213	0.218	2.34
Area (mm^2)	-	2.78×10^{-3}	-

The minus sign ($-$) shows the decrease in performance parameter values in post-layout simulation.

C. Applications of the UTBSOI-OTA

The UTBSOI-OTA has been tested by using it in the integrator circuits. Fig. 10(a) shows a basic integrator circuit (integrator 1) which is obtained from an inverting amplifier configuration by replacing the feedback resistor R_F with a capacitor C_F [23]. The unity-gain frequency of integrator 1 is $f_u = 1/(2\pi R_1 C_F)$, where, $R_1 = 15.9$ kΩ, $C_F = 0.01$ μF are chosen so as to generate $f_u = 1$ KHz. The circuit is tested

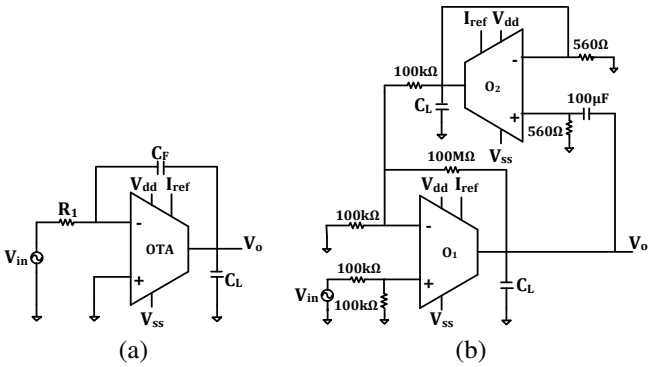

Fig. 10. The circuit diagram of (a) integrator 1, (b) integrator 2

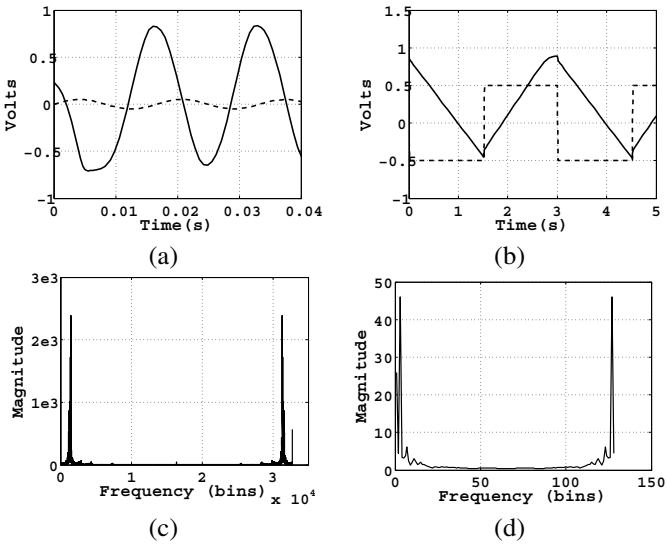

Fig. 11. Simulation results of UTBSOI-OTA based (a) integrator 1, (b) integrator 2. (c) 32K-point FFT for the output of integrator 1, (d) 128-point FFT for the output of integrator 2. (The V_{in} and V_{out} waveforms are represented by dashed and solid lines respectively).

by applying a sinusoidal input voltage of amplitude 24 mV at 60 Hz. Fig. 11(a) shows the output waveform obtained from the integrator 1. The validity of the OTA has been further verified by using it in a low-frequency integrator (integrator 2) [24] as shown in Fig. 10(b). A square wave voltage of amplitude $\pm$ 0.5 V at 330 mHz is applied which generates triangular wave output as shown in Fig. 11(b). Fig. 11(c) and (d) show the FFT obtained in MATLAB from the transient outputs of integrator 1 and integrator 2 respectively. From the FFT, the signal-to-noise ratio (SNR) and total-harmonic-distortion (THD) are calculated to acquire the signal-to-noise-and-distortion ratio (SNDR) as given in Table V. The relation used to calculate of the SNDR is [25]

$$SNDR = -10\ log\left[10^{-SNR/10} + 10^{-THD/10}\right] \qquad (20)$$

A good integration action is clearly seen from the above results which imply that the UTBSOI-OTA can be successfully used to design any analog circuits.

Addition to this, application of the UTBSOI-OTA has also been extended to active filters [26] in which the OTA is used for amplification and gain control. Fig. 12(a) shows

TABLE V
CALCULATED SNR, THD, AND SNDR OF THE INTEGRATOR CIRCUITS [FIG. 10]

Integrator circuits	SNR (dB)	THD (dB)	SNDR (dB)
Integrator 1	7.23	8.33	10.9
Integrator 2	10.34	−4.20	−10.02

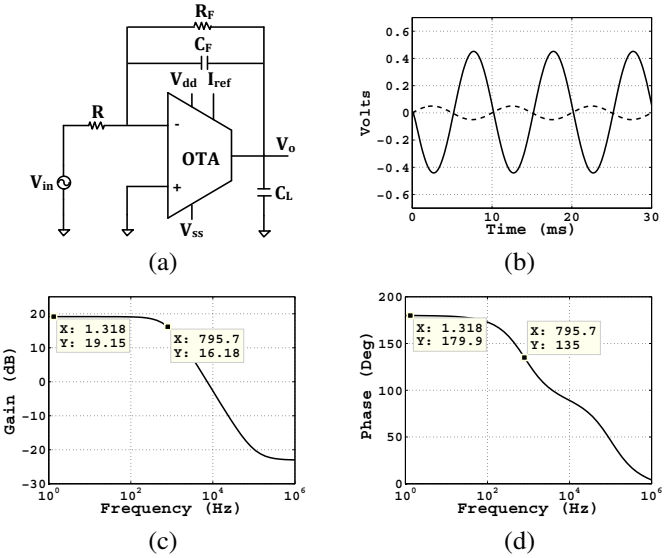

Fig. 12. Application of UTBSOI-OTA in (a) active low-pass filter, (b) transient response with sinusoidal input voltage of amplitude 50 mV at $f = 100$ Hz, (c) gain, (d) phase. (The V_{in} and V_{out} waveforms are represented by dashed and solid lines respectively).

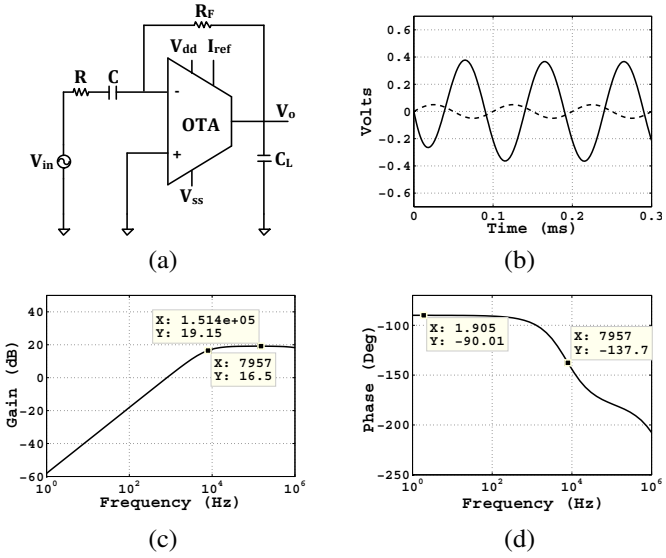

Fig. 13. Application of UTBSOI-OTA in (a) active high pass filter, (b) transient response with sinusoidal input voltage of amplitude 50 mV at $f = 10$ KHz, (c) gain, (d) phase. (The V_{in} and V_{out} waveforms are represented by dashed and solid lines respectively).

the first order low-pass filter having cut-off frequency ($f_c = 1/2\pi R_F C_F$) of 795.77 Hz with component values $R = 20$ kΩ, $C_F = 1$ nF, and $R_F = 200$ kΩ. The gain vs frequency plot in Fig. 12(c) clearly indicates the property of a low-pass filter with gain $\approx$ 19.15 dB which gets reduced by 3 dB

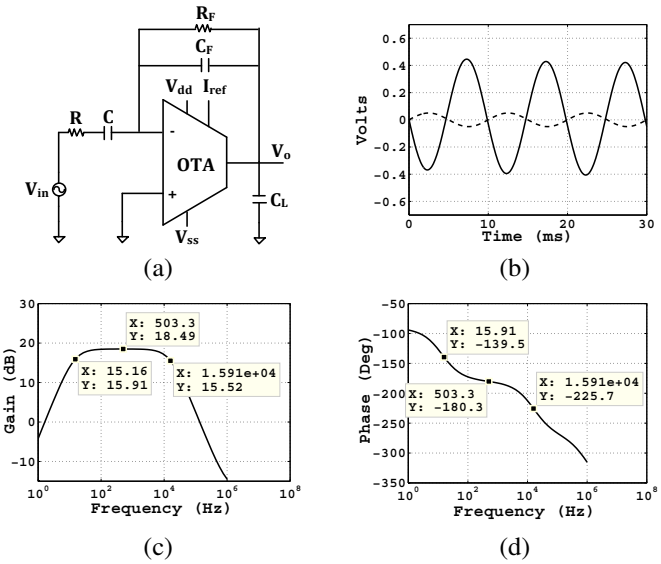

Fig. 14. Application of UTBSOI-OTA in (a) active band pass filter, (b) transient response with sinusoidal input voltage of amplitude 50 mV at $f = 100$ Hz, (c) gain, (d) phase. (The V_{in} and V_{out} waveforms are represented by dashed and solid lines respectively).

(=16.18 dB) at 795.77 Hz. Fig. 13(a) show the UTBSOI-OTA based first order high-pass filter in which component values $R = 20$ kΩ, $C = 1$ nF, and $R_F = 200$ kΩ are chosen to generate $f_c = 1/2\pi RC \equiv 7957.77$ Hz. Similarly, the second order band-pass filter in Fig. 14(a) is using the UTBSOI-OTA with component values $R = 10$ kΩ, $C = 1$ μF, $C_F = 100$ pF and $R_F = 100$ kΩ having the low ($f_L = 1/2\pi RC$) and high ($f_H = 1/2\pi R_F C_F$) cut-off frequencies of 15.91 Hz and 15.91 KHz. Simulation results of the active filters [Fig. 12−14] proves the applicability of UTBSOI-OTA in audio frequency applications.

IV. Conclusion

In this paper, single-stage OTA has been designed where the W/L of constituting MOSFETs have been evaluated mathematically and graphically through g_m/I_d methodology. Keeping the transistor's aspect ratio constant, the OTA has been designed through UTBSOI transistor. Simulation is performed in Cadence-spectre where BSIM3v3 and BSIM-IMG models have been utilized for MOSFET and UTBSOI respectively. Open-loop and unity-gain configurations are simulated accordingly to show a comparative analysis between the CMOS and UTBSOI based OTAs. In brief, the performance achieved by UTBSOI-OTA meets all the desired specifications within a desired limit. From the simulated results, it is observed that in sub-micron regime (180-nm), UTBSOI transistor can be successfully used to design the analog circuits. Advantage of the UTBSOI has been further clarified from the improvements of UTBSOI-OTA over the CMOS-OTA in terms of DC gain and power consumption by $\approx 33.26\%$ and 2.81%, respectively, through circuit simulation at the schematic level. Moreover, the UTBSOI-OTA has been verified by using it in integrator and active filter circuits which are able to show the desired output successfully. Based on the performance improvements obtained by applying the g_m/I_d methodology to UTBSOI at the schematic level simulation, it can be concluded that investing considerable effort into creating a process-design kit for the UTBSOI technology would be a very welcome step in enabling further improvements in analog and mixed-signal circuits results.

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References

[1] P.E. Allen and D.R. Holberg, *CMOS Analog Circuit Design*, 3rd ed. London, UK.: Oxford Univ. Press, 2014.

[2] W. Liu and C. Hu, "BSIM3v3 MOSFET model," *Int. J. of High Speed Electron. Syst.*, vol. 9, no. 3, pp. 671−701, Sep. 1998.

[3] J.R-. Angulo, B. Calvo, R.G. Carvajal, and A.L-. Martin, "Low-voltage gm-enhanced CMOS differential pairs using positive feedback," in *Proc. IEEE Int. Symp. Circuits Syst.*, Paris, 2010, pp. 773−776.

[4] M.R.V. Bernal, S. Celma, N. Medrano, and B. Calvo, "An ultralow-power low-voltage class-AB fully differential OpAmp for long-life autonomous portable equipment," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 59, no. 10, pp. 643˘647, Oct. 2012.

[5] M. Akbari, "Single-stage fully recycling folded cascode OTA for switched-capacitor circuits," *Electron. Lett.*, vol. 51, no. 13, pp. 977−979, Jun. 2015.

[6] S. Sutula, M. Dei, L. Terés, and F.S-.Graells, "Variable-mirror amplifier: a new family of process-independent class-AB single-stage OTAs for low-power SC circuits," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 63, no. 8, pp. 1101−1110, Aug. 2016.

[7] L. Severo and V. Noije, "0.36 V PGA combining single-stage OTA and input negative transconductor for low energy RF receivers," *Electron. Lett.*, vol. 54, no. 5, pp. 977−979, Mar. 2018.

[8] A.J.L-.Martin *et al*., "Enhanced single-stage folded cascode OTA suitable for large capacitive loads," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 65, no. 4, pp. 441−445, Apr. 2018.

[9] R. Póvoa *et al*., "Single-stage OTA biased by voltage combiners with enhanced performance using current starving," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 65, no. 11, pp. 1599−1603, Nov. 2018.

[10] Q. Zhang, Y. Wang, X. Zhao, and L. Dong, "Single-stage multipath class-AB bulk driven OTA with enhanced power efficiency," *AEU-Int. J. Electron. Commun.*, vol. 107, pp. 39−48, Jul. 2019.

[11] F. Silveira, D. Flandre and P.G.A. Jespers, "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE J. Solid-State Circuits*, vol. 31, no. 9, pp. 1314−1319, Sep. 1996.

[12] I. Ferain, C.A. Colinge, and J.-P. Colinge, "Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors," *Nature*, vol. 479, pp. 310−316, Nov. 2011.

[13] N. Paydavosi *et al*., "BSIM-SPICE models enable FinFET and UTB IC designs," *IEEE Access*, vol. 1, pp. 201−215, May 2013.

[14] Q. Liu *et al.*, "Ultra-thin-body and BOX (UTBB) fully depleted (FD) device integration for 22 nm," in *Proc. Symp. VLSI Technol.*, Honolulu, 2010, pp. 61−62.

[15] S. Khanderwal *et al*., "BSIM-IMG: A compact model for ultrathin-body SOI MOSFETs with back-gate control," *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2019−2026, Aug. 2012.

[16] BSIM-IMG Model. (2017, Aug. 10). [Online]. Available: http://bsim.berkeley.edu/models/bsimimg/

[17] C. Hu *et al*., *Industry Standard FDSOI Compact Model BSIM-IMG for IC Design*, 1st ed. Woodhead Pub., 2019.

[18] T. Konishi, K. Inaju, J.G. Lee, M. Natsui, S. Masui, and B. Murmann, "Design optimization of high-speed and low-power operational transconductance amplifier using gm/ID lookup table methodology," *IEICE Trans. Electron.*, vol. E94-C, no. 3, pp. 334−345, Mar. 2011.

[19] M.N. Sabri, H. Omran, and M. Dessouky, "Systematic design and optimization of operational transconductance amplifier using gm/ID design methodology," *Microelctronics J.*, vol. 75, pp. 87−96, May 2018.

[20] V. Subramanian *et al*., "Impact of fin width on digital and analog performances of n-FinFETs," *Solid-State Electron*, vol. 51, no. 4, pp. 551−559, Apr. 2007.

[21] K.N. Leung and P.K.T. Mok, "Analysis of multistage amplifier-frequency compensation," *IEEE Trans. Circuits Syst. I: Fundam. Theory Appl.*, vol. 48, no. 9, pp. 1041−1056, Sep. 2001.

[22] M. Yang and G.W. Roberts, "Synthesis of high gain operational transconductance amplifiers for closed-loop operation using a generalized controller-based compensation method," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 63, no. 11, pp. 1794−1806, Nov. 2016.

[23] R.A. Gayakwad, *Op-amps and Linear Integrated Circuits*, 4th ed. New Delhi, India: PHI., 2010.

[24] M.A. Al-Alaoui, "Low-frequency differentiators and integrators for biomedical and seismic signals," *IEEE Trans. Circuits Syst. I: Fundam. Theory Appl.*, vol. 48, no. 8, pp. 1006−1011, Aug. 2001.

[25] W. Kester, "Understand SINAD, ENOB, SNR, THD, THD + N, and SFDR so you don't get lost in the noise floor," Analog Devices, Norwood, MA, USA, Tech. Rep. MT-003, 2009.

[26] S. Franco, *Design with Operational Amplifiers and Analog Integrated Circuits*, 3rd ed. New York: McGraw-Hill, 2013.

Dual Output Sinusoidal Oscillator Using Second Generation Current Controlled Conveyor

Syed Zahiruddin, Avireni Srinivasulu and Musala Sarada

***Abstract*—Second Generation Current Controlled Conveyor (CCCII) based tunable Dual Output Sinusoidal Oscillator (MSO) is proposed. It consists of three CCCIIs, a resistor and two grounded capacitors. By tuning external DC bias current, the oscillator frequency and commencement of its oscillations are controlled electronically. The proposed circuit is verified using PSPICE simulator and also on laboratory breadboard using commercially available integrated circuits Current Feedback Operational Amplifier (AD844AN) and Operational Transconductance Amplifier (LM13600) at a supply rail voltage of ±6 V. Further its nonlinearities, sensitivities, performance characteristics are also verified. Comparison of the proposed topology with the ongoing methods are also undertaken. PSPICE simulation results are verified with a low supply voltage of ±1 V, temperature analysis, analysis by using Montecarlo method and finally Total Harmonic Distortion (THD) is also demonstrated.**

***Keywords*—Dual Output Sinusoidal Oscillator (MSO), Current Feedback Operational Amplifier (CFOA), Operational Transconductance Amplifier (OTA) and Current mode oscillators.**

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I. Introduction

DUAL Output Sinusoidal Oscillators play an important role in many applications especially in the areas like communication systems, power electronics and measurement, instrumentation and Bio-medical fields etc. Specific applications of MSO include decoupled dynamic control of six phase two-motor drive system, vector control of single-phase to three-phase pulse width modulation converter and control schemes for five-phase induction motor drives. In literature several methods are innovated and explained to design MSO but they are prone to encounter with the problem of utilizing more number of active and passive devices for their realization. The likely features of interest are that floating resistors seldom control the frequency, further floating capacitors however restrict the high frequency operation, and also in this case, electronic tunability may not be possible [1-3]. M.S. Ansari *et al* [4] had proposed mixed mode of three phase sinusoidal oscillator realized with Dual-X Current Conveyor (DXCCII) as an active element. Its design depends on the first order inverter low pass filter, which contains DXCCII, resistors and capacitors. It involves twelve passive components and is really a complex structure for monolithic IC fabrication besides offering the benefit of grounded passive components. S. Maheshwari and R. Verma [5], have developed several oscillator circuits and drew comparison between third order and second order sinusoidal oscillator circuits. It is observed that the third order oscillator, however, has low harmonic distortion over second order. The design is involved with four CCCIIs to develop three low pass filters and one gain block in feedback. It has the drawback of requiring four CCCIIs and four passive components. In order to obviate the above restrictions, translinear based Dual Output Sinusoidal Oscillator has been proposed.

Proposed design is entailed with the following features:

1. Single grounded external resistor is required for realization of the design.
2. Utilizes grounded capacitors that are worthwhile for IC fabrication, also the chip area is reduced effectively in comparison with floating capacitor configuration and also preferred in high frequency applications.
3. Oscillator frequency and commencement of oscillations are independent of each other and thus enhances the electronic tunability.
4. Possess low passive sensitivities [6].

The design consists of three CCCIIs, a resistor and two grounded capacitors only. By varying the external DC bias current, the oscillator frequency and the oscillatory condition of the proposed circuit are tuned separately.

II. Current Conveyor

A. Current Mode Circuits

For the past few decades, analog designers have been trusted current-mode circuits as necessary building blocks for analog circuits design. Smith and Sedra [1] had invented the first generation current conveyor (CCI), employing bipolar junction

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transistors. It has the drawback of low input impedance, which is not feasible to apply in many applications. The modified CCI, called as Second Generation Current Conveyor (CCII) was introduced by the same duo in 1970. It has high input impedance and is preferred in many applications. CCCII, a series of CCII, has the parasitic resistance at input port *X* which is current controlled. Thus, it has introduced the concept of Current Controlled Conveyor (CCCII) [7-10].

B. Second Generation Current Controlled Conveyor

Basically, CCII is the current mode active structural element. It is a mixed translinear loop that has considerable amount of intrinsic resistance R_B at the input node *X*. It is varied by tuning the external bias current.

The state space representation, by considering the intrinsic resistance R_B of an ideal CCCII is given below in (1).

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_B & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

From (1), if the direction of current at input port X and output port Z are the same, it becomes a positive current conveyor (CCCII+). If the direction of current is opposite to each other then it is a negative current conveyor (CCCII-). At node *X*, R_B denotes the input intrinsic resistance, tuned with bias current, ($R_B=V_T/2I_B$), where $V_T \approx 26$ mV is the voltage equivalent of room temperature, and $I_B \geq 0$ is the external bias current of the CCCII [5]. At node *Y,* the current I_Y is zero since the impedance at the input of node *Y* is infinite. So, the current applied at input node *X* is transformed to high impedance output node *Z*. Several applications have been presented by applying bias current to the CCCII [9-13]. Fig. 1 shows the symbol of CCCII.

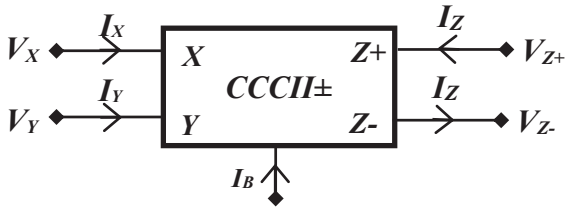

Fig. 1. Symbol of CCCII±

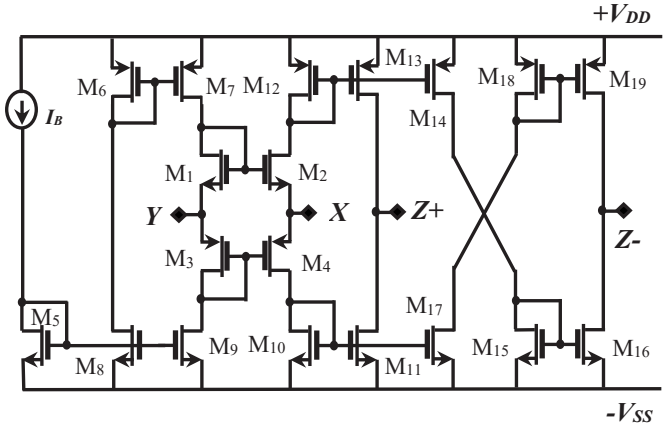

Fig. 2. Internal structure of CCCII±

CCCII is a three terminal device, two input terminals *X* and *Y* along with an output terminal *Z,* as shown in Fig. 2 [11]. The device is characterized by $I_Y = 0$, $V_X = V_Y + R_B I_X$ and $I_Z = \pm I_X$, shown in the matrix form in (1). The device has an infinite input impedance at terminal *Y* and *Z,* whereas, the input terminal *X* has intrinsic resistance R_B which is tuned by the external bias current I_B, given as

$$R_B = \frac{1}{g_{m2} + g_{m4}} \quad (2)$$

where g_{mi} is the transconductance of the MOS transistor, assuming that both the transistors are matched, $g_{m2}=g_{m4}$, then

$$R_B = \frac{1}{\sqrt{8\mu C_{OX}\left(\frac{W}{L}\right) I_B}} \quad (3)$$

where μ is the mobility of the carrier, C_{OX} is the oxide capacitance, *W* is the channel width and *L* is the channel length of the MOS transistors (M_2 and M_4). The schematic of CCCII is realized with MOS transistors [11], as shown in Fig. 2. The circuit has translinear loop involving the transistors M_1 to M_4, DC biased by using the current mirrors M_6-M_7 and M_8-M_9. The input current I_X is duplicated to produce I_{Z+} and I_{Z-} using translinear loops. The current is replicated using additional current mirrors M_{10}-M_{13}, M_{14}-M_{16} and M_{17}-M_{19}. The transistor aspect ratios of Fig. 2 are shown in Table. I. For $I_Z = +I_X$, the device is termed as positive current conveyor and for $I_Z = -I_X$ it is called negative current conveyor [1]. In bipolar CCCII, the intrinsic resistance R_B is inversely proportional to the bias current I_B whereas, R_B is inversely proportional to the square root of I_B for CMOS based CCCIIs.

TABLE I
ASPECT RATIOS OF FIG. 2 TRANSISTORS

Transistor	Width (μm)	Length (μm)
M_1, M_2	2	0.5
M_3, M_4	4	0.5
M_5, M_8, M_9, M_{10}, M_{11}, M_{15}, M_{16}, M_{17}	5	0.5
M_6, M_7, M_{13}, M_{14}, M_{18}, M_{19}	15	0.5
M_{12}	14.2	0.5

C. Electronically Tunable MSO using CCCII

Figure. 3 shows the proposed electronically tunable MSO involving CCCII as an active device. Using routine analysis and current-voltage characteristics of the CCCII in (1), the characteristic equation of the proposed design is given as:

$$S^2 C_1 C_2 R_{B1} R_{eq} R_{B3} + s\left(C_1 R_{B1} R_{B3} - C_2 R_{eq} R_{B3}\right) + 2R_{B3} = 0 \quad (4)$$

where $R_{eq} = R + R_{B2}$

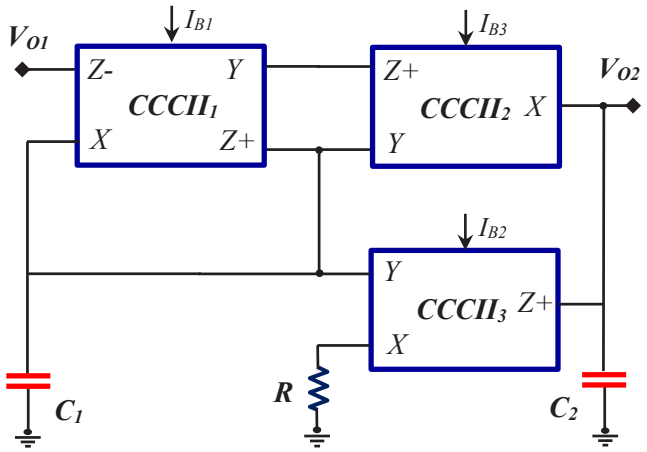

Fig. 3. Proposed electronically tunable MSO using CCCIIs

The oscillation condition and the oscillation frequency expression are realized by equating real and imaginary components of (4) to zeros and are given by

$$C_1 R_{B1} = C_2 R_{eq} \tag{5}$$

and

$$\omega = \sqrt{\frac{2}{C_1 C_2 R_{B1} R_{eq}}} \tag{6}$$

where R_B (R_B=R_{B1}=R_{B2}=R_{B3}) refers to the parasitic resistance at the input terminals X of $CCCII_1$, $CCCII_2$ and $CCCII_3$ due to its bias current.

Circuit as mentioned in Fig. 3 can also be inhibited to oscillate using this condition:

$$I_{B1} = I_{B2} = I_{B3} \tag{7}$$

The oscillator frequency and commencement of oscillation are controlled using bias currents.

The multiphase outputs V_2 and V_1 of Fig. 3, can be related as

$$\frac{V_2}{V_1} = \frac{1}{sC_1 R_{B2}} \tag{8}$$

where the phase shift is -90°.

III. Non Ideal Analysis

In practice, due to presence of non-ideal current and voltage transfer, CCCII ideal characteristics are affected that causes error to occur. Taking the non-idealities into consideration, the nodal voltages and branch currents are related as

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \alpha & R_B & 0 \\ 0 & \beta & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{9}$$

where $\alpha = 1-\varepsilon$, $|\varepsilon| << 1$ defines the tracking error of voltage and $\beta = 1-\delta$, $|\delta| << 1$ is the tracking error of current.

The characteristic equation of Fig. 3, using (9), is written as shown under

$$s^2 C_1 C_2 R_{B1} R_{eq} R_{B3} + s\left(C_1 R_{B1} R_{B3} - \alpha_2 \beta_2 C_2 R_{eq} R_{B3}\right) + 2\alpha_1 \beta_1 \beta_2 R_{B3} = 0 \tag{10}$$

Therefore, the condition for commencement of oscillation and oscillation frequency are modified respectively, as

$$C_1 R_{B1} = \alpha_2 \beta_2 R_{eq} C_2 \tag{11}$$

and

$$\omega = \sqrt{\frac{2\alpha_1 \beta_1 \beta_2}{C_1 C_2 R_{B1} R_{eq}}} \tag{12}$$

Referring to (11) and (12), the tracking errors thus slightly effect the oscillator frequency and condition of oscillation respectively. But, this effect can be minimized by improving the current gain.

According to (6) the sensitivities of passive and active components using partial derivative method with respect to the frequency are given as:

$$S^{\omega}_{C_1 C_2} = -1/2 \tag{13}$$

$$S^{\omega}_{R_B} = -1/2 \tag{14}$$

$$S^{\omega}_{IB_1, IB_2} = 1/2 \tag{15}$$

$$S^{\omega}_{V_T} = -1 \tag{16}$$

It is apparent that all parametric sensitivities of ω are low, only 0.5 in magnitude. Thus, the design exhibits good and appealing low sensitivity value [19-21].

IV. Simulation Results

The proposed MSO of Fig. 3 has been simulated using PSPICE simulator. The internal schematic of CCCII was realized as shown in Fig. 2. The voltages $\pm V_{CC}$ = 1V and the value of dc for all the CCCIIs are same, I_B = 100 µA (R_B = 260 Ω) along with C_1=8 nF, C_2=0.21 nF and R=10 kΩ are applied. The distinctive output simulation results of Fig. 3 is illustrated in Fig. 4, the theoretical time period is 6.608 µs, and the simulated time period is 5.9999 µs. The maximum oscillation frequency of 500 kHz is obtained by tuning the bias current and passive component values that are kept constant. In addition, Fig. 5 represents the simulated frequency spectrums of the output.

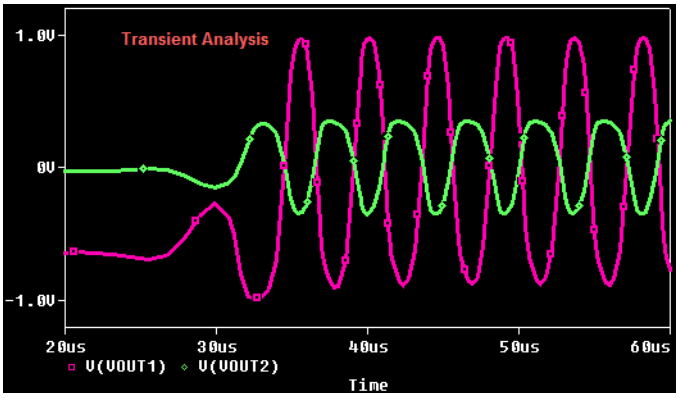

Fig. 4. The simulated output waveform of Fig.3, selected: I_B=100µA and C_1=8 nF C_2=0.21nF and R=10kΩ.

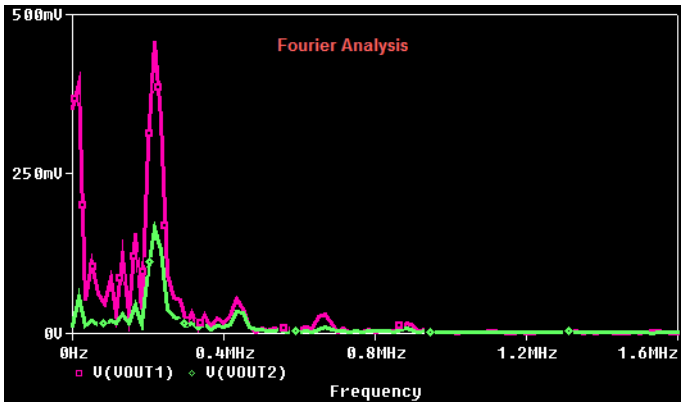

Fig. 5. Simulated output spectrums of Fig. 3, selected I_B=100 µA and C_1=8 nF, C_2=0.21 nF and R=10 kΩ.

Figure 6 shows the graphic representation of variations in amplitudes of output voltages over the variation of temperature from 0° C to 100° C, keeping the bias currents and passive component values constant.

Figure 7 illustrate the simulation results of the proposed topology of Fig. 3, by varying the values of bias currents I_B (i.e., I_B=I_{B1}=I_{B2}=I_{B3}) verses frequency. The bias current is varied from 5 µA to 250 µA by maintaining C_1=8 nF, C_2=0.21 nF and R=10 kΩ are constant. The plot specifies the linear variation of frequency with bias current, the non-idealities may be due to the ignored tracking errors.

The simulation conditions and the performance characteristics of CCCII configuration are summarized in Table II. The circuit is structured with low supply voltage of ±1 V and has low power dissipation of the order of 1.7 mW. The total harmonic distortion is good and it is 1.97%. The input and output resistances are also measured which has exerted some influence on the performance of the circuit.

Figure 8 is the graphic representation of the Montecarlo analysis for the proposed configuration as shown in Fig. 3. The graph is produced for the 50 iterations for both the output signals. The histogram for the output signal 1 and 2 are represented in Figures 9 and 10 respectively. The mean and standard deviation values are 0.977, 0.351 and 0.0097, 0.00037 for the two signals, which are quite low and acceptable.

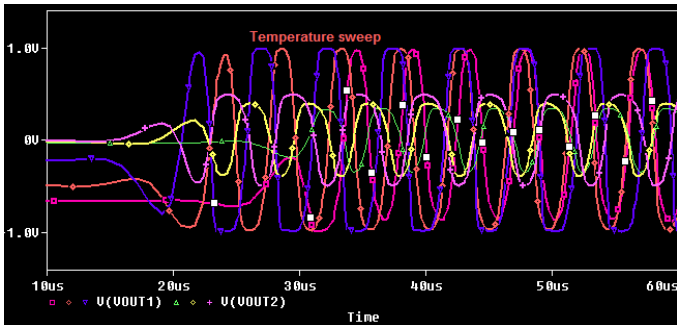

Fig. 6. Simulated results of the proposed MSO for variation in temperatures from 0° C to 100° C.

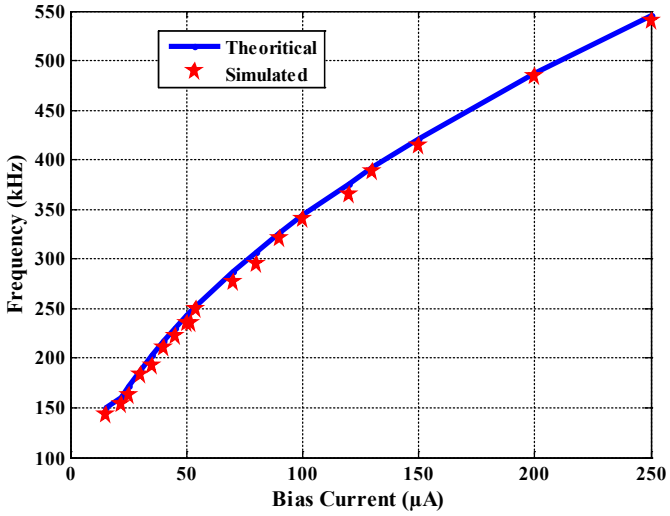

Fig.7. Simulated results of the oscillation frequency Vs bias current of Fig. 3.

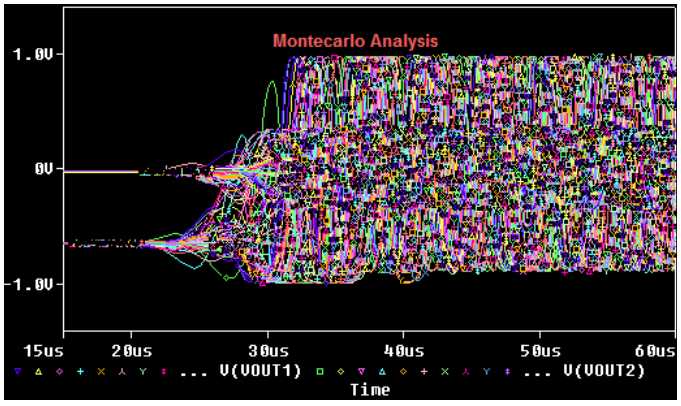

Fig. 8. Montecarlo analysis of proposed MSO

Figure 11 is the worst case analysis where as Figure 12 and 13 are the worst case sensitivities for the designed configurations. The worst case and sensitivity analysis is to identify the uncertainty in the output of a mathematical model or system. The graphs specify the insensitivity of the output and reflects the analysis as derived previously. The phase margin between the two output signals is 180 degrees and is graphically shown in Figure 14. The simulation conditions and the performance characteristics of CCCII configuration are summarized in Table

II. The input and output resistances are also measured which have exerted some influence on the performance of the circuit.

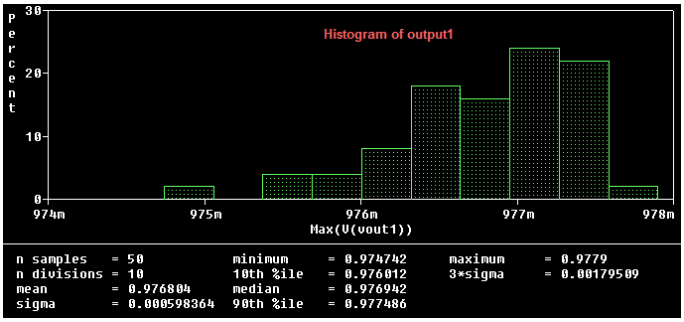

Fig. 9. Histogram for the output signal V_{O1} of the proposed MSO

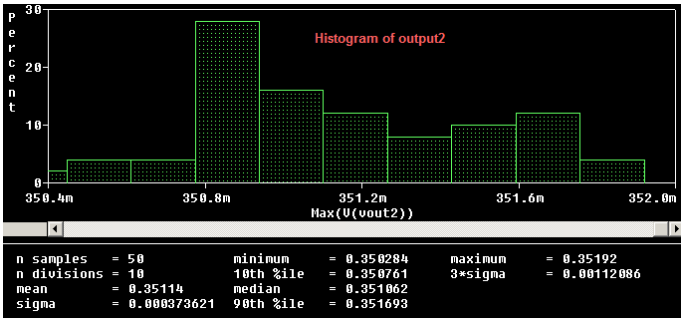

Fig. 10. Histogram for the output signal V_{O2} of the proposed MSO

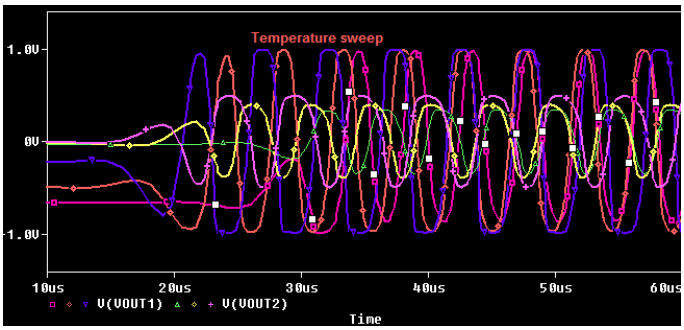

Fig. 11. Worst case analysis for the proposed MSO

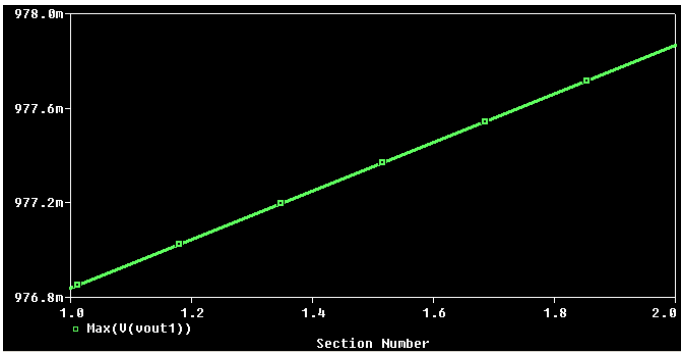

Fig. 12. Worst case sensitivity for output signal V_{O1}

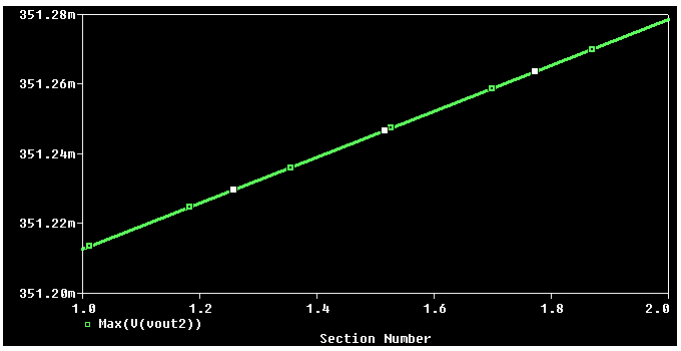

Fig. 13. Worst case sensitivity for output signal V_{O2}

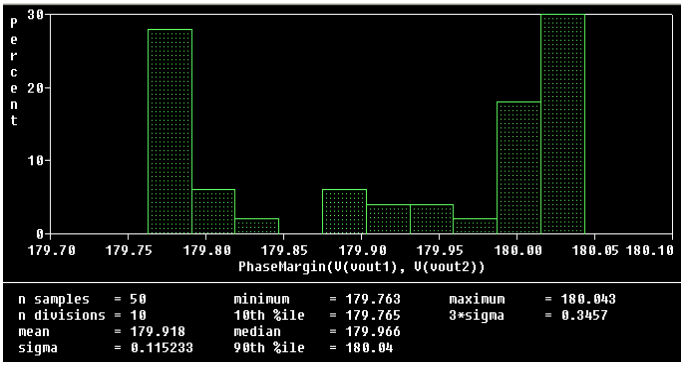

Fig. 14. Phase margin between the output signals.

TABLE II
SIMULATION CONDITIONS AND THE PERFORMANCE CHARACTERISTICS OF CCCII

S. No	Transistor Count	PDP (aJ)
1.	Supply Voltage	±1 V
2.	Power Dissipation	1.7065 mW
3.	Input Bias Current Linear Range	1 µA-500 µA
4.	R_B Ranges	26 Ω to 1300 Ω
5.	R_O	4.68 kΩ
6.	R_Z	1.176 kΩ
7.	R_Y	7.273 MΩ
8.	Total Harmonic Distortion (THD)	1.97 %

TABLE III
COMPARISON OF EXISTING TOPOLOGIES WITH PROPOSED MSO.

Ref	No. of active elements and type	No. of passive elements	Supply Voltage (Volts)	THD (%)	†PCG	*H/S Results
[4]	3, DXCCII	12	±1.25	----	Yes	S
[5]	4, CCCII	4	±1.25	2.9	Yes	S
[14]	3, ZCCDU	6	±1.5	0.24	No	H
[15]	3, CCCII	3	±2.5	----	Yes	S
[16]	4, CBTA	4	±1.5	2.1	Yes	S
[17]	4, CCDU	5	±1.5	2.2	Yes	S
This work	3, CCCII	3	±1 (±6 V)	1.97	Yes	S (H)

†PCG: Passive Components Grounded, *H: Hardware, S: Simulation

The comparative analysis of the proposed circuit is given in Table III. The proposed model employs less number of active devices and passive components for realization and are grounded. The circuits in [4] have the drawback of using more passive components. The circuit of [5] has the advantage of using less passive components but at the cost of 2.9% of the Total Harmonic Distortion (THD). The circuit in [14] has low THD of 0.24% but has the drawback that the passive components are not grounded. The grounded capacitor provides the feature such as reduced noise and low parasitic effects. The circuit of [15] has less number of active and passive devices and are grounded. Though the supply voltage as mentioned in [16] and [17] is low, but it suffers from the distortion levels of 2.1% and 2.2% respectively. While comparing the above circuits, the proposed method has the advantage of requiring less supply voltage with satisfactory THD of 1.97% and also hardware results are verified.

V. Measured Results

CCCII equivalent model has been put to implementation using the structure shown in Fig. 15 [18]. The hardware implementation on laboratory breadboard with external passive components of proposed MSO of Figure 3 is realized with commercially available Current Feedback Operational Amplifiers (CFOAs) of IC AD844AN [22] and Operational Transconductance Amplifiers (OTAs) of IC LM31600 [23] that produces the waveform as shown in Figure 16. For $C_1 = C_2 = 0.01$ µF, I_B = 100 µA, R=10 kΩ and supply voltage of ±6 V are selected to produce the experimentally measured time period of 54.79 µs, whereas, the theoretical time period is 50.99 µs and the results are found to be close to each other. The experimental results of output voltages in *X*-*Y* mode measured on oscilloscope and able to produce 180° phase shift as shown in Figure 17. As the tunability plot obtained for the measured results is more or less replica of the simulated ones which are already presented, and not included here.

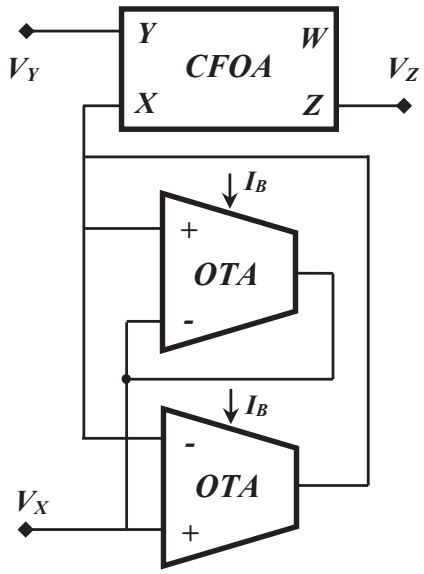

Fig. 15. Implementation of CCCII+ using CFOA and OTAs

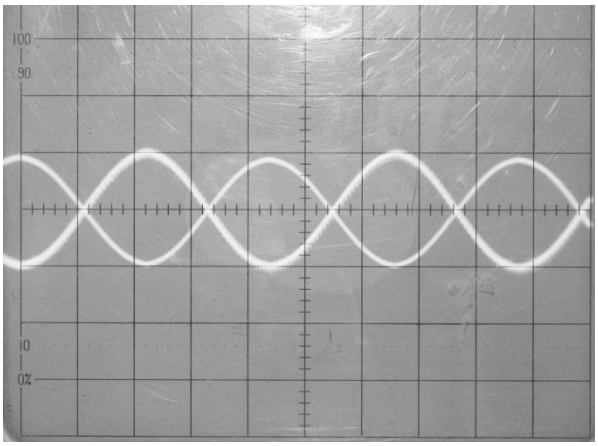

Fig. 16. Experimental results of the proposed MSO in Fig. 3. Scale X-axis: 10 µs/div and Y-axis: 2 V/div.

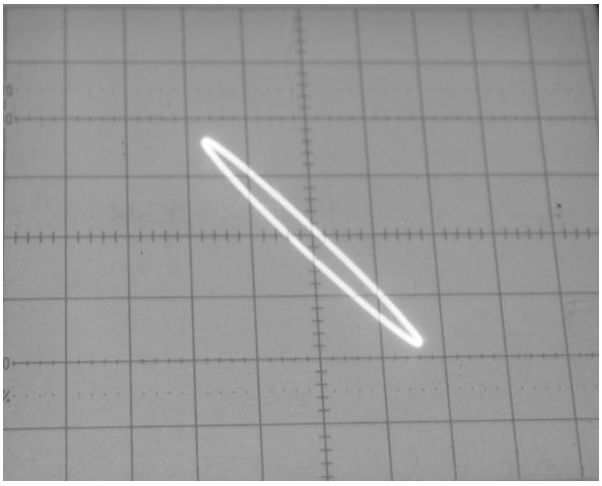

Fig. 17. Experimental results of the Fig. 3 output voltages V_{o1} Vs V_{o2}.

VI. Conclusion

In this manuscript, a current mode electronically tunable Dual Output Sinusoidal Oscillator using three CCCIIs is presented. The oscillation frequency can be tuned to a maximum of 500 kHz by tuning the external bias currents of CCCIIs. The circuit has one resistor and two capacitors that are grounded, which is more advantageous in IC fabrication. Simulation results verifying the theoretical analysis are included along with frequency spectrums. Sensitivity parameters and performance characteristics are also determined. Hardware results of the proposed MSO are in agreement with the software results. Temperature analysis with respect to the variation of amplitudes and THD are also determined. The comparative analysis drawn for the proposed topology is made with the existing methods. The reported electronically tunable MSO has a simple structure that is requiring less area, dissipating at low power of 1.7065 mW and low THD of 1.97%.

References

[1] A. S. Sedra, G. W. Roberts and F. Gohh, "The current conveyor: history, progress and new results," *IEE Proceedings (Part G) of Circuits, Devices and Systems*, vol.137, no. 2, April 1990, pp. 78-87. DOI:10.1049/jp-g-2.1990.0015.

[2] A. Srinivasulu, "A novel current conveyor-based Schmitt trigger and its application as a relaxation oscillator," *Int. J. Circuit Theory and Applic*, vol. 39, no. 6, pp. 679-686, 2011. DOI:10.1002/CTA.669.

[3] A. Srinivasulu and P. Ch. Shaker, "Grounded resistance/capacitance-controlled sinusoidal oscillators using operational transresistance amplifier", *WSEAS Trans. on Circuits and Syst.*, vol. 13, pp. 145-152, 2014.

[4] M. S. Ansari, Iqbal A Khan, Parveen Beg, Ahmed M. Nahhas, "Three passive mixed-mode CMOS VCO with grounded passive components," *Electrical and Electronics Engineering,* vol. 3, no. 6, pp. 149-155, 2013. DOI: 10.5923/j.eee.20130306.02.

[5] S. Maheshwari, R. Verma, "Electronically tunable sinusoidal oscillator circuit," *Active and Passive Electronic Components*, vol. 2012, pp. 1-6, 2012. DOI:10.1155/2012/719376.

[6] R. Pandey, N. Pandey, M. Bothra and S. K. Paul, "Operational Transresistance Amplifier based multiphase sinusoidal oscillators," *Journal of Electrical and Computer Engineering*, vol. 2011, pp. 1-8, 2011. DOI: 10.1155/2011/586853.

[7] M. Kumngern and S. Junnapiya, "A sinusoidal using translinear current conveyors", in *Proc. of IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Kuala Lumpur, Malaysia, 06 - 09 Dec 2010, pp. 740-743, 2010. DOI: 10.1109/APCCAS.2010.5774754.

[8] A. Bhargav, A. Srinivasulu and D. Pal, "An Operational Transconductance Amplifiers Based Sinusoidal Oscillator Using CNTFETs, *in Proc. of the 23rd IEEE International Conference on Applied Electronics*, Pilsen, Czech Republic, 11 Sept - 13 Sept, 2018, Pages-6. DOI: 10.23919/AE.2018.8501428.

[9] S. Zahiruddin and A. Srinivasulu, " A high frequency tunable sinusoidal oscillator using single CCCII+", in *Proc. of IEEE International conference on Control, Instrumentation, Communication and Computational Technologies* (ICCICCT 2015), pp. 490-493, 2015. DOI: 10.1109/ICCICCT.2015.7475323.

[10] A.K.M.S. Haque, MD M. Hossain, W. Alan Davis, H. T. Russell and R. L. Carter, "Design of sinusoidal, triangular, and square wave generator using current feedback amplifier (CFOA)," *IEEE Region 5 Conference*, Kansas, USA, pp. 1-5, 2008.

[11] P. Prommee, M. Somdunyakanok, K. Angkeaw, "CCCII-based multiphase sinusoidal oscillator employing high-pass sections", *in proc. of* the 6th International Conference on Electrical Engineering/ Electronics, Computer, Telecommunications and Information Technology, Pattaya, Chonburi, Thailand, Vol. 01, pp. 530 - 533, 2009, DOI: 10.1109/ECTICON.2009.5137063.

[12] A. Srinivasulu and D. Pal, "CCII+ Based Dual Square-Cum-Triangular Waveform Generator", in proc. of IEEE International Conference on Electronics, Computers and Artificial Intelligence, Targoviste, Romania, 29 June - 01 July, 2017, pp. 6. DOI:10.1109/ECAI.2017.8166422.

[13] D. Pal, A. Srinivasulu, B. B. Pal, A. Demosthenous, and B. N. Das, "Current conveyor- based square/triangular waveform generators with improved linearity," *IEEE Tran. Instr. and Measuremen*, vol. 58, no.7, pp.2174-2180, 2009. DOI: 10.1109/TIM.2008.2006729.

[14] Jirivavra and J. Bajer, "Current-mode multiphase sinusoidal oscillator based on current differencing units," *Analog Integrated Circuits Signal Proc.*, vol.74, pp. 121-128, 2013. DOI 10.1007/s 10470-012-9906-8.

[15] M. Kumnegern, J. Chanwutitum and K. Dejhan, "Electronically tunable multiphase sinusoidal oscillator using translinear current conveyors," *Analog Integrated Circuits Signal Processing*, vol.65, pp. 327-334, 2010. DOI: 10.1007/s 10470-010-9470-z.

[16] M. Sabgas, U. Engin Ayten, N. Herencsar and S. Minaei, "Current and voltagemode multiphase sinusoidal oscillators using CBTAs," *Radioengineering*, vol.22, no.1, pp. 24-33, 2013.

[17] J. Jin, L. Xiao, Xi Yang, B. Liao and S. Li, "Dual mode multiphase sinusoidal oscillator with equal amplitudes," *Engineering Review*, vol. 36, issue 3, pp. 211-220, 2016.

[18] C. Chanapromma, N. Maneetien and M. Siripruchyanum, "A practical implementation of the CC - CFA based on commercially available ICs and its applications", *in Proc. of Int. Conf. on Electrical Engineering/ Electronics, Computer, Telecommunications and Information Technology* (ECTI-CON 2009), Pattaya, Chonburi, 6-9 May, 2009, pp. 564-567.

[19] M. T. Abuelma'atti and M. A. Al-Qahtani, " A new current controlled Multiphase sinusoidal oscillator using translinear current conveyors," *IEEE Transactions on circuits and systems-II, Analog and Digital processing*, vol. 45, no.7, pp. 881-885, July 1998.

[20] A.Lahiri, "Deriving (MO) (I) CCCII based second-order sinusoidal oscillators with non-interactive tuning laws using state variable method," *Radioengineering*, vol. 20, no.1, pp. 349-353, 2011.

[21] T. Piyatat, W. Tangsrirat and W. Surakampontorn, "Electronically tunable quadrature oscillator using current controlled voltage conveyors," *in Proc. of IEEE Conference on Electron Devices and Solid State Circuits,* pp. 133-136, Hong Kong, China, 2005. DOI: 10.1109/EDSSC.2005.1635224.

[22] AD844 Current Feedback Op-Amp Data Sheet, Analog Devices Inc., Norwood, MA, 1990 [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/AD844.pdf [Accessed: October 14th, 2019].

[23] LM13600, Dual Operational Transconductance Amplifiers Data Sheet, National Semiconductor, 1995 [Online]. Available: http://www.datasheetcatalog.com/datasheets_pdf/L/M/1/3/LM13600.shtml [Accessed: October 14th, 2019]

Contribution to Time and Frequency Analysis of Irregular Sleep Snoring

Mohamed Rezki, and Abdennour Alimohad

***Abstract*—The purpose of this paper is to give a summary analysis of human snoring and its episodes. In particular, we consider an acute snoring. In order to extract some frequency information of snoring signal, we apply the Fast Fourier Transform (FFT), Short Time Fourier Transform (STFT) algorithms, Discrete Wavelet Technique, and Power Spectral Density (PSD). Once irregular snoring characterized, we use a Voice Activity Detection (VAD) for snoring episode detection. Furthermore, we give comparative study of three types of thresholds that can control the VAD approach, a fixed threshold, a soft threshold, and a Gaussian threshold. Next, we use a Perceptual Evaluation of Speech Quality (PESQ) method to evaluate the efficiency of the VAD. We find that VAD based on Gaussian threshold is better.**

***Index Terms*—Sleep Snoring; Frequency Analysis; Time Analysis; Thresholds; Snore quality measures.**

Original Research Paper
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I. Introduction

Snoring is an inspiratory noise caused by vibration of the soft supper-airway tissues, mainly soft palate and posterior faucial pillars [1]. Mostly, snoring can provoke obstructive sleep apnea with the possibilities of higher risks of cardiovascular disease such as heart attacks, strokes, sleep disorders, etc. [2]. With the development of the signal processing tools, many fields of study have been opened and thus non-stationary and complicated signals such as irregular snoring can be analyzed. In addition, one of the most famous processing techniques is the use of wavelet because it can express signals with different frequency components [3].

Also, it offers statistical analysis tools such as histograms. The wavelet-based histograms provide us the ability to naturally extend to multidimensional case, a good optimization [4] and to improve the accuracy substantially over random sampling [5].

Several studies have been done on detection and analysis of sleep snoring (acoustical characterization) based on the classification methods using some experimental databases through the choice of selected features [6]—[8]. Furthermore, other authors treated the sleep snoring by the application of personalized software. Statistical parameters such as the number of the snoring episodes , duration , etc. were calculated in [9]-[10].

However, all these works require a complete characterization with integration of aspects of time and frequency at the same time. In the present work we establish a global model based on time and frequency analysis with integration of the VAD (Voice Activity Detection). In addition, we show the effect of changing the VAD threshold on the efficiency of detection of snoring episodes.

The remainder of the paper is organized as follows: In section 2, we present the different processing frequency techniques used to analyze the sleep snoring, Section 3 is devoted to describe the theoretical and practical approach for time analysis of sleeps snoring. Finally, we give a summary conclusion in section 4.

II. Theoretical Approach for Frequency Analysis

The signal recorded in [11] is considered the strongest snoring signal characterized also by its high irregularity. So we can consider it as an obstructive sleep apnea (OSA) signal, which contains an apnea part (see Fig. 1 [8]).

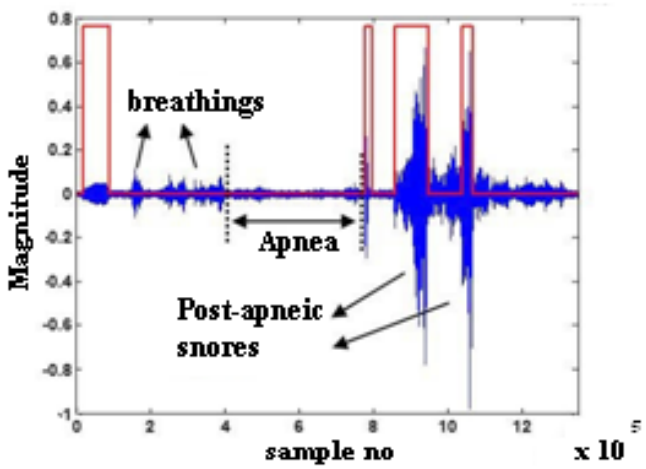

Fig. 1. Detection of snoring episodes for the OSA patient having both regular and post-apneic snoring sounds (rectangular pulse in red represents sound segments). [8].

Fig.1 shows four breathing cycles separated by four snoring periods. And we observe that when the breathings become much

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attenuated during a long time it becomes an episode of apnea. After the apnea episode the snoring becomes quite intense and very irregular what is called post- apneic episodes.

A. Processing techniques

A.1. Fast Fourier Transform

The Fast Fourier Transform (FFT) was derived from the Discrete Fourier Transform (DFT), which is given by [12]:

$$y_k = \sum_{n=0}^{N-1} \omega_N^{nk} x_n \tag{1}$$

where $K = 0,\ldots, N-1$, ω_N is the primitive root of unity

$\exp\left(\frac{-2\pi i}{N}\right)$, and N is the size of the input x.

A.2. Short Time Fourier Transform (STFT)

Short Time Fourier Transform (STFT) gives spectrograms that are created either by approximation as a filter Bank or from Fourier transform calculation. The continuous –time STFT for a given time signal x(t) is written as:

$$STFT(x(t)) = X(\tau, f) = \int_{-\infty}^{+\infty} x(t).w(t-\tau).e^{-j2\pi ft} dt \tag{2}$$

where w is the windowing function and f is the frequency. In contrast with the Fourier transform techniques which give the frequency part, the STFT allows to operate in frequency and time.

A.3. Wavelet Transform

The Wavelet Transform is a particular technique that describes signals in both time and frequency domains**.** Its physical form is a small window (mother wavelet) which is used to scan a macro signal [3]. The wavelet equation as a function of mother wavelet is given by:

$$\varphi_{a,b}(t) = |a|^{-\frac{1}{2}} \varphi\left(\frac{t-b}{a}\right) \tag{3}$$

where *a, b* are, respectively, the dilation and translation parameters, and $\varphi(t)$ is called the single mother wavelet.

In literature, there exits two large groups of wavelets: continuous and discrete. The Continuous Wavelet Transform (CWT) for a given function $f(t)$ is defined as [3]:

$$W_f(a,b) = |a|^{-\frac{1}{2}} \int_R f(t) \overline{\varphi\left(\frac{t-b}{a}\right)} dt \;\; a,b \in R; a \neq 0 \tag{4}$$

where $\overline{\varphi\left(\frac{t-b}{a}\right)}$ denotes the complex conjugate of the wavelet function $\varphi\left(\frac{t-b}{a}\right)$.

Next, the Discrete Wavelet Transform (DWT) is a sampling wavelet using a bank of filters. It is given by [13]:

$$W(l,s) = 2^{\frac{s}{2}} \sum_n x(n) \Psi(2^s n - l) \tag{5}$$

where n=1, 2,…N and N is the total number of samples, *l* describes the shifting and *s* is the scale.

Examples of the discrete mother wavelets are presented in Fig. 2.

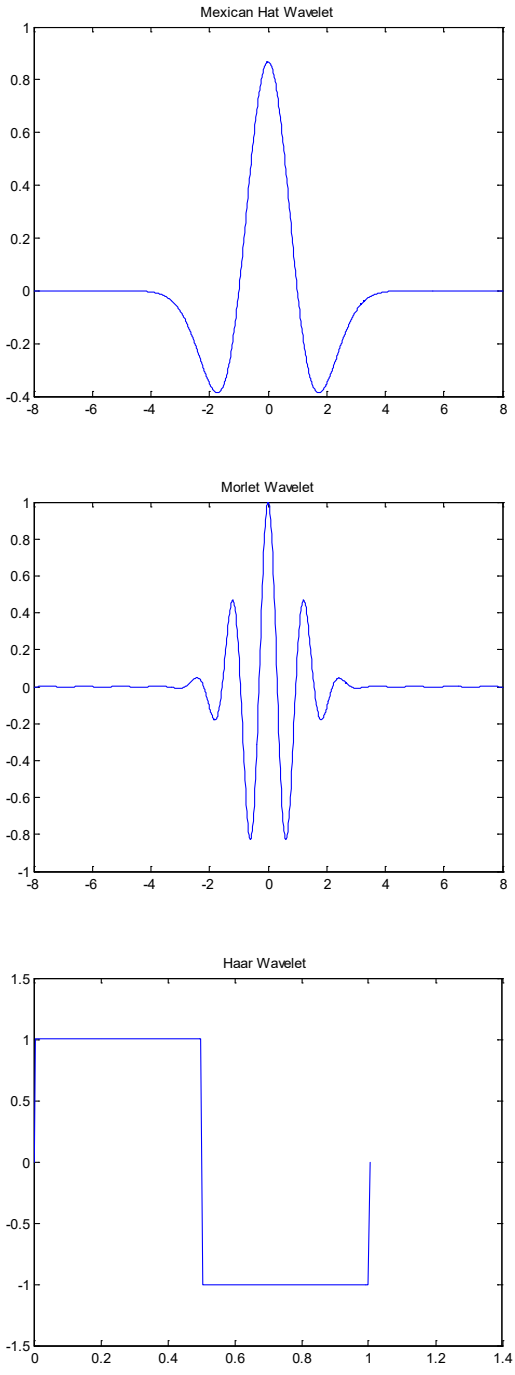


Fig. 2. Discrete mother wavelets examples.

A.4. Spectral analysis

The power spectral density (PSD) estimation has many applications such as the elimination of the wide-band noise mixed to the useful signal. PSD allows also, seeing the real distribution of the signal power depending on its frequency. In other word, the power spectral density represents the power content of a signal in an imperceptible frequency band contrary to the power spectrum that shows the frequencies which contain the signal's power. In order to estimate the power spectral density, we use the Welch's method that is described as follows [14]-[15]:

First, the original data is split up into overlapped data segments. Second, a window signal is applied to each segment.

Noticing that the windowing operation is what makes the Welch method a "modified" periodogram.

B. Practical aspects of snoring signal frequency analysis

Our experiments were performed on data given by [11], which consists of mp3 sounds. The data were recorded in a high quality format with a sampling frequency of 44100 Hz.

B.1. FFT technique

The application of FFT algorithm to a snoring signal is given in the following figure.

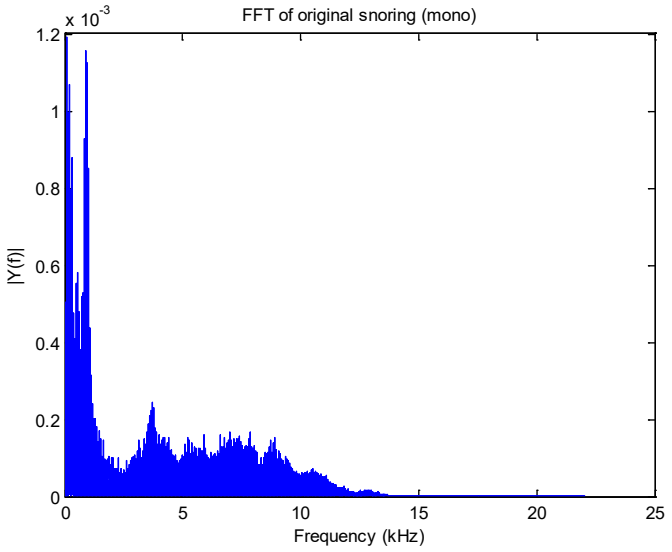


Fig. 3. FFT of original snoring.

As we can see, Fig.3 displays only the positive half of the frequency spectrum and discards the redundant negative half. Therefore, the spectral component extends to half the sampling frequency (around 22 kHz).

We can deduce from Fig. 3 that the main part of the snoring signal reaches 14 kHz and the FFT signal has two highest picks at 0.06 kHz and 0.88 kHz.

B.2. STFT technique

In this part we compute the STFT for the snoring signal and the apnea part, which are presented, respectively, in Fig.4 (a) and Fig. 4 (b).

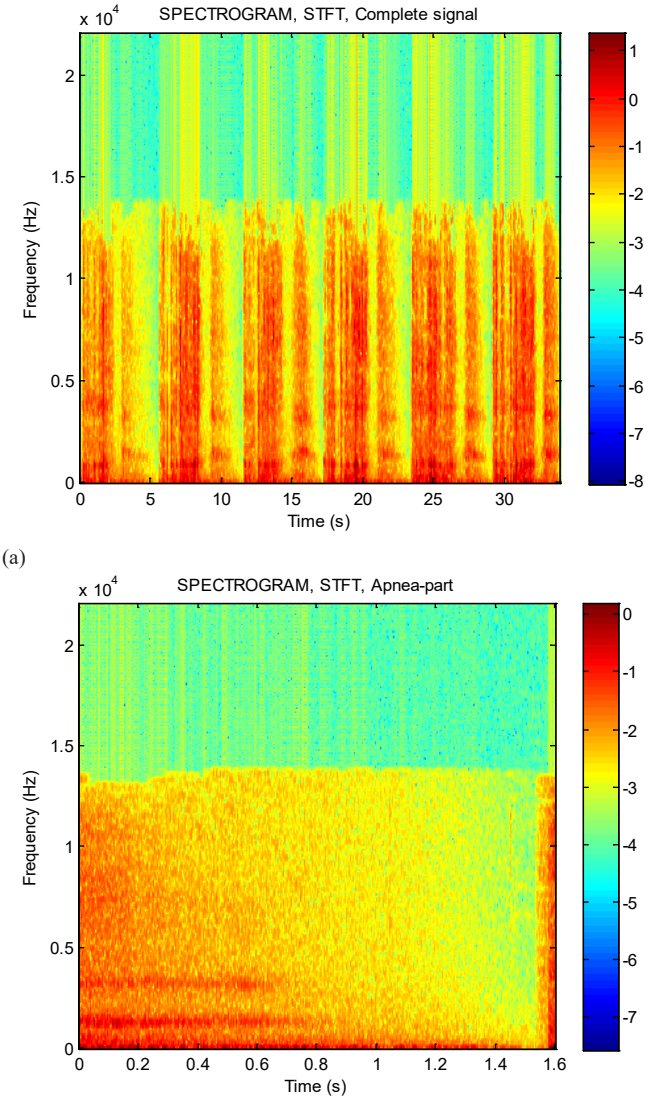


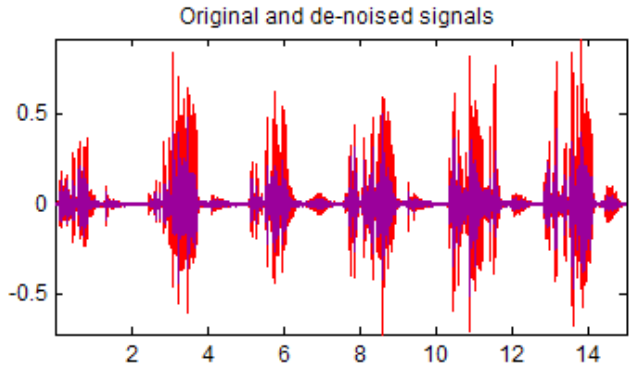
Fig. 4. STFT of original snoring: (a) Complete signal, (b) Apnea-part of snoring signal.

It's clear from Fig.4(b) that the STFT of the apnea-part has greatly lower magnitude then the STFT of the complete signal (Fig 4.a). This result confirms the fact that the apnea part follows a quite audible snore. And the presence of apnea is related to the existence of a strongly snore (see Fig. 1).

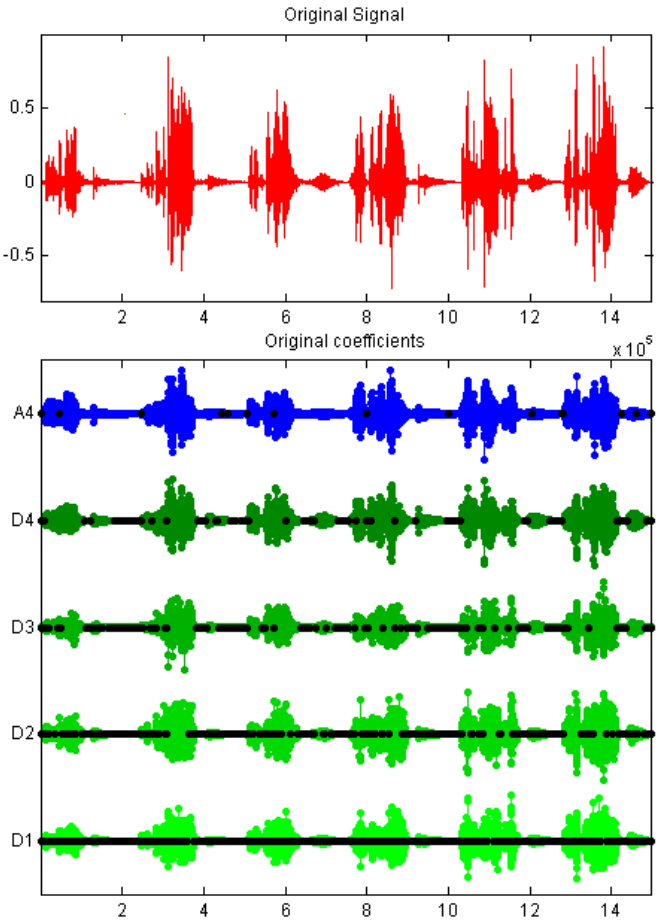
B.3. Discrete Wavelet Transform technique

Here, we analyze the snoring signal using the Discrete Wavelet Transform with four level Haar wavelet. This level presents the advantage of having minimal coefficients of decomposition (A4, D1, D2, D3, D4).

In practice, we find that over 4 levels, the signals will have a different shape compared to the original signal. So, we compute 4 levels of decomposition and the obtained results are shown in Fig. 5.



(a) Loaded and de-noised signals (red & purple colors respectively)



(b) Original details coefficients

Fig. 5. Wavelet decomposition of the snoring signal and its de-noised operation.

The outputs "**A**" and "**D**" are the reconstruction wavelet coefficients [16]:

- The approximation output A: is the low frequency content of the input signal component.
- The multidimensional output D: gives the details or the high frequency components of the input signal at various levels.

From Fig.5 (a), we noticed that the wavelet de-noising of the signal gives a nuanced result with attenuation of amplitude and a slight decimation of the fluctuations.

In order to derive statistical information from the wavelet analysis, a histogram is used. The representation of this histogram is given in Fig. 6.

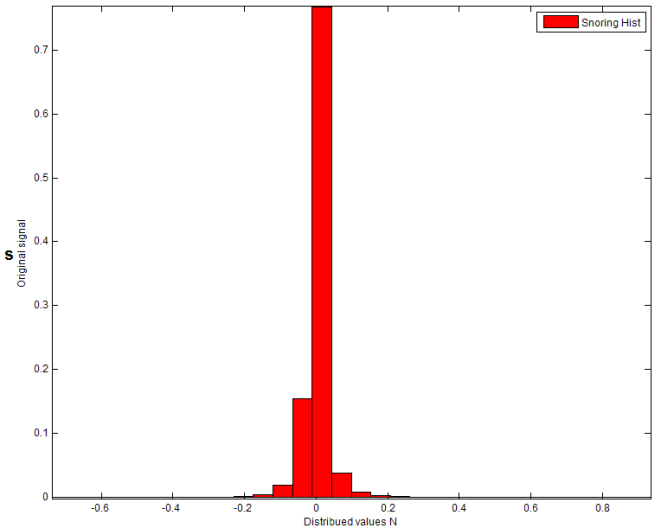


Fig. 6. Histogram representation of the snoring signal.

From Fig. 6, we observe that the distribution of the positive and negative values is not the same (considering the non-stationary character of the signal). Also, the major concentration of the values (almost 85 %) is around zero.

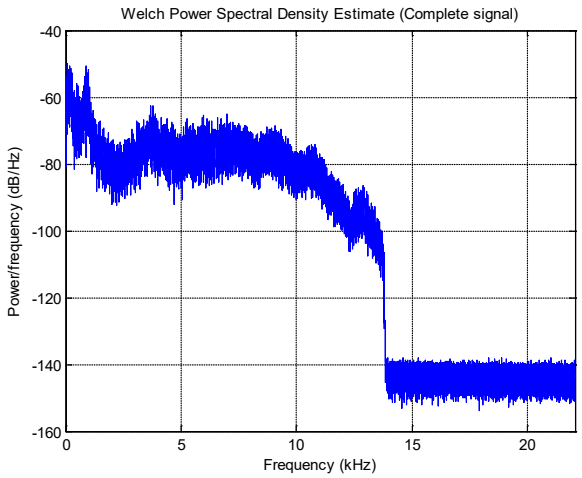
Finally, we noticed that the shape of the histogram reflects the Gaussian nature of the signal distribution which will be exploited in section III.

B.4. Power Spectral Density technique and Spectral Envelope

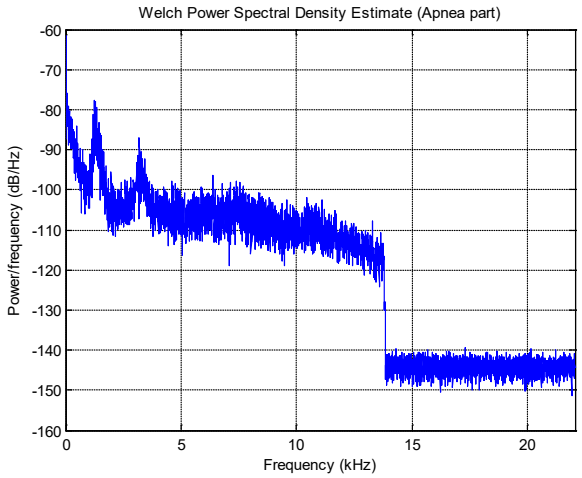
The computation of the Power Spectral Density (PSD) is realized using the Welch's method. Therefore, the PSD of the snore signal is shown in Fig. 7.

The Fig. 7 shows that the smooth character of the complete snoring signal is better than the apnea part, and the most energy of the signal (complete or partial) is concentrated in the frequency interval [0 14] (kHz). We can also see the existence of some peaks such as at 1.25 kHz and at 3.2 kHz. These peaks are important because they help to locate formants of an acoustic signal. These formants are used, as parameters, in many applications such as acoustic synthesis and speech recognition. In addition, we can see the existence of an abrupt decrease in energy around the frequency 14 kHz (exactly 13.8 kHz). This is due to the non-regular nature of the snoring signal.

Next, to confirm the results of the power spectral density technique, we apply the spectral envelope method that represents the spectral magnitude versus the frequency. And gives an envelope to the spectrum by linking the peaks. In Fig. 8, we show the spectral envelope of the snoring signal.

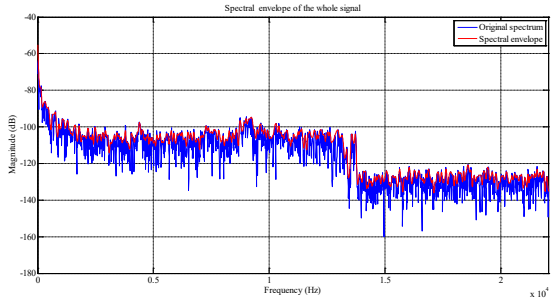


(a)

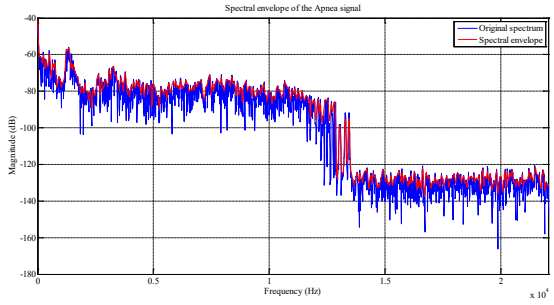


(b)

Fig. 7. Welch power spectral density estimation of: (a) Complete signal, (b) Apnea-part of snoring signal



(a)



(b)

Fig. 8. The spectral envelope of: (a) Complete signal, (b) Apnea-part of snoring signal

The results shown in Fig.8 are similar to those of Fig. 7, and we have the same collapse of power around the frequency 14 kHz.

III. Theoretical Approach of Time Analysis

The International Telecommunication Union (ITU) had imposed and coordinates some standards for telecommunications to better exploit the frequency band of speech. Among these standards, the silence elimination in speech keeps only the voice. This latter guarantees the effectiveness of transmission, because only speech activity is detected and treated.

The most used technique for silence elimination is VAD (Voice Activity Detection), it consists of detecting the presence or absence of human speech.

In our case, we consider the snoring signal as the voice and the long delay between two episodes of snore as an apnea sequence.

Various VAD algorithms have been developed. These algorithms used an energy threshold to separate the presence or absence of voice. In this work, we propose to introduce the VAD technique in our system to detect apnea episodes in the snoring signal. This is shown in the following figure (Fig. 9).

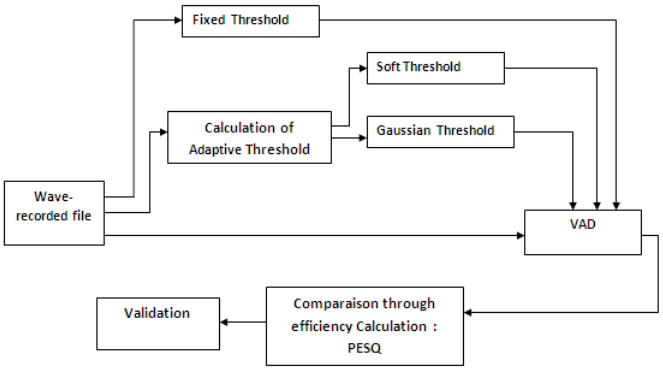


Fig. 9. Flow chart of the proposed system

We have applied three (03) different thresholds. First, we consider a fixed threshold with an experimentally value of 0.05. Then, we use an adaptive threshold which varies according to each frame of the snoring signal. For this latter threshold, we have selected two (02) techniques, a soft threshold and a Gaussian threshold.

The soft threshold was given by D.L. Donoho in [17] as:

$$tw2 = k.w_{mean}.(\sigma_w) \tag{6}$$

w_{mean} is a parameter depending on the frames number, the energy of each frame and the zero crossing number. k is a constant which can be determined empirically. σ_w^2 is the variance. Finally, the Gaussian threshold is expressed as follows:

$$tw3 = \frac{FWHM}{2.\sqrt{2}\log(2)} \tag{7}$$

where $FWHM$ is the Full Width at Half Maximum, which expressed the difference between the two extreme values of

the Gaussian distribution. Since we have shown the Gaussian nature of our snore signal (see Fig. 6), we apply this last threshold to each frame of the signal. Thresholds mean is then taken (Fig. 10).

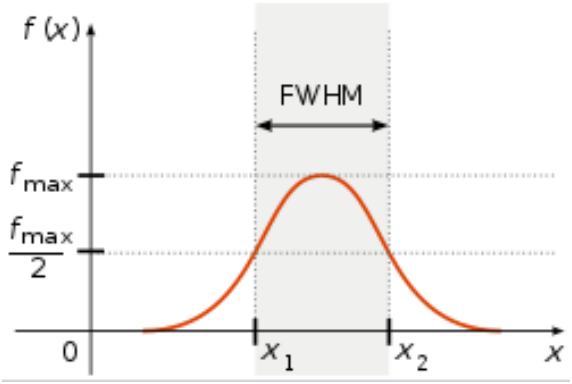


Fig. 10. Shape of a Full width at half maximum

As an example, Fig.11 presents the Gaussian distribution corresponding to the 10th frame.

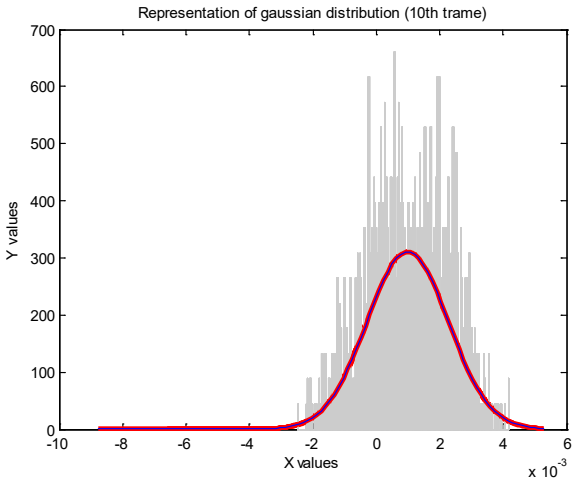
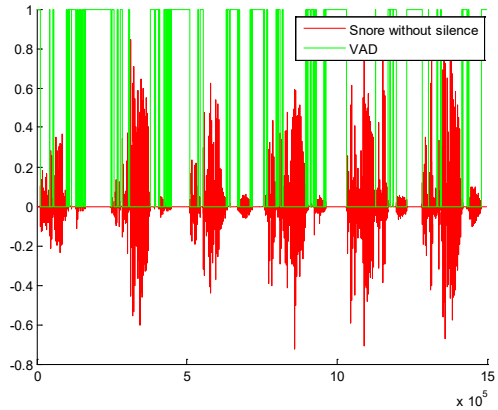
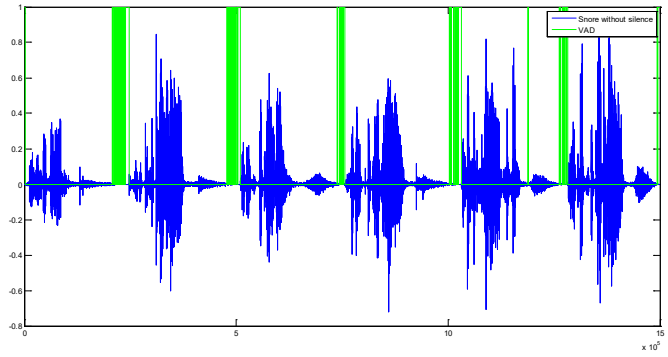


Fig. 11. FWHM of the 10th frame.

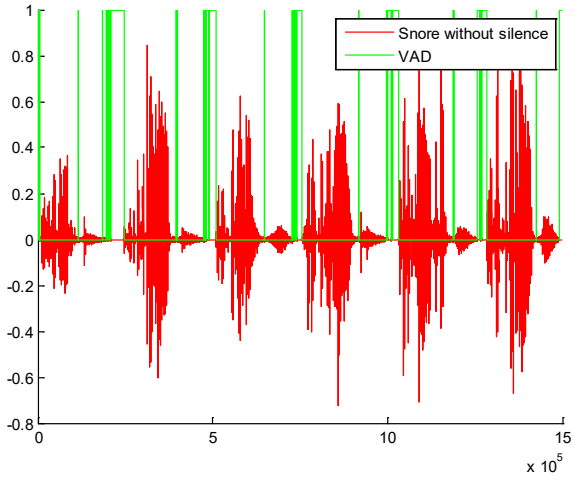
The application of the VAD technique based on the different thresholds, cited before, gives the following results:



(a)



(b)



(c)

Fig. 12. Detection of snoring episodes by applying the VAD with: (a) fixed threshold, (b) soft threshold, and (c) Gaussian threshold.

We remark from Fig.12 that the duration of the snoring episode depends on the VAD, and more precisely on the threshold level. Notice also that the decision of considering a silence as a sleep apnea episode depends on its duration, its repetition per hour, and a subject examination by a doctor.

A. Performance evaluation measure of the proposed system:

Measuring the quality of a sound signal is an important and a very difficult task. There are objective and subjective measures. These latter are based on the tests of direct listening (qualified normative auditors who hear). These measures are expensive and difficult to apply on a snoring signal. Therefore, they have been replaced by objective methods [18].

Several objective speech quality measures were evaluated such as: segmental Signal to Noise Ratio (segSNR), distortion (signal distortion, background distortion), PESQ (Perceptual Evaluation of Speech Quality) and others [19].

Perceptual Evaluation of Speech Quality, is a standardized objective method of measuring speech quality. A detailed description of PESQ can be found in ITU-T Recommendation P.862 (02/01) (standards for telecommunications and Information Communication Technology of the International Telecommunication Union 'ITU') [20]. The original and degraded

signals are aligned in time to correct for delays, and then processed through an auditory transform to obtain the loudness spectra. The absolute difference between the degraded and original loudness spectra is used as a measure of audible error in the next stage of PESQ computation. The objective evaluation allows transformation of the reference and degraded signal to an internal representation resembling a psychophysical representation of audio signals in the human auditory system [21].

The final PESQ score is computed as a linear combination of the average symmetrical disturbance value d_{sym} and the average asymmetrical disturbance value d_{asym} as follows [22]:

$$PESQ = a_0 + a_1.d_{sym} + a_2.d_{asym} \quad (8)$$

where $a_0 = 4.5$, $a_1 = -0.1$ and $a_2 = -0.0309$.

We have chosen PESQ in order to show that the quality of a signal containing the information (speech, snoring, etc.) still remains acceptable after truncation following the use of the VAD. By applying the PESQ_MOS (wideband measurements) to our system with two sampling frequencies: 44100Hz (original recording frequency) and 16000 Hz (standard frequency for PESQ), we get the results shown in Table 1. Notice that the PESQ calculation was done using the software given in [19].

Table I
Performance Evaluation measure by PESQ

Sampling frequency (Hz)	PESQ (fixed threshold)	PESQ (soft threshold)	PESQ (Gaussian threshold)
44100	2.9706	4.0261	4.5000
16000	2.5648	3.9832	4.4095

According to Table I, the best PESQ score is given for the Gaussian threshold, this confirms the superiority of adaptive threshold compared to the fixed threshold.

IV. Conclusion

In this work, we analyzed an irregular sleep snoring signal using several methods in time and frequency. The results in frequency domain were obtained by applying the Fast Fourier Transform (FFT), the Short Time Fourier Transform (STFT), the Discrete Wavelet Transform (DWT), and Power Spectral Density (PSD). Which show the existence of some peaks that can be used to locate formants of the snoring signal and its frequency band. These results were also confirmed by using the spectral envelope method. Concerning the time domain, Three variants of VAD technique were used to detect the snoring/apnea episodes. Where, the VAD uses respectively, a fixed threshold, an adaptive soft threshold, and a Gaussian threshold. In order to choose the best threshold, a performance study of the method was done through the use of two (02) criterias. Firstly by subjective criteria via a simple listening of the sound signal issued from the VAD. Secondly by calculating the PESQ (Perceptual Evaluation of Speech Quality) score which is an objective quality measure. Both methods have confirmed that the Gaussian threshold is the best.

References

[1] M. Partinen, "Chapter 18 - Epidemiology of sleep disorders", *Handbook of Clinical Neurology*, vol. 98, p.p. 275-314, 2011.

[2] (How to Stop Snoring: Causes, Aids, Remedies) Siamak N. Nabili. Available: https://www.medicinenet.com/snoring/article.htm, (Date accessed: 04 July 2019).

[3] Z. Yinhong, L.Quanlu, "The Study of the Snoring Signal Analysis Wavelet Transform", in *Recent Advances in Computer Science and Information*, Lecture Notes in Electrical Engineering, vol. 129. Springer-Verlag, Berlin Heidelberg New York, p.p.67-75, 2012.

[4] Y. Matias, J. S.Vitter, and M. Wang, "Dynamic Maintenance of Wavelt-Based Histograms", *Proceedings of the 26th International Conference on Very Large Data Bases, VLDB'00*, pp. 101-110, 2000.

[5] T. Li, Q. Li, S. Zhu, and M. Ogihara, "A Survey on Wavelet Applications in Data Mining", *SIGKDD Explorations*. vol.4, no 2, pp.49- 68, 2002.

[6] C. Wang , and J. Peng, "The Methods of Acoustical Analysis of Snoring for the Diagnosis of OSAHS", *Journal of Sleep Medicine & Disorders,* vol, no2, pp.1-7, 2017.

[7] M.M.D. De Meyer, W. Jacquet, O.M. Vanderveken, L.A.M. Marks, "Systematic review of the different aspects of primary snoring ", *Sleep Medicine Reviews,* p.p. 1-32, 2019.

[8] M. Cavusoglu, C.F. Poets, and M.S.Urschitz., "Acoustics of snoring and automatic snore sound detection in children", *Physiological Measurement*, vol.38, no.11, pp.1919-1938, 2017.

[9] M. Cavusoglu, M. Kamasak, O. Erogul, T. Ciloglu, T. Akcam, Y. Serinagaoglu, "SASA: A Software System for Sleep and Snoring Analsis", *HIBIT'07- international symposium on health informatics and bioinformatics,* pp.1-8, 2007.

[10] B. Calabrese, F. Pucci, M. Sturniolo, P.H. Guzzi, P. Veltri, A. Gambardella, M. Cannataro, "*A* System for the Analysis of Snore Signals", *International Conference on Computational Science, ICCS 2011, Procedia Computer Science,* vol.4, pp. 1101–1108, 2011.

[11] Salamisound: Sound Effect. Available: http://www.salamisound.com/2045645-heavy-snoring-very-irregular (Date accessed: 22 December 2017).

[12] S. G. Johnson, M. Frigo, "A Modified Split-Radix FFT With Fewer Arithmetic Operations", *IEEE Transactions on Signal Processing*, vol. 55, no.1, p.p.111-119, 2007.

[13] M. Aqil, A. Jbari, A. Bourouhou, , "ECG Signal Denoising by Discrete Wavelet Transform", *International Journal of Online and Biomedical Engineering (iJOE)*, vol.13, no.9,pp. 51-68, 2017.

[14] Spectral density – Using pwelch to a set of signals: some questions (Matlab). Available: https://stackoverflow.com/questions/35528353/using-pwelch-to-a-set-of-signals-some-questions-matlab, (Date accessed: 04 July 2019)

[15] P. Sysel, Z. Smekal, "Enhanced estimation of power spectral density of noise using the wavelet transform" in 2007, *IFIP International Federation for Information Processing*, vol. 245.Personal Wireless Communications, Boston: Springer, pp. 521-532, 2007.

[16] Discrete Wavelet Transform (DWT). Available: https://hvdc.ca/webhelp/Master_Library_Models/CSMF/Discrete_Wavelet_Transform_(DWT)/Discrete_Wavelet_Transform_(DWT).htm, (Date accessed: 07 July 2017).

[17] D. L. Donoho, "De-noising by soft-thresholding", *IEEE Transactions on Information Theory*,vol.41. pp. 613–627, 1995.

[18] M. Guéguin, "Evaluation objective de la qualité vocale en contexte de conversation (Doctoral thesis),", Lab. Traitement du signal et de l'image, Université Rennes 1, 2006.

[19] H. Yi , and P.C. Loizou , "Evaluation of objective measures for speech enhancement", *IEEE Transactions on Audio, Speech, and Language Processing*,vol.16, no.1, pp. 229-238, 2006.

[20] ITU-T Recommendation P.862. "Perceptual Evaluation of Speech Quality (PESQ), an Objective Method for End-To-End Speech Quality Assessment of Narrowband Telephone Networks and Speech Codecs," February 2001.

[21] W. Zhang, Y. Chang, Y. Liu, and L. Xiao, “A New Method of Objective Speech Quality Assessment in Communication System”, *Journal of multimedia*, vol. 8, no. 3, pp.291-298, 2013.
[22] A.W. Rix, J. G. Beerends, M.P. Hollier and A.P. Hekstra, “Perceptual Evaluation of Speech Quality (PESQ) – a new method for speech quality assessment of telephone networks and codecs”, *IEEE International Conference on Acoustics, Speech, and Signal Processing, 2001. Proceedings. (ICASSP ‘01),* volume: 2, pp. 749-752, 2001

PI Regulator with Tracking Anti-Windup Based Modified Power Balance Theory for SAPF under Unbalanced Grid Voltage Unbalance Non Linear Loads

Khechiba Kamel, Zellouma Laid, and Benaissa Amar

***Abstract*—This paper presents a modified power balance theory for extracting the reference compensating currents to shunt active power filter (SAPF) which is applied to illuminate current harmonics and compensate reactive power under unbalanced voltages and unbalancing Nonlinear loads. A new method has been proposed based proportional-integrator (PI) controller with tracking anti-windup protection is presented. The power balance theory is used to establish suitable current reference signals. The studied is carried out with Matlab/Simulink and power system tools to verify the performance of the proposed technique. The filtering method of the SAPF can achieve the THD% limit specified by the IEEE-519 standard.**

***Index Terms*—Power Balance Theory, STF, SAPF, THD, Tracking Windup, Unbalance grid Voltage, Unbalanced non linear loads**

Original Research Paper
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I. Introduction

Due to growing demand of energy, the power distribution system network becomes more and more polluted due to the presence of power electronic-based converts which creates a non-linear load in house appliances such as a television, computer, printers and fax machines, food preparation and cooking, lighting products that include electronic ballasts, and in industrial applications such as variable speed motor drives for HVAC and converter stations, flexible ac transmission system (FACTS), and static var compensators. Almost all new electrical or electromechanical equipment, contain power electronic circuits and/or systems, these loads increase the burden on the distribution system and pollute the supply system, and the harmonics injected by the power converters becomes inevitable and by consequence influence the performance of other loads which are connected to the same load terminal [1]. Therefore, it is clearly stated in the harmonic IEEE standard 519 that the total harmonic distortion (THD) for current should be at most 5%. Hence, the 5% of current THD limit has always been the performance target that all researchers and designers are trying their best to achieve. In the beginning, the researchers propose techniques based on the conventional passive filters [2]. And due to its fixed mitigation abilities and bulky size, the designer replaces them. By another filter which uses power semiconductor switching devices such as insulated gate bipolar transistors (IGBT) [3].

Among the solutions proposed and applied by the research to eliminate these harmonics, and minimize the effects of nonlinear is the shunt active power filter (SAPF) [4]. Very much effort has been made to control the SAPF, and different algorithms emerged for the harmonic detection, which considers the speed, the filter stability, easy, inexpensive implementation, and the detection accuracy, in the time domain as well as in frequency domain.

The time domain methods are most widely used based on the instantaneous derivation of reference current signals from harmonic-polluted sources to gain more speed and less complexity in calculations [5]. To generate the reference current for SAPF, the most popular one that has been developed in the field of harmonic detection is the instantaneous power theory by H. Akagi [6]. Which has been proved to be effective operation and has a good performance under balanced voltage source conditions [7]. Among different harmonic compensation techniques, the SRF (Synchronous Reference Frame) method, which is usually used the LPF as a conventional second order low pass filter to separate the DC component of the current [8]. This method leads to an increase in the reaction time of the active power filter by prolonging the time response of the LPF.

One other problem of the conventional SRF technique is that load current compensation will not be well done if the load terminal voltages are distorted, and thus a PLL (Phase Locked Loop) proposed to extract the direct fundamental component of the network voltage [9].

Some papers have proposed different solutions to improve the result of compensation and the drawbacks of the conventional SRF and PQ methods. In [10]. A modified PLL structure was proposed to improve the THD which is limited in the best case

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to 2.7%. In [11]. A self-tuning filter was used with SRF and PQ under non-sinusoidal load terminal voltage condition.

This method was limited the THD to 2.30%. In [12]. A 2nd order low pass filter wavelet-based multi-resolution analysis is deployed using SOGI (Second Order Generalized Integrator) to extract the fundamental frequency component of an unbalance and nonlinear load current. The THD of this method is limited to 2.08%. In [13], [14]. Icosα algorithm is used which is consider to be the product of its magnitude and a unity of sine wave which can be obtained from PLL block. The THD gets from this method is limited to 1.25However, the three-phase power system cannot be continuously balanced, which is the case in the present time, and the reason of this is the majority of loads in the distribution systems are unbalanced in radial distribution feeders, and the power quality problems are more prevailing in the grid which are prime concerns in the distribution system and this necessitates the study of the combined effect of unbalance and nonlinearity on power system voltages and currents. Thus, the direct application of the instantaneous power theory will result in large errors.

To overcome the limitations in the existing methods, a modified power balance theory is proposed and developed in this paper based on cascade second-order filter to handle unbalanced three-phase voltage sources with unbalance load system with practical considerations. The algorithm is simple with less memory requirement which makes it easy to implement and which uses indirect current control technique in estimating the fundamental load components. The DC capacitor voltage is recovered and attains the reference voltage through the PI controller having anti-windup integral action.

II. Literature Review

The APF technology got a real enhancement and a major factor in advancing the APF technology with the introduction of insulated gate bipolar transistors (IGBTs) [15]. Rather than the use in the initial state the BJTs, MOSFET and GTOs. Based on converter topology, type, and number of phases, the Active Power Filter can be classified Shunt as shown in Fig.1or Series or a combination of both and can be either a voltage source inverter (VSI) or current source inverter (CSI) in terms of type, the classification can also be in terms of phase a two-wire (single phase) and three- or four-wire three- phase systems.

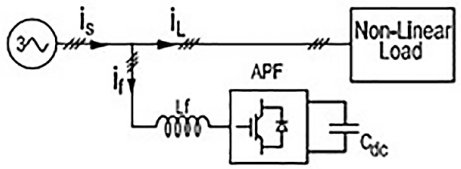

Fig.1. Block diagram of the APF [16]

III. Material and Methods

The main advantage of power balance theory is the fast detection of distortion with high accuracy and quick response extraction of reference source currents. The basic equations of power balance theory for the generation of switching signals for VSC are given below.

A. *The in Phase Component of Reference Source Currents*

$$V_t = \sqrt{2(V_{sa}^2 + V_{sb}^2 + V_{sc}^2)}/3 \quad (1)$$

V_t is the amplitude of the terminal voltage at PCC. The unity sine waves of the phase main voltages are estimated as:

$$V_{au} = (V_{sa}(t)/V_t), V_{bu} = (V_{sb}(t)/V_t), V_{cu} = (V_{sc}(t)/V_t) \quad (2)$$

The consumed load active power will be calculated as follows:

$$P_L = V_t(i_{la}V_{au} + i_{lb}V_{bu} + i_{lc}V_{cu}) \quad (3)$$

The supply current has two components.

- The first is required for DC component of load consumed power

The magnitude of the fundamental active power component of load current can be estimated as:

$$i_{Ldc} = (2/3) * (P_{Ldc}/V_t) \quad (4)$$

Where P_{Ldc} is the DC component extracted from the total consumed active power after filter out by using a self-tuning filter (STF) which is the most important part of this control which allows making insensible to the disturbances and filtering correctly the current.

- The second component is required for the self-supporting DC bus voltage of the filter can be expressed as:

$$i_{Ld} = K_p V_{dce} + K_i \int V_{dce}\, dt \quad (5)$$

Where $V_{dce} = V_{dc} - V_{dc}^*$ is the error in DC bus voltage between the sensed and the reference respectively. The proposed method is to use the PI controller with anti-windup integral action.

In this paper, study has been carried out using tracking anti-windup scheme.

After we obtain the two parts of the currents, we propose to filter out again to eliminate the ripple by using a second-order low pass filter where the cut-off frequency is 50 Hz and the damping factor Zeta is 0.707.

B. *The Tracking Windup*

In nonlinear loads, some effect must be taken into consideration such as the actuator saturation; the neglecting phenomenon leads to closed-loop instability, especially if the process is open-loop unstable.

Such undesirable condition can arise. If the error is too large or it remains non-zero for a long duration during which the integrator causes the rollover [17]. To limit the output a saturation block can be used at the output terminal as shown in Fig. 2.

Fig. 2. Saturation function [17]

Saturation can be defined as the static nonlinearity

$$sat(u) = \{U_{min} if U < U_{min} \quad (6)$$

$$sat(u) = \{U_{min} if U < U_{min} \quad (7)$$

$$sat(u) = U_{max} \; if \; U > U_{max} \quad (8)$$

Whereas the transfer function of a PI controller is expressed as:

$$G_{PI}(s) = K_p + (K_i/s) \quad (9)$$

The closed-loop transfer function of dc voltage regulation is given by:

$$V_{dc}/V_{ref} = (K_p/C) .s\,(K_i/K_P)/[s^2 + (K_p/C)s + (K_i/C)] \quad (10)$$

We can obtain the proportional constant by solving the second order equation above and replacing the values of the capacitor C, the reference DC voltage which is in our case 120V (simulation parameter Table I) and by knowing ζ 0.707, ω and cut off frequency 50Hz respectively.

The choice of limiting gain K_S in Fig. 3 depends on acceptable restriction on integrator output. The higher value keeps the actual output close to the saturated output which in turn enables the controller to come out of saturation quickly when the error reverses.

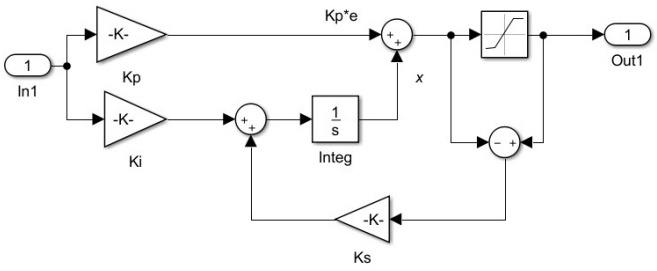

Fig. 3. Block diagram of the Tracking Anti-Windup regulator

Here the difference of actual output and saturated output is fed back through again to reduce the amount of error input error going into the integrator.

From the circuit above

$$U = x + K_p e \quad (11)$$

where:

$$dx/dt = K_i\,(e - K_S(U - U_{max})) \quad (12)$$

Hence, by replacing "(11)" into "(12)" yields

$$dx/dt = -K_i K_S x + K_i(1 - K_S K_p)e + K_i K_S U_{max} \quad (13)$$

The solution of the above equation for a given error $e(t) = E$ Yields:

$$x(t) = (X_0 - (E/K_S) - U_{max} + K_p E).exp(-k_i k_s t) + ((E/K_S) + U_{max} - K_p e) \quad (14)$$

Replacing "(14)" in "(11)" yields

$$U(t) = (X_0 - (E/K_S) - U_{max} + K_p E).exp(-k_i k_s t) + ((E/K_S) + U_{max}) \quad (15)$$

It can be observed from the dynamic and steady-state relationships that the dynamic part goes to zero if the value of K_S has to be high and hence $U(t) \approx U_{max}$ and controller will come out of saturation quickly when the error input reverses.

C. *Self-Tuning Filter*

To obtain a satisfactory extraction, the dynamic regime is slow. In general, the cutoff frequency is chosen between 5 Hz and 35 Hz, which then generates instability of the active power filter during rapid changes in the load.

In the opposite case, if a higher cutoff frequency is chosen, the accuracy of the determination of the alternative component is impaired and may prove insufficient [18]. For these reasons, a new type of extraction filter named self-tuning filter (STF) has been developed as shown in Fig. 4.

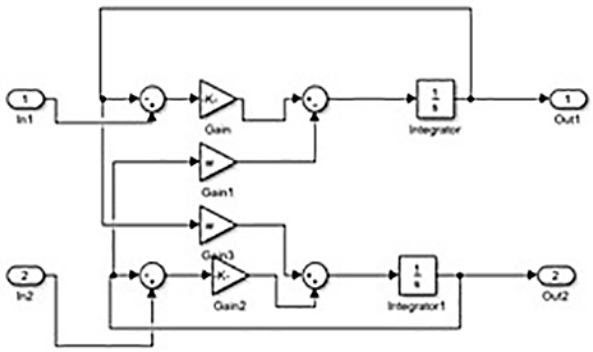

Fig. 4. Block diagram of STF

The transfer function of the STF is defined as:

$$H(s) = V_{xy}(s)/U_{xy}(s) = K\,.\,[(s + j\omega)/(s^2 + \omega^2)] \quad (16)$$

From the integral effect on the input magnitude, the STF does not alter the phase of the input, hence $U_{xy}(s)$ and $V_{xy}(s)$ have the same phase [19].

The three-phase references of source current are calculated as:

$$i_{ref(a)} = (i_{Ldc} + i_{ld})V_{au} \quad (17)$$

$$i_{ref(a)} = (i_{Ldc} + i_{ld})V_{au} \quad (18)$$

$$i_{ref(c)} = (i_{Ldc} + i_{ld})V_{cu} \quad (19)$$

The compensating current could be obtained by subtracting the load current from the reference supply current [20]. The generated currents pass through a Hysteresis Current Control HCC to obtain switching signals needed in semiconductors commutation of the VSC.

IV. Results and Discussions

A MATLAB/Simulink model of the control system is developed to verify the performance of the proposed technique. Three variable RL type nonlinear load groups' gives in Table I and different operating unbalance supply voltage in Table II.

Table I
Simulation Parameters

Parameter	value
Source voltage	100V
System frequency	50Hz
DC link Capacitance	1100 µF
Source inductance	1.3 mH
Source resistance	0.42 Ω
Coupling inductance	2m H
Coupling resistance	0.1 Ω
Load 1	8Ω , 3mH
Load 2	12Ω , 5 mH
Load 3	30Ω , 4 mH
K_p	0.1074
K_i	0.2055

Table II
Simulation Parameters

	0%	10%	20%	30%
Phase A	100 V	100V	100 V	100 V
Phase B	100 V	90 V	80 V	70 V
Phase C	100 V	110 V	120 V	130 V
THD%	1.115	1.286	1.711	2.411

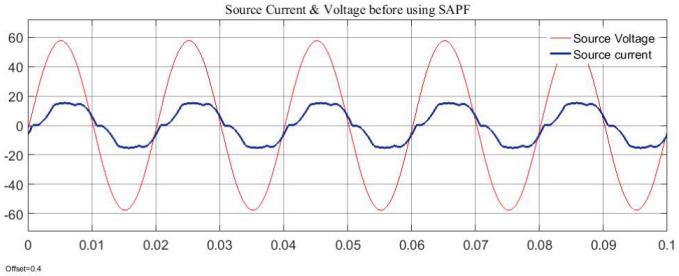

Fig. 5. The system before applying the SAPF (p hase A)

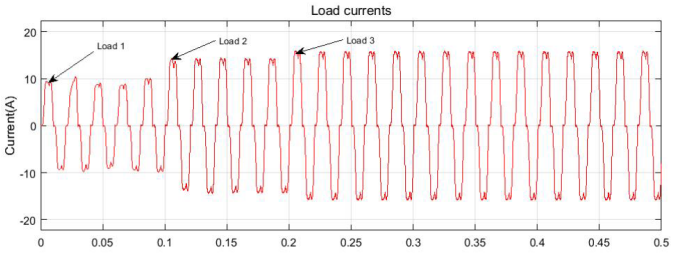

Fig. 6. The load currents

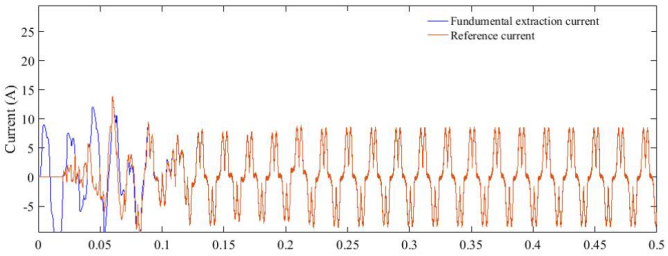

Fig. 7. The reference current followed by the fundamental after using SAPF

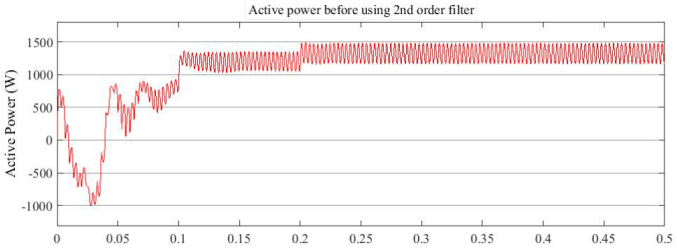

Fig. 8. The fundamental component of the active power of the three phases

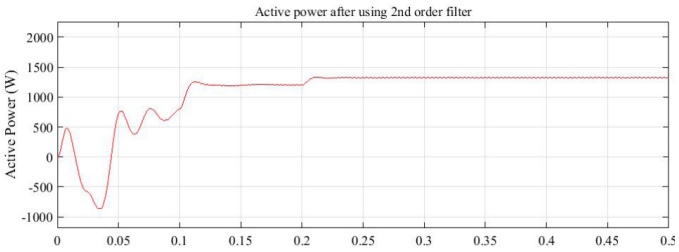

Fig. 9 The fundamental component of the active power of the three phases after using cascade 2nd order filters

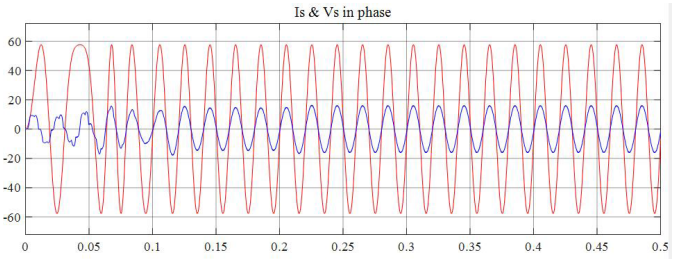

Fig. 10. The system after applying the SAPF (phase A)

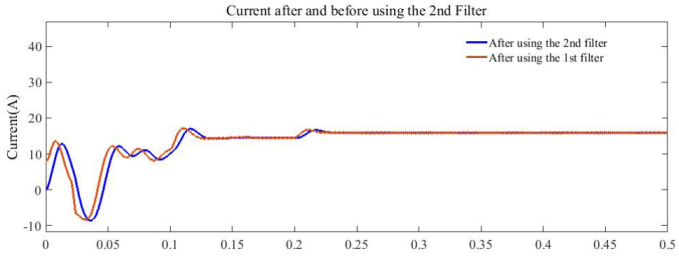

Fig. 11. The DC component of the fundamental current before and after using the 2nd order LPF. Stability of the fundamental current after introducing load2and load 3 at 0.1s, and after 0.2s respectively.

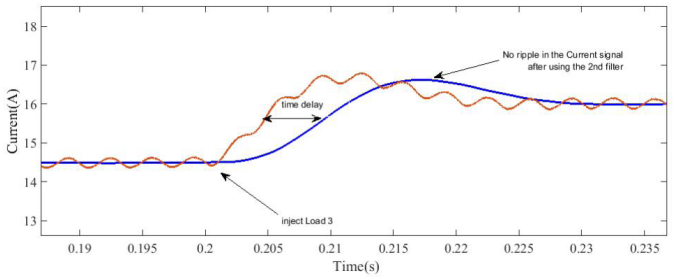

Fig. 12. Elimination of current signal ripple after using 2nd cascade filter

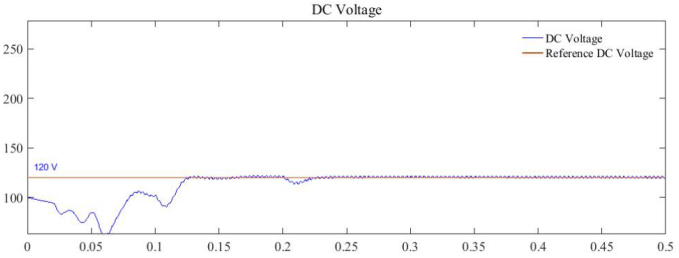

Fig. 13. The Voltage of the DC link side

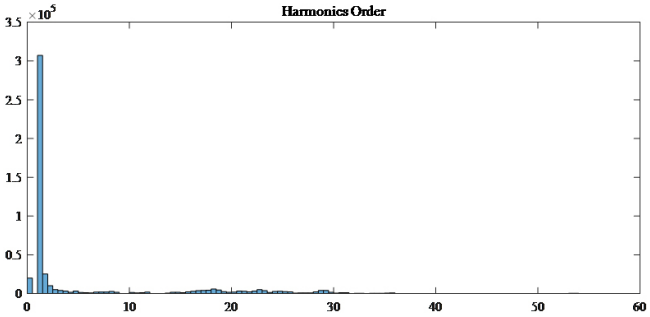

Fig. 14. Harmonic Order

TABLE III
COMPARAISON OF THE PERFORMANCE IN THE PROPOSED METHOD AGAINST OTHER DESIGN

Reference	Technical used	THD %
[10]	modified PLL structure	2.7
[11]	self-tuning filter	2.30
[12]	2nd order low pass filter wavelet-based multiresolution	2.08
[13]-[14]	Icosα	1.25
Presented work	PI controller with Tracking anti windup	1.115

A comparison of the achieved SAPF performance with respect to other realized with various designs for 3 phase unbalance non linear loads is summarized in Table III. It is clear that our proposed shows low percentage of THD even in the case of unbalanced grid voltage.

V. CONCLUSION

Simulation of three-phase three-wire shunt active power filter under unbalanced nonlinear loads and unbalanced grid voltage have been performed for improving power quality aspect at distribution system such as harmonic suppression. A modified Power Balance Theory technique based on PI controller with Anti windup integral action as a closed-loop regulator to eliminate the roll-over of the integrator and place it within a saturation region have been used to extract the fundamental component of the load current. A combination of a second-order low pass filter with Self Tuning Filter has been utilized for reference to current extraction. The result has shown that the proposed method has been found satisfactory in achieving harmonic reduction, compensation of reactive power and balancing in current supply. The study shows a good performance in terms of THD percentage which gives 1.115% in case of balanced grid voltage unbalanced three nonlinear loads integrated into the system in the different instant of time simulation as shown in Fig. 10 and also by using the proposed solution, the stability of the system on the DC link side is satisfactory. The simulation results from Table II, shows also the standard IEEE 519 is satisfied under 10%, 20%, 30% of unbalanced supply voltage [21].

REFERENCES

[1] Singh, B.; Al-Haddad, K.; Chandra, A. "A review of active filters for power quality improvement", *IEEE Trans. Industrial Electronics,* vol.46, no.5, 1999.

[2] K. Al-Haddad, Power Quality: Problems B. Singh, A. Chandra, *Problems and Mitigation Techniques*, John Wiley and Sons, U.K., 2015, pp. 48–89.

[3] P. Kanjiya, V. Khadkikar, and H. H. Zeineldin, "A non-iterative optimized algorithm for shunt active power filters under distorted and unbalanced supply voltages" *IEEE Trans. Industrial. Electronics,* vol. 60, no.12, pp.5376–5390, 2013.

[4] B. Singh, S. Arya, A. Chandra, and K. Al-Haddad, "Implementation of adaptive filter in distribution static compensator", *IEEE Transaction. Industrial Applications*, vol. 50, no. 5, pp. 3026–3036, 2014.

[5] De AraujoRibeiro, R.L.; De Oliveira Alves Rocha, T.; Maciel de Sousa, R.; dos Santos Junior, E.C.;Lima, A.M.N. "A robust DC-link voltage control strategy to enhance the performance of shunt active power filters without harmonic detection schemes". *IEEE Trans. Industrial. Electron*, vol.62, no. 3, pp. 803–813, 2015.

[6] M.Ramya, M .Sathyapriya, A. Benazir Hajira ,P.Kumar. "Mitigation of line current harmonics using shunt active filter with instantaneous real and reactive power theory", Journal of Electrical and Electronics Engineering. vol. 9, no.2, pp.59–67, Mar-Apr 2014.

[7] Joao Afonso, Mauricio Aredes, Edson Watanabe, J ulio Martins "Shunt active filter for power quality improvement", In *Proc. Conf.* UIE 2000 Electricity for a Sustainable Urban Development", Lisboa , Porugal, 2000, pp 683-691.

[8] K-L. Areerak and K-N. Areerak, "The comparison study of harmonic detection methods for shunt active power filters", *International Journal*

Of Electrical Computer Energetic Electronic and Communication Engineering vol. 4, no.10, 2010.

[9] Papan Dey, Saad Mekhilef "Current controllers of active power filter for power quality", *AUTOMATIKA* vol.56.no.1, pp.42-54, 2015.

[10] Kesler M, Ozdemir E. "Synchronous reference frame based control method for UPQC under unbalanced and distorted load conditions". *IEEE Transaction Industrial Electron,* vol.58, no.9, pp. 3967–3975, 2011.

[11] Biricik S, Ozerdem OC, Redif S, Kmail MOI. "Performance improvement of active power filters based on P-Q and D-Q control methods under non-ideal supply voltage conditions". In *Proc. Conf Electrical and Electronics Engineering ELECO IEEE*, Bursa, Turkey. New York, NY, USA, 2011, pp. 1312–1316.

[12] Isaac K, Emmanuel A.F A "2nd order LPF wavelet based control Scheme for shunt active power filter". In *Proc. Conf. IEEE PES-PowerAfrica,* Accra, Ghana, 2017, pp. 444–448.

[13] Ilango K ,Manitha P.V, Manjula G Nair "Modifieded *Icos* controller for shunt active filer interfacing renewable energy source and grid" In *Proc. Conf. American Applied Science Research Institute on Power and Energy Systems,* USA, 2012, pp. 62–68.

[14] Chrles. S , Member, IACSIT , G. Bhuvaneswari " Comparison of three phase shunt active power filter algorithms" *International journal of computers and Electrical Engineering*, vol. 2 no. 1, pp. 1793–8163, February, 2010.

[15] D. Vrancic. "Design of Anti-Windup and bumpless transfer protection", Ph.D. dissertation, Dept. Elect. Eng., Ljubljana Univ., Slovenia, 1997,

[16] Chennai Salim, Benchouia M-T, "Three – phase three wire shunt active power filter based on hysteresis, fuzzy and MLPNN controllers to compensate current harmonics" *Journal of electrical and control engineering American V-king Scientific Publishing*, vol. 3 no. 3, pp. 6–12, 2013.

[17] A. Visioli. "Modified anti-windup scheme for PID controllers", *IEE Control Theory and Applications, IET Publishing*, vol.150, no.1, pp. 49–54, January 2003.

[18] Mihai Ciobotaru, Remus Teodorescu and Frede Blaabjerg "A new single-phase PLL structure based on second order generalized integrator", In *Proc.37th Conf. IEEE, Power Electronics Specialists,* South Korea, 2006, pp. 453–459.

[19] A. Scott Edward Hodel and C. E. Hall. "Variable-structure PID controls to prevent integrator windup", *IEEE Transactions on Industrial Electronics*, vol.48 no.2, pp. 442–451, 2001.

[20] J. M. Espi, J. Castello, R. Garcia-Gil, G. Garcera, and E. Figueres, "An adaptive robust predictive current control for three-phase grid connected inverters," *IEEE Trans. Industrial Electronics*, vol. 58, no. 8, pp. 3537–3546, Aug. 2011.

[21] *IEEE Recommended Practices and requirement for Harmonic Control on electric power System*, IEEE Standard 519, 1992.

Preparation of Papers for Electronics (September 2011)

First A. Author, Second B. Author, and Third C. Author

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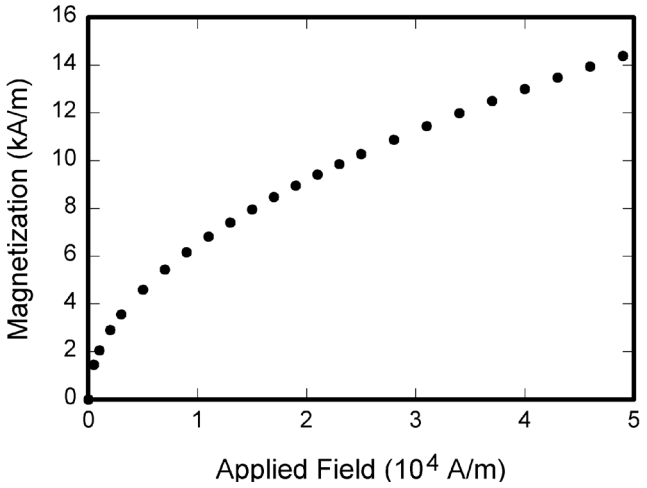

Fig. 1. Magnetization as a function of applied field. Note that "Fig." is abbreviated. There is a period after the figure number, followed by two spaces. It is good practice to explain the significance of the figure in the caption.

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The SI unit for magnetic field strength H is A/m. However, if you wish to use units of T, either refer to magnetic flux density B or magnetic field strength symbolized as $\mu_0 H$. Use the center dot to separate compound units, e.g., "A·m^2."

TABLE I
Units for Magnetic Properties

Symbol	Quantity	Conversion from Gaussian and CGS EMU to SI [a]
Φ	magnetic flux	1 Mx $\rightarrow 10^{-8}$ Wb = 10^{-8} V·s
B	magnetic flux density, magnetic induction	1 G $\rightarrow 10^{-4}$ T = 10^{-4} Wb/m^2
H	magnetic field strength	1 Oe $\rightarrow 10^3/(4\pi)$ A/m
m	magnetic moment	1 erg/G = 1 emu $\rightarrow 10^{-3}$ A·m^2 = 10^{-3} J/T
M	magnetization	1 erg/(G·cm^3) = 1 emu/cm^3 $\rightarrow 10^3$ A/m
$4\pi M$	magnetization	1 G $\rightarrow 10^3/(4\pi)$ A/m
σ	specific magnetization	1 erg/(G·g) = 1 emu/g $\rightarrow$ 1 A·m^2/kg
j	magnetic dipole moment	1 erg/G = 1 emu $\rightarrow 4\pi \times 10^{-10}$ Wb·m
J	magnetic polarization	1 erg/(G·cm^3) = 1 emu/cm^3 $\rightarrow 4\pi \times 10^{-4}$ T
χ, κ	susceptibility	1 $\rightarrow 4\pi$
χ_ρ	mass susceptibility	1 cm^3/g $\rightarrow 4\pi \times 10^{-3}$ m^3/kg
μ	permeability	1 $\rightarrow 4\pi \times 10^{-7}$ H/m = $4\pi \times 10^{-7}$ Wb/(A·m)
μ_r	relative permeability	$\mu \rightarrow \mu_r$
w, W	energy density	1 erg/cm^3 $\rightarrow 10^{-1}$ J/m^3
N, D	demagnetizing factor	1 $\rightarrow 1/(4\pi)$

Vertical lines are optional in tables. Statements that serve as captions for the entire table do not need footnote letters.

[a]Gaussian units are the same as cgs emu for magnetostatics; Mx = maxwell, G = gauss, Oe = oersted; Wb = weber, V = volt, s = second, T = tesla, m = meter, A = ampere, J = joule, kg = kilogram, H = henry.

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Multipliers can be especially confusing. Write "Magnetization (kA/m)" or "Magnetization (10^3 A/m)." Do not write "Magnetization (A/m) x 1000" because the reader would not know whether the top axis label in Fig. 1 meant 16000 A/m or 0.016 A/m. Figure labels should be legible, approximately 8 to 12 point type.

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Capitalize only the first word in a paper title, except for proper nouns and element symbols. For papers published in translation journals, please give the English citation first, followed by the original foreign-language citation [8]. All references **must be** written in Roman alphabet.

C. Abbreviations and Acronyms

Define abbreviations and acronyms the first time they are used in the text, even after they have already been defined in the abstract. Abbreviations such as IEEE, SI, ac, and dc do not have to be defined. Abbreviations that incorporate periods should not have spaces: write "C.N.R.S.," not "C. N. R. S." Do not use abbreviations in the title unless they are unavoidable (for example, "IEEE" in the title of this article).

D. Equations

Number equations consecutively with equation numbers in parentheses flush with the right margin, as in (1). First use the equation editor to create the equation. Then select the "Equation" markup style. Press the tab key and write the equation number in parentheses. To make your equations more compact, you may use the solidus (/), the exp function, or appropriate exponents. Use parentheses to avoid ambiguities in denominators. Punctuate equations when they are part of a sentence, as in

$$\int_0^{r_2} F(r,\varphi)\,\mathbf{d}\,d\varphi = [\sigma r_2/(2\mu_0)] \cdot \int_0^{\infty} \exp(-\lambda\,|z_j - z_i|)\,\lambda^{-1} J_1(\lambda r_2)\,J_0(\lambda r_i)\,d\lambda\,. \tag{1}$$

Be sure that the symbols in your equation have been defined before the equation appears or immediately following. Italicize symbols (*T* might refer to temperature, but T is the unit tesla). Refer to "(1)," not "Eq. (1)" or "equation (1)," except at the beginning of a sentence: "Equation (1) is ... ."

E. Other Recommendations

Use one space after periods and colons. Hyphenate complex modifiers: "zero-field-cooled magnetization." Avoid dangling participles, such as, "Using (1), the potential was calculated." [It is not clear who or what used (1).] Write instead, "The potential was calculated by using (1)," or "Using (1), we calculated the potential."

Use a zero before decimal points: "0.25," not ".25." Use "cm^3," not "cc." Indicate sample dimensions as "0.1 cm x 0.2 cm," not "0.1 x 0.2 cm^2." The abbreviation for "seconds" is "s," not "sec." Do not mix complete spellings and abbreviations of units: use "Wb/m^2" or "webers per square meter," not "webers/m^2." When expressing a range of values, write "7 to 9" or "7-9," not "7~9."

A parenthetical statement at the end of a sentence is punctuated outside of the closing parenthesis (like this). (A parenthetical sentence is punctuated within the parentheses.) In American English, periods and commas are within quotation marks, like "this period." Other punctuation is "outside"! Avoid contractions; for example, write "do not" instead of "don't." The serial comma is preferred: "A, B, and C" instead of "A, B and C."

If you wish, you may write in the first person singular or plural and use the active voice ("I observed that ..." or "We observed that ..." instead of "It was observed that ..."). Remember to check spelling. If your native language is not English, please get a native English-speaking colleague to carefully proofread your paper.

[1] It is recommended that footnotes be avoided (except for the unnumbered footnote with the receipt date and authors' affiliations on the first page). Instead, try to integrate the footnote information into the text.

VI. Some Common Mistakes

The word "data" is plural, not singular. The subscript for the permeability of vacuum μ_0 is zero, not a lowercase letter "o." The term for residual magnetization is "remanence"; the adjective is "remanent"; do not write "remnance" or "remnant." Use the word "micrometer" instead of "micron." A graph within a graph is an "inset," not an "insert." The word "alternatively" is preferred to the word "alternately" (unless you really mean something that alternates). Use the word "whereas" instead of "while" (unless you are referring to simultaneous events). Do not use the word "essentially" to mean "approximately" or "effectively." Do not use the word "issue" as a euphemism for "problem." When compositions are not specified, separate chemical symbols by en-dashes; for example, "NiMn" indicates the intermetallic compound $Ni_{0.5}Mn_{0.5}$ whereas "Ni–Mn" indicates an alloy of some composition Ni_xMn_{1-x}.

Be aware of the different meanings of the homophones "affect" (usually a verb) and "effect" (usually a noun), "complement" and "compliment," "discreet" and "discrete," "principal" (e.g., "principal investigator") and "principle" (e.g., "principle of measurement"). Do not confuse "imply" and "infer."

Prefixes such as "non," "sub," "micro," "multi," and "ultra" are not independent words; they should be joined to the words they modify, usually without a hyphen. There is no period after the "et" in the Latin abbreviation "*et al.*" (it is also italicized). The abbreviation "i.e.," means "that is," and the abbreviation "e.g.," means "for example" (these abbreviations are not italicized).

An excellent style manual and source of information for science writers is [9].

VII. Editorial Policy

Each manuscript submitted is subjected to the following review procedure:

- It is reviewed by the editor for general suitability for this publication
- If it is judged suitable, two reviewers are selected and a single-blinded review process takes place
- Based on the recommendations of the reviewers, the editor then decides whether the particular paper should be accepted as is, revised or rejected.

Do not submit a paper you have submitted or published elsewhere. Do not publish "preliminary" data or results. The submitting author is responsible for obtaining agreement of all coauthors and any consent required from sponsors before submitting a paper. It is the obligation of the authors to cite relevant prior work.

Every paper submitted to "Electronics" journal are single-blind reviewed. For conference-related papers, the decision to accept or reject a paper is made by the conference editors and publications committee; the recommendations of the referees are advisory only. Undecipherable English is a valid reason for rejection.

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The contents of "Electronics" are peer-reviewed and archival. The "Electronics" publishes scholarly articles of archival value as well as tutorial expositions and critical reviews of classical subjects and topics of current interest.

Authors should consider the following points:

1) Technical papers submitted for publication must advance the state of knowledge and must cite relevant prior work.
2) The length of a submitted paper should be commensurate with the importance, or appropriate to the complexity, of the work. For example, an obvious extension of previously published work might not be appropriate for publication or might be adequately treated in just a few pages.
3) Authors must convince both peer reviewers and the editors of the scientific and technical merit of a paper; the standards of proof are higher when extraordinary or unexpected results are reported.
4) Because replication is required for scientific progress, papers submitted for publication must provide sufficient information to allow readers to perform similar experiments or calculations and use the reported results. Although not everything need be disclosed, a paper must contain new, useable, and fully described information. For example, a specimen's chemical composition need not be reported if the main purpose of a paper is to introduce a new measurement technique. Authors should expect to be challenged by reviewers if the results are not supported by adequate data and critical details.
5) Papers that describe ongoing work or announce the latest technical achievement, which are suitable for presentation at a professional conference, may not be appropriate for publication in "Electronics".

IX. Conclusion

A conclusion section is not required. Although a conclusion may review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions.

Appendix

Appendixes, if needed, appear before the acknowledgment.

Acknowledgment

The preferred spelling of the word "acknowledgment" in American English is without an "e" after the "g." Use the singular heading even if you have many acknowledgments. Avoid expressions such as "One of us (S.B.A.) would like to thank ... ." Instead, write "F. A. Author thanks ... ." **Sponsor and financial support acknowledgments are placed in the unnumbered footnote on the first page, not here.**

References

[1] G. O. Young, "Synthetic structure of industrial plastics (Book style with paper title and editor)," in *Plastics*, 2nd ed. vol. 3, J. Peters, Ed. New York: McGraw-Hill, 1964, pp. 15–64.

[2] W.-K. Chen, *Linear Networks and Systems* (Book style). Belmont, CA: Wadsworth, 1993, pp. 123–135.

[3] H. Poor, *An Introduction to Signal Detection and Estimation*. New York: Springer-Verlag, 1985, ch. 4.

[4] B. Smith, "An approach to graphs of linear forms (Unpublished work style)," unpublished.

[5] E. H. Miller, "A note on reflector arrays (Periodical style—Accepted for publication)," *IEEE Trans. Antennas Propagat.*, to be published.

[6] J. Wang, "Fundamentals of erbium-doped fiber amplifiers arrays (Periodical style—Submitted for publication)," *IEEE J. Quantum Electron.*, submitted for publication.

[7] C. J. Kaufman, Rocky Mountain Research Lab., Boulder, CO, private communication, May 1995.

[8] Y. Yorozu, M. Hirano, K. Oka, and Y. Tagawa, "Electron spectroscopy studies on magneto-optical media and plastic substrate interfaces (Translation Journals style)," *IEEE Transl. J. Magn.Jpn.*, vol. 2, Aug. 1987, pp. 740–741 [*Dig. 9th Annu. Conf. Magnetics* Japan, 1982, p. 301].

[9] M. Young, *The Techincal Writers Handbook.* Mill Valley, CA: University Science, 1989.

[10] J. U. Duncombe, "Infrared navigation—Part I: An assessment of feasibility (Periodical style)," *IEEE Trans. Electron Devices*, vol. ED-11, pp. 34–39, Jan. 1959.

[11] S. Chen, B. Mulgrew, and P. M. Grant, "A clustering technique for digital communications channel equalization using radial basis function networks," *IEEE Trans. Neural Networks*, vol. 4, pp. 570–578, Jul. 1993.

[12] R. W. Lucky, "Automatic equalization for digital communication," *Bell Syst. Tech. J.*, vol. 44, no. 4, pp. 547–588, Apr. 1965.

[13] S. P. Bingulac, "On the compatibility of adaptive controllers (Published Conference Proceedings style)," in *Proc. 4th Annu. Allerton Conf. Circuits and Systems Theory*, New York, 1994, pp. 8–16.

[14] G. R. Faulhaber, "Design of service systems with priority reservation," in *Conf. Rec. 1995 IEEE Int. Conf. Communications,* pp. 3–8.

[15] W. D. Doyle, "Magnetization reversal in films with biaxial anisotropy," in *1987 Proc. INTERMAG Conf.*, pp. 2.2-1–2.2-6.

[16] G. W. Juette and L. E. Zeffanella, "Radio noise currents n short sections on bundle conductors (Presented Conference Paper style)," presented at the IEEE Summer power Meeting, Dallas, TX, Jun. 22–27, 1990, Paper 90 SM 690-0 PWRS.

[17] J. G. Kreifeldt, "An analysis of surface-detected EMG as an amplitude-modulated noise," presented at the 1989 Int. Conf. Medicine and Biological Engineering, Chicago, IL.

[18] J. Williams, "Narrow-band analyzer (Thesis or Dissertation style)," Ph.D. dissertation, Dept. Elect. Eng., Harvard Univ., Cambridge, MA, 1993.

[19] N. Kawasaki, "Parametric study of thermal and chemical nonequilibrium nozzle flow," M.S. thesis, Dept. Electron. Eng., Osaka Univ., Osaka, Japan, 1993.

[20] J. P. Wilkinson, "Nonlinear resonant circuit devices (Patent style)," U.S. Patent 3 624 12, July 16, 1990.

[21] IEEE Criteria for Class IE Electric Systems (Standards style), IEEE Standard 308, 1969.

[22] Letter Symbols for Quantities, ANSI Standard Y10.5-1968.

[23] R. E. Haskell and C. T. Case, "Transient signal propagation in lossless isotropic plasmas (Report style)," USAF Cambridge Res. Lab., Cambridge, MA Rep. ARCRL-66-234 (II), 1994, vol. 2.

[24] E. E. Reber, R. L. Michell, and C. J. Carter, "Oxygen absorption in the Earth's atmosphere," Aerospace Corp., Los Angeles, CA, Tech. Rep. TR-0200 (420-46)-3, Nov. 1988.

[25] (Handbook style) *Transmission Systems for Communications,* 3rd ed., Western Electric Co., Winston-Salem, NC, 1985, pp. 44–60.

[26] *Motorola Semiconductor Data Manual,* Motorola Semiconductor Products Inc., Phoenix, AZ, 1989.

[27] (Basic Book/Monograph Online Sources) J. K. Author. (year, month, day). *Title* (edition) [Type of medium]. Volume (issue). Available: http://www.(URL)

[28] J. Jones. (1991, May 10). Networks (2nd ed.) [Online]. Available: http://www.atm.com

[29] (Journal Online Sources style) K. Author. (year, month). Title. *Journal* [Type of medium]. Volume(issue), paging if given. Available: http://www.(URL)

[30] R. J. Vidmar. (1992, August). On the use of atmospheric plasmas as electromagnetic reflectors. *IEEE Trans. Plasma Sci.* [Online]. *21(3).* pp. 876–880. Available: http://www.halcyon.com/pub/journals/21ps03-vidmar

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