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UNIVERSITY OF BANJA LUKA

Address: Patre 5, 78000 Banja Luka, Bosnia and Herzegovina
Phone: +387 51 211824
Fax: +387 51 211408
Web: www.etf.unibl.org

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Editor's Column

Mladen Knezic

> The best time to plant a tree was 20 years ago. The second best time is now.
>
> *Chinese Proverb*

Editorial Letter
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THE second issue of *Electronics* journal in December 2020 brings new research in the fields of image processing and integrated circuit design but also many challenges caused by the COVID-19 pandemic that affected all the aspects of our lives globally. Unfortunately, COVID-19 also brought away our friend and renowned member of the Editorial Board of the journal "Electronics", prof. Ninoslav Stojadinović who passed away on 25 December 2020. In honor to this great scientist, educator, and influential leader, our founder and honorary Editor-in-Chief, prof. Branko Dokić, accepted to pass to our knowledge at least a tiny part of prof. Stojadinović's rich and fruitful professional life within "In Memoriam" section.

In this issue we have three original research papers.

The first paper "A Novel Unsupervised Approach for Land Classification Based on Touzi Scattering Vector Model in the Context of Very High Resolution PolSAR Imagery," authored by J. Gong, Sheng Sun, and Z. Xu, describes a novel classifying algorithm based on Touzi scattering vector model by means of integrating Touzi decomposition with conventional Wishart statistical models. The experimental results proved proposed method to be superior to classical method in terms of producer, user and overall accuracy.

The paper "A Full Adder Design with CNFETs for Real Time, Fault Tolerant and Mission Critical Applications," by J. K. Saini, A. Srinivasulu, and R Kumawat, presents a full adder design with CNFETs that provides high fault resistance towards transient and permanent faults. Moreover, the proposed design enables operation with least power, delay and power-delay product (PDP). Finally, the authors simulated the design at 32 nm technology with 0.9V supply voltage using the Cadence Virtuoso CAD tool.

Finally, the paper "Sensitivity Analysis of the UTBSOI Transistor based Two-Stage Operational Amplifier," by R. U. Ahmed, E. A. Vijaykumar, and P. Saha provides a sensitivity analysis procedure for the CMOS and UTBSOI based two-stage operational amplifiers (OPAMPs) as a function of perturbation in W/L. To this end, the authors proposed an algorithm for computing sensitivity and conducted simulations for a number of scenarios. The results shown that the sensitivity of the UTBSOI based OPAMP is larger than in the case of CMOS based OPAMP.

I thank the authors for their contribution to this issue of the journal and to all the reviewers who participated in the editorial process by providing valuable comments in timely manner to the editors and the authors.

In Memoriam – Prof. Ninoslav Stojadinović

Branko Dokic
Founder and Honorary Editor-in-Chief

DOI: 10.7251/ELS2024055D

ON December 25, 2020, our friend, renowned scientist, educator, world renowned expert, and member of the Editorial Board of journal "Electronics",

Ninoslav Stojadinović

(20.09.1950–25.12.2020) lost the battle for his life against Covid-19.

Ninoslav Stojadinović was a full member of Serbian Academy of Sciences and Arts (SASA), a full member of Academy of Engineering Sciences of Serbia (AESS), a full professor of the Faculty of Electronics, University of Niš, Serbia and its former dean, a fellow of IEEE Society and a fellow of ETRAN Society. An influential and cited scientist, he achieved a number of exceptional results in the field of microelectronics and nanoelectronics. His research included both fundamental and applied science, and a number of his innovative results have been in semiconductor industry in Serbia (EI) and worldwide. He was elected the first president of the Branch of SASA in Niš in 2016 and organized more than 250 events related to it. Prof. Stojadinović has won several important awards and recognitions for his dedicated work.

He led several international science journals, including Elsevier's Microelectronics Journal (Editor-in-Chief 1993–1995); Elsevier's Microelectronics Reliability, (Editor-in-Chief, 1996–2017); IEEE EDS Newsletter, (Editor-in-Chief, 2002–2012); J. Semiconductor Technology and Science (since 2001); Nanoscience & Nanotechnology-ASIA (since 2011) and Facta Universitatis, Series: Electronics and Energetics (Editor-in-Chief). For three decades he was the chair of the Conference on Microelectronics – MIEL, and under his leadership it developed into the leading scientific conference in this part of Europe and was on the list of IEEE conferences. He was also a member of Scientific and/or Programme Committees of more than 50 international and numerous national scientific meetings. He was Chair of the Society for ETRAN in the period 2001–2006.

He was a visiting professor at the Technical University of Vienna, a member of the international scientific committee

of the Center for Nanotechnology with Clemson University, USA, and of the EU Center of Excellence for Micro and Nanotechnology Research with the Technical University of Warsaw, Poland. He was also one of the members of the Expert Commission for EU framework programs and a consultant to the Science Foundation of the Government of Taiwan.

Academician Stojadinović had significant political and diplomatic activities. He was a member of the National Assembly of the Republic of Serbia (1997–2000), a member of the Assembly of the State Union of Serbia and Montenegro and its representative in the Parliamentary Assembly of the Council of Europe (2004–2006). He was the Vice President of the National Assembly of the Republic of Serbia (2014–2016). He was the Ambassador of the Republic of Serbia to the Kingdom of Sweden (2005-2011) and to Bosnia and Herzegovina (2011–2013).

On December 25, 2020 prof. Stojadinović lost his battle against COVID-19. His demise is a great loss for SASA, AESS, IEEE, the ETRAN Society , as well as for microelectronics science in general, but undeniably the greatest loss for his family – his wife Andjelka and his son Dragan.

A Novel Unsupervised Approach for Land Classification Based on Touzi Scattering Vector Model in the Context of Very High Resolution PolSAR Imagery

Jian Gong, Sheng Sun, and Zhijia Xu

***Abstract*—With the popularization of very high resolution polarimetric synthetic aperture radar image dataset, it is essential to re-investigate the classification scheme for 2-D land cases. The Touzi scattering vector model, a unique and roll-invariant decomposition solution, is employed to extract the scattering properties of different land covers. The parameters of Touzi decomposition act as input dataset for initial classification. A novel classifying algorithm is put forward by means of integrating the Touzi decomposition with conventional Wishart statistical models. Quantitative experiments are then conducted using uninhabited aerial vehicle synthetic aperture radar sample data for evaluating the performance of this new proposed approach. It can be concluded from the experimental results that the new proposed method is superior to the classical method in terms of producer accuracy, user accuracy, and overall accuracy.**

***Index Terms*—Polarimetric synthetic aperture radar, scattering vector model, Touzi decomposition, unsupervised classification, very high resolution**

Original Research Paper
DOI: 10.7251/ELS2024057G

I. Introduction

LAND classification applications based on the polarimetric synthetic aperture radar (PolSAR) remain hotspots in the community of radar remote sensing over the past few decades. Classification methods play a prominent role in these applications. In general, these methods can be categorized into three groups: algorithms based on statistical models, algorithms based on physical scattering mechanisms, and the ones that combine both of them. The third group, on the whole, excels at this task owing to the combination of statistical and physical scattering characteristics [1]. For one thing, the manner in which physical scattering properties are extracted is of great importance to the classification of polarimetric synthetic aperture radar images. There were various academic explorations to deal with this problem in recent years. Kusano *et al.* in 2015 proposed a generalized scattering model based on the particle cloud model adding the ellipticity angle. Their experimental results showed that the decomposition parameters were considerably dissimilar from those of eigenvalue-based methods [2]. Besic *et al.* in 2015 put forward an alternative approach for polarimetric incoherent target decomposition (ICTD) that was dedicated to the analysis of very high resolution (VHR) polarimetric synthetic aperture radar images. They argued that this ICTD decomposition strategy was capable of retrieving the edge diffraction of an elementary trihedral by recognizing dipole as the second component [3]. Bhattacharya *et al.* in 2015 suggested an adaptive general four-component scattering power decomposition method that was an extension of the best-known Yamaguchi four-component decomposition [4]-[5]. Touzi *et al.* came up with a solution that was inspired from the Cloude-Pottier ICTD in 2016 [6]-[7]. They employed Kennaugh-Huynen scattering matrix con-diagonalization and derived a new scattering vector model (SVM). The symmetric scattering type (SST) was brought in by them for an unambiguous description of symmetric target scattering. Due to the limited space, it is unachievable to review all the related methods here. For another, researchers seek to apply these newly-developed polarimetric property extractors and statistical methods to land classification. Trisasongko presented an evaluation on strategies for rubber plantation mapping employing PolSAR data coupled with random forest and support vector machine in 2017. He showed that classification accuracy could be further augmented by integrating texture features [8]. Sonobe *et al.* conducted a classifying experiment using Sentinel-1A C-SAR images and the Sentinel-2A image acquired during the 2016 growing season. They demonstrated an overall classification accuracy of 96.8% by means of kernel-based extreme learning machine [9]. Middinti *et al.* argued that the integration of polarimetric information with textures could supply complimentary information in forest type discrimination and produce high accuracy map [10]. Ohki *et al.* accomplished a large-area land classification over entire Japan using PALSAR-2 data. They implemented an algorithm based on support vector

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Jian GONG is with the Guangzhou Railway Polytechnic, 100 Qinglong Middle Rd, Baiyun, Guangzhou, Guangdong Province, 510430, China. (e-mail: 33668933@qq.com).

Sheng SUN is with the Guangdong University of Technology, No. 100 Waihuan Xi Road, Guangzhou Higher Education Mega Center, Panyu District, Guangzhou, Guangdong Province, 510006, China. (phone: +86-20-39322279; fax: +86-20-39322279; e-mail: sunsheng@gdut.edu.cn).

Zhijia XU is with the Guiyang University, 103 Jianlongdong Rd, Nanming District, Guiyang, Guizhou, 550005, China. (e-mail: xzjbelinda@163.com).

machine. Their experiments involved full polarimetry (FP), compact polarimetry (CP), and dual polarimetry (DP) data. The maximum accuracy of 73.4% was attained with 15 full polarimetric features [11]. Buono *et al*. developed two unsupervised classification algorithms on the basis of Wishart models by integrating Freeman-Durden and Cloude-Pottier decomposition methods. They conducted a quantitative comparison between two classifying schemes using a fully polarimetric C-band dataset acquired by Radarsat-2 over the test site, the Yellow River Delta of China [12]. Khosravi *et al*. put forward two improved decision tree ensembles that were named balanced filter-based forest (BFF) and cost-sensitive filter-based forest (CFF). These tree ensembles were reported to be able to deal with imbalanced data problems. The performances of such two tree ensembles were evaluated using three airborne L-band PolSAR datasets acquired by AIRSAR, EMISAR, and UAVSAR [13]. Li and Zhang came up with a unified Huynen dichotomy by extending Huynen decomposition. This new algorithm provided a unified selection mechanism. Additionally, they presented a classification method based on scattering degree of preference. They evaluated this new classifier on the classic San Francisco Bay sample data provided by AIRSAR [14].

Still, it is worthwhile to start an exploration of classification techniques based on the state-of-the-art polarimetric extractors in the context of very high resolution PolSAR images. Studies on the data of the very high resolution synthetic aperture radar systems, such as F-SAR [15] and Uninhabited Aerial Vehicle Synthetic Aperture Radar (UAVSAR) [16], are booming recently. The imagery data with very high resolution generally has large dimension and is in single, dual, and full polarization configurations. The spatial resolution of these systems is often decimeter level and the dimension is on the order of ten to twenty thousand by ten to twenty thousand pixels [17]. The size of the resolution cell with reference to these very high resolution data is close to the radar wavelength. One fundamental presumption, for the fully developed speckle, is that the resolution cell is much larger than the radar wavelength. This presumption will become ineffective, because the diameter of the resolution cell is only about six to ten times larger than radar wavelength [17]. Hence, it is necessary to re-validate those classical statistical models for PolSAR data. Meanwhile, it is also essential to re-design and re-evaluate the algorithms for land classification using very high resolution PolSAR images.

In this paper, the Touzi scattering vector model is combined with statistical properties of SAR data. An unsupervised land classification scheme is implemented and applied to very high resolution PolSAR images. The experiment accomplished for land classification is one of the exploratory works on PolSAR images with decimeter-level resolution. The rest of this paper is organized as follows. An analysis for incoherent decomposition models for PolSAR will be put forth in Section II in the first place. Afterwards, we will describe the new proposed classification scheme based on Touzi incoherent decomposition model in Section III. A quantitative experiment using very high resolution PolSAR data will be conducted in Section IV. A brief summary will be drawn in the last section.

II. Analysis of Decomposition Models for PolSAR

A. Data for describing scattering medium

Most man-made and natural scatterers fall into two categories: deterministic scatterers and distributed scatterers. The former may be associated with a dominant and stable scattering phenomenon. Coherent target decompositions could be applied to the scattering matrix of imaging data and employed to characterize such sort of deterministic scattering targets, for extracting physical scattering properties. The latter corresponds to a medium that varies over time and is not stable or fixed. The radar scattering response of distributed scatterers consists of diverse scattering mechanisms. It is therefore only possible to extract the average physical scattering mechanism of these targets. Moreover, they will be affected by speckle to different degrees. These fluctuating targets can be described by the second order moment statistics of imaging data, such as coherency matrix or covariance matrix. The expression of scatter matrix S and coherency matrix T_3 are presented in equation (1) and (2) respectively. In the mono-static backscattering case, the scattering matrix is defined in terms of complex scattering coefficients of the observed medium. Its form can be cast in a local Cartesian basis for convenience. If the roles of the transmitting and receiving antennas are interchangeable, the reciprocity theorem goes into effect and then S_{XY} is equal to S_{YX}. The coherency matrix T_3 can be generated from the outer product of the target vector that is denoted by $\underline{k}$. The superscript T^* stands for conjugate transpose, while the operator <…> stands for temporal or spatial ensemble averaging in equation (2) [18].

$$S = \begin{bmatrix} S_{XX} & S_{XY} \\ S_{YX} & S_{YY} \end{bmatrix}, \underline{k} = \frac{1}{\sqrt{2}} \begin{bmatrix} S_{XX} + S_{YY} \\ S_{XX} - S_{YY} \\ 2S_{XY} \end{bmatrix} \tag{1}$$

$$T_3 = < kk^{T^*} > = \left\langle \begin{bmatrix} |k_1|^2 & k_1 k_2^* & k_1 k_3^* \\ k_2 k_1^* & |k_2|^2 & k_2 k_3^* \\ k_3 k_1^* & k_3 k_2^* & |k_3|^2 \end{bmatrix} \right\rangle = \left\langle \begin{bmatrix} T_{11} & T_{12} & T_{13} \\ T_{12}^* & T_{22} & T_{23} \\ T_{13}^* & T_{23}^* & T_{33} \end{bmatrix} \right\rangle \tag{2}$$

B. Decomposition Models for extracting polarimetric scattering properties

The purpose of target decomposition is to extract underneath scattering mechanisms as the sum of diverse pure scattering processes. Coherent target decomposition aims to express the measured scattering matrix S as a combination of a string of canonical scattering mechanisms. It is only suitable for deterministic targets. Incoherent target decomposition seeks to obtain the average scattering mechanism in each resolution cell and can merely be applied to distributed targets that are expressed in terms of coherency matrix or covariance matrix. Due to the limited space, it is impossible to review all the decomposition methods here. We will, in this paper, concentrate on Touzi scattering vector model which springs from Cloude-Pottier incoherent target decomposition. Cloude-Pottier incoherent target decomposition presented, to a certain extent, ambiguities of scattering

type parameter for some scatterers [7]. An example, listed in [7], showed that a helix scatterer and dihedral scatterer had identical Cloude-Pottier α scattering type parameter ($\alpha=\pi/2$). For this reason, these two distinct scatterers can not be distinguished by such a parameter. Touzi scattering vector model was put forth with the goal of solving such ambiguities [7].

Firstly, Touzi scattering vector model is derived by adopting a projection of the Kennaugh-Huynen scattering matrix con-diagonalization into the Pauli basis. This projection allows eliminating the aforementioned ambiguities. The Touzi scattering vector model is composed of one complex entity called symmetric scattering type (SST). This complex variable consists of symmetric scattering type magnitude α_s and phase $\phi_{\alpha s}$ which are defined in polar coordinates. The former one ranges from 0 to $\pi/2$ and the latter one ranges from $-\pi/2$ to $\pi/2$. These two parameters are defined as a function of the scattering matrix con-eigenvalues μ_1 and μ_2 in equation (3) [7]. Besides, the scattering vector model for symmetric and asymmetric targets is denoted as equation (4). m is the maximum amplitude return. φ is the orientation of the maximum polarization with respect to the horizontal polarization. τ_m and ψ correspond to the helicity and the absolute phase respectively.

$$\tan(\alpha_s)e^{j\phi_{\alpha s}} = \frac{\mu_1 - \mu_2}{\mu_1 + \mu_2} \tag{3}$$

$$\underline{e}^{SV} = m \mid \underline{e} \mid \exp(j\psi) \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos 2\varphi & -\sin 2\varphi \\ 0 & \sin 2\varphi & \cos 2\varphi \end{bmatrix} \begin{bmatrix} \cos\alpha_S \cos 2\tau_m \\ \sin\alpha_S \exp(j\phi_{\alpha S}) \\ -j\cos\alpha_S \sin 2\tau_m \end{bmatrix} \tag{4}$$

Secondly, it is required to extend the scattering vector model mentioned above on account of the fact that it can only be effective for deterministic targets. This extension can be implemented by means of the following three steps.

(1) Figure out the coherency matrix T_3 through a simple spatial averaging within a square window.

(2) Perform a diagonalization of coherency matrix T_3. The corresponding three eigenvectors u_i (i=1, 2, 3) and eigenvalues λ_i (i=1, 2, 3) will be obtained.

(3) Carry out the parametrization of three eigenvectors u_i (i=1, 2, 3) according to the scattering vector model in equation (4). Each eigenvector can be characterized in terms of scattering vector model basis-invariant parameters as equation (4). A process for extracting the average scattering mechanisms can be put into effect in the similar manner that Cloude-Pottier has utilized in [19]. The average scattering parameters can be obtained by applying an arithmetic mean to these eigenvectors and eigenvalues afterwards.

Lastly, the above extended scattering vector model is qualified to extract the physical scattering properties for both deterministic targets and distributed targets. It is notable that only symmetric scattering type magnitude α_s and phase $\phi_{\alpha s}$ are adequate to meet the demand for classifying a 2-D land. As a result, other parameters will be omitted in the following sections.

III. Classification algorithm based on Touzi Scattering Model

A. Statistical model for very high resolution PolSAR data

As far as very high resolution data is concerned, the size of the resolution cell is close to the radar wavelength. Many conventional statistical models are based on a fundamental assumption that the resolution cell is much larger than the radar wavelength. The diameter of the resolution cell of very high resolution PolSAR data is generally about six to ten times larger than radar wavelength. Such assumption may, therefore, become invalid with reference to most very high resolution PolSAR datasets, such as F-SAR and UAVSAR. The amplitudes of four fully polarimetric channels were investigated and their histograms were computed and shown in [20]. A tight fit of the Rayleigh distributions to these histograms can easily be observed. Furthermore, it can be concluded that Wishart distribution will still be correct for those very high resolution datasets [20]. For this reason, the statistical models based on Wishart probability distributions continue to be effective for classification scheme using very high resolution PolSAR datasets.

The distributions of n-look coherency matrix Z, defined in eqination (5), will be utilized here to extract physical scattering mechanisms using Touzi incoherent decomposition. For convenience, let $A=nZ$, then the matrix A follows a complex Wishart distribution. The matrix A is defined in eqination (6).

$$Z = \frac{1}{n}\sum_{i=1}^{n} \underline{k}(i)\underline{k}(i)^{T^*} \tag{5}$$

$$P_A^{(n)}(A) = \frac{|A|^{n-q}\exp(-Tr(T^{-1}A))}{K(n,q)|T|^n} \tag{6}$$

$$K(n,q) = \pi^{0.5q(q-1)}\Gamma(n),...,\Gamma(n-q+1)$$

The conventional Wishart distance, defined in equation (7), characterizes the distance between a pixel and a class. Such distance is essential to calculate the statistical distance for pixels. Let T_m denote the coherency matrix of a certain class center. It can be approximated by the averaging of all the training samples. Each pixel is labeled with a class code if its Wishart distance to this class is the minimum among all classes. In addition, it is requisite to bring up the distance between classes to split or merge classes. The so-called distance between class with label i and the one with label j is presented in equation (8).

$$d(Z,\omega_m) = \ln(|T_m|) + Tr(T_m^{-1}Z) \tag{7}$$

$$D_{ij} = \frac{1}{2}\{\ln(|T_i|) + \ln(|T_j|) + Tr(T_i^{-1}T_j + T_j^{-1}T_i)\} \tag{8}$$

B. Classification algorithm

In light of the analysis in Section II, Touzi incoherent target decomposition model is competent to extract physical scattering mechanisms unambiguously. For example, the symmetric scattering type phase $\phi_{\alpha s}$ has been proven to be effective for Convair-580 airborne dataset which has a resolution of 0.64 meter in azimuth and 5.6 meter in range direction [21]. This parameter could easily be used to produce a set of coarse classifying results. And an unsupervised classification scheme based on these coarse results is supposed to be convincing if it can be incorporated with conventional statistical assumptions. The core parameters of Touzi incoherent decomposition are the magnitude and phase of symmetric scattering type. These two parameters can collectively be used for describing symmetric and asymmetric targets. Moreover, they are not dependent on polarization basis of radar antennas because they are derived from eigenvalues that are polarimetric basis invariant. At last, they play a role similar to Cloude-Pottier incoherent decomposition in the process of producing initial input data for classification. It is remarkable that there are three other decomposition parameters in the original version of Touzi decomposition. They are nevertheless redundant in 2-D land classification applications and so that the new proposed algorithm will omit them for a lower computational complexity.

There are totally four types of land covers to be discerned, including vegetation, bare soil, urban area, and water body. The detailed steps of the proposed algorithm can be found in the following.

(1) Apply the Touzi incoherent target decomposition steps itemized in Section II. It has been investigated in [6] that the configurations of window size may introduce biases of decomposition parameters. These biases will introduce an amplified error in the final classification results. Due to the significant upgrading of spatial resolution of VHR PolSAR images, the requirement of 60-look processing window that corresponds to a 9*9 window size configuration, proposed in [6] and [7], should be loosened to gather nearly unbiased incoherent decomposition parameters. Alternatively, a 7*7 window size configuration will be deployed in this algorithm. The range of scattering type phase $\phi_{\alpha s}$ will be equally divided into eight sub sections, including [$-\pi/2$, $-3\pi/8$], [$-3\pi/8$, $-2\pi/8$], [$-2\pi/8$, $-\pi/8$], [$-\pi/8$, 0], [0, $\pi/8$], [$\pi/8$, $2\pi/8$], [$2\pi/8$, $3\pi/8$], and [$3\pi/8$, $\pi/2$]. There will be eight initial top-level land classes correspondingly. Each pixel will be assigned a label according to their value of symmetric scattering type phase $\phi_{\alpha s}$.

(2) All the pixels in each top-level class will be sorted according to their symmetric scattering type magnitude α_s. The subsection with the highest 20% scattering type magnitude α_s for each top-level class and the subsection with the lowest 20% scattering type magnitude for its adjacent top-level class will be conflated to form a new second-level class. This step will generate fifteen second-level classes. Such tactic allows mitigating the negative effect of outliers in each top-level class.

(3) Adopt clustering for those second-level classes. Such clustering takes advantage of the conventional statistical models. The distance between classes in equation (8) will be employed in this step. The distance from one class to other classes will be calculated one after another. The classes with the lowest distance are merged into one class, *i.e.* the third-level class, and there will be four third-level classes ultimately. Each class center is generated by an averaging of all the members within this class.

(4) Traverse all the pixels in third-level classes. Re-calculate the Wishart distance between each pixel and each third-level class in light of equation (7). Then a re-assignment is performed for each pixel based on such a new distance. An iterative updating for class center is often needed for better classification accuracy.

(5) The new class center will be obtained by an average of all the pixels within this class in terms of scattering type phase. The mapping from third-level class to the actual land cover type is determined by equation (9). There will be four land cover types, including vegetation, bare soil, urban area, and water body. The last step is to allocate colors for each third-level class with the purpose of a better visualization.

$$third-level\ class=\begin{cases}\text{vegetation, if } -\pi/2<\phi_{\alpha s}<-\pi/4\\ \text{bare soil, if } -\pi/4\le\phi_{\alpha s}<0\\ \text{urban area, if } 0\le\phi_{\alpha s}<-\pi/4\\ \text{water body,if } \pi/4\le\phi_{\alpha s}<\pi/2\end{cases} \tag{9}$$

The dataflow and flowchart of the new proposed algorithm are illustrated in Fig. 1 and Fig. 2, respectively.

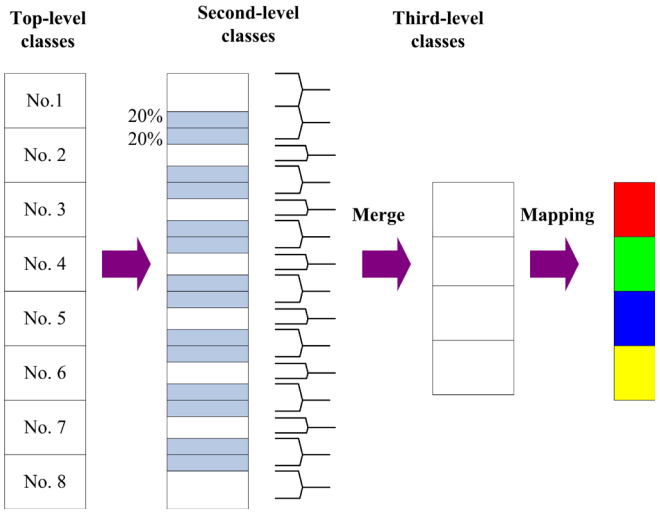


Fig. 1. The generating of top-level, second-level, and third-level classes and the dataflow.

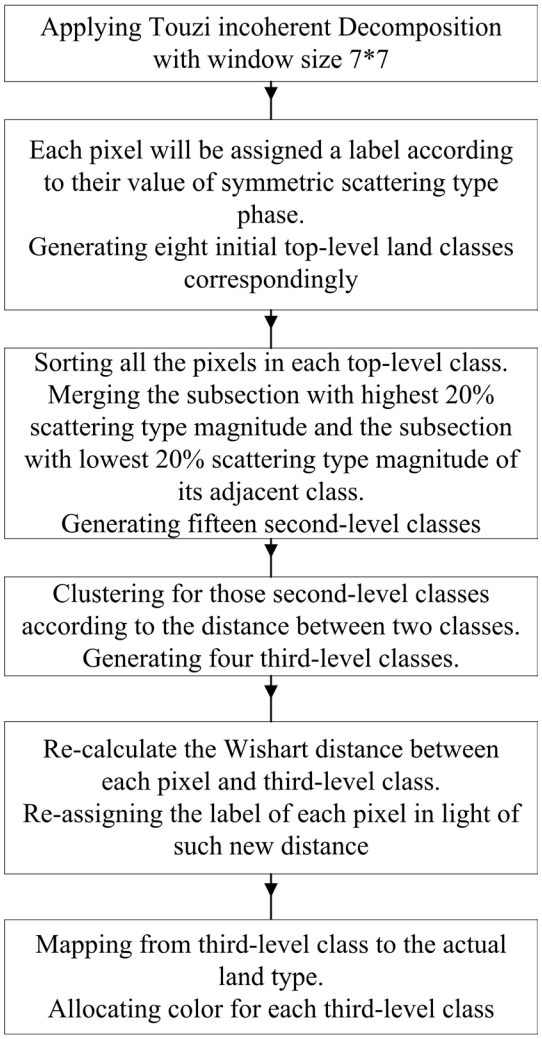


Fig. 2. The flowchart of classification scheme based on Touzi decomposition

IV. Experiment and Analysis

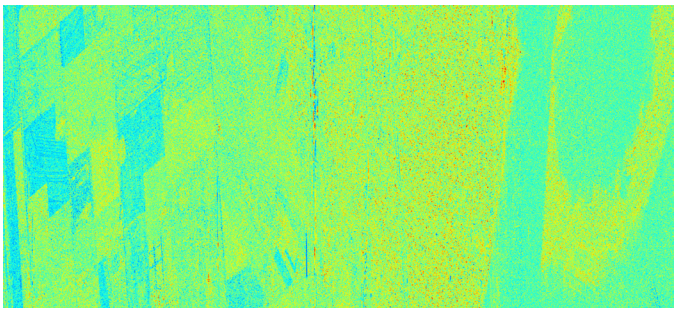
A. Test site and experimental data

The test site Rosario is the largest city in the province of Santa Fe, in central Argentina. It is located 300 km northwest of Buenos Aires, on the western shore of the Paraná River. It contains a lot of flat areas and represents a typical rural and urban landscape with heterogeneous land covers.

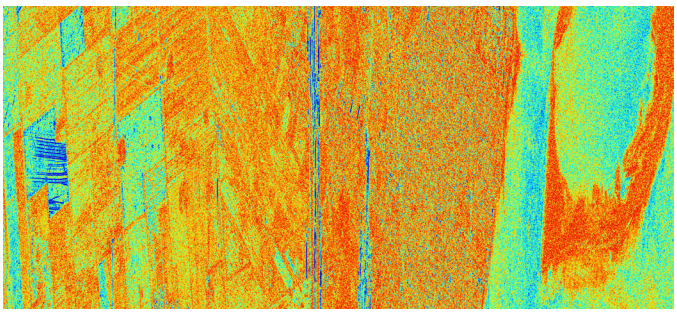
The very high resolution PolSAR experimental data to be evaluated is provided by the UAVSAR system. UAVSAR is a L-Band imaging radar instrument that uses microwaves in the 1.2 GHz range to detect and measure objects [16]. The detailed configurations of this original sample data are in table I. This sample data, courtesy of NASA/JPL-Caltech, is in single look complex (SLC) format and has slant range geometry. A sub-region with 2600 pixels in azimuth direction and 5772 pixels in range direction is cropped as an experimental area for the sake of low computational complexity. The Pauli coded pseudo-color image of this experimental area is presented in Fig. 4 (a). The production of ground truth map is accomplished under a commercial contract with Guangzhou Jiantong Surveying Mapping and Geo-information Technology Corporation, one Chinese A-class license survey company. This map for the land covers is obtained by annotations on the basis of the contemporaneous Google Earth imageries. It is essential to generate the plots of Cloude Pottier and Touzi Scattering Vector Model (TSVM) decomposition parameters respectively. These plots are listed in Fig. 3. Such plots are advantageous to make a visual comparison of the performance of two polarimetric decomposition methods. It can be easily seen from these plots that symmetric scattering type phase and magnitude attain better results for discerning diverse land covers.

Table I
The original experimental data and system configuration Parameters

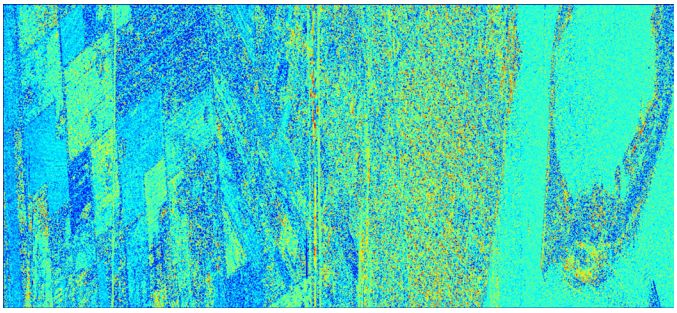
Data ID:	rosari_16002 _15033_004_150402 _L090_CX_03	Acquisition Time:	April 2nd, 2015
Wavelength:	23.8403cm	Dimension of Azimuth:	93117
Dimension of Range:	9900	Size of cell in Azimuth and Range:	(0.6m, 1.66m)



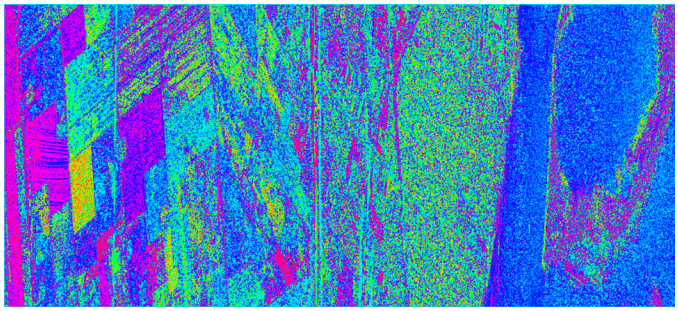
(a)



(b)

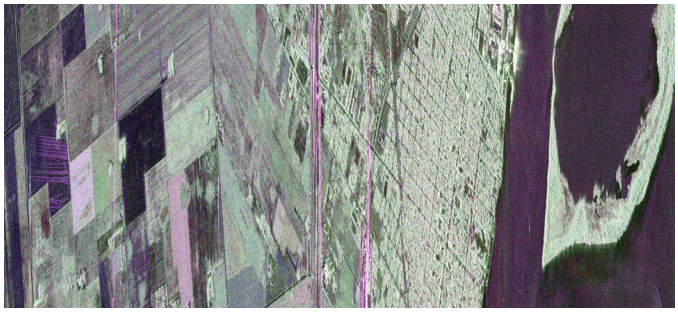


(c)

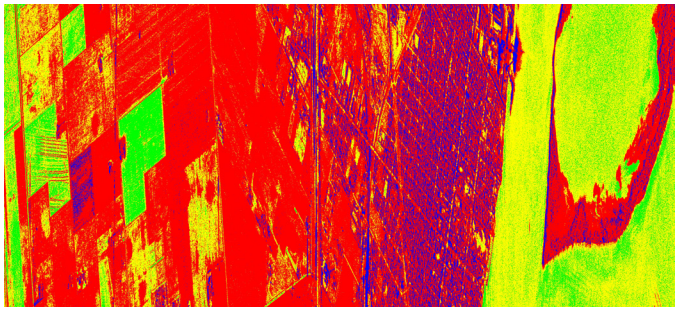


(d)

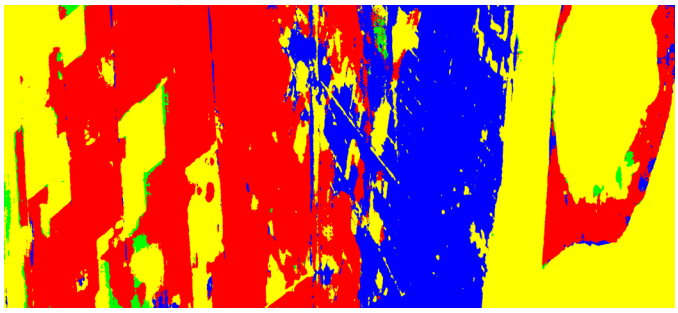
Fig. 3. The decomposition results of Cloude-Pottier target decomposition and TSVM decomposition: (a) Cloude-Pottier target decomposition - Alpha; (b) Cloude-Pottier target decomposition - Entropy; (c) TSVM decomposition - α_s ; (d) TSVM decomposition - $\phi_{\alpha s}$



(a)



(b)



(c)

Fig. 4. (a) Pauli coded pseudo-color image of experimental area cropped from Rosario. UAVSAR data courtesy NASA/JPL-Caltech.
(b) Classification results using Cloude-Pottier Model; (c) Classification results using the new proposed method.

B. Evaluation Metrics

There are various evaluation metrics used in land cover classification. Due to the limited space, only three popular metrics, including user accuracy (*UA*), producer accuracy (*PA*), and overall accuracy (*OA*), will be involved in this study. Let *M* denote the total number of classes (*M*=4 in this study). Let C_{ij} denote the total number of pixels that actually belong to class *i* but are predicted to be class *j*. Then the user accuracy, producer accuracy, and overall accuracy are defined as equation (10), equation (11), and equation (12). The *UA* indicates the ratio of the pixels in a land cover that are correctly predicted to the pixels that are actually predicted to be such sort of cover. The *PA* signifies the proportion of pixels that are correctly predicted within a certain land cover to the total number of pixels of such land cover in ground truth data. *OA* suggests what proportion is correctly classified over all the classes.

$$UA_i = \frac{C_{ii}}{\sum_{j=1}^{M} C_{ji}} \tag{10}$$

$$PA_i = \frac{C_{ii}}{\sum_{j=1}^{M} C_{ij}} \tag{11}$$

$$OA = \frac{\sum_{i=1}^{M} C_{ii}}{\sum_{i=1}^{M}\sum_{j=1}^{M} C_{ij}} \tag{12}$$

C. Results and Analysis

A set of experiments will be conducted using the very high resolution sample data in Section IV. (A). The confusion matrix of two methods, Cloude-Pottier method and the new method based on TSVM, are presented in Table II and Table III, respectively. The corresponding predicting results are listed in Fig. 4 (b) and (c). The quantitative comparison in terms of *UA* and *PA* are illustrated in Fig. 5 and Fig. 6. It can be observed that the new method based on TSVM performs better than the one based on Cloude-Pottier decomposition model in general. The *UA* and *PA* of the new method for the urban area are significantly higher than the results obtained by the method based on Cloude-Pottier decomposition. These differences of performances are mainly caused by the ambiguity of Cloude-Pottier α scattering type parameter. The extent of improvement with respect to the classifying accuracy of bare soil is not so prominent compared with of other land covers. The relatively low accuracy for discerning bare soil is chiefly caused by the performance deficiency of TSVM in terms of bare soil. As to the overall accuracy, the method based on Cloude-Pottier decomposition only achieves 67.63%. In contrast, the new method proposed in this study reaches 80.99%. It is also worthwhile to make a comparison of other recent unsupervised or semi-unsupervised land classification algorithms for PolSAR imag-

eries. Actually, the quantitative results in different studies are acquired on diverse test data. Nevertheless, it will be helpful to introduce a quantitative comparison of their predicting accuracy taking into account the main parameters of the test data used by them. The Enhanced decision tree method proposed in [13] and a unified Huynen method proposed in [14] are involved in this comparison. The *OA* obtained by the classifiers based on Cloude-Pottier decomposition, new TSVM, Enhanced decision tree, and Unified Huynen decomposition on different test data are illustrated in Fig. 7. It can be observed that Enhanced decision tree and Unified Huynen method attain higher accuracy than the Cloude-Pottier method and our new proposed method. This is caused by the characteristics of test data. For one thing, the spatial resolution of test data Rosario is 2600×5772, but the test data Winnipeg and San Francisco are only 260×480 and 900×1024 respectively. For another, the test data Rosario covers a very large area with a lot of heterogeneous land objects. However, the test data Winnipeg and San Francisco cover a relatively small area with a large number of homogeneous land objects. The performance differences of the new proposed method are less than 7%, even though the current overall accuracy is obtained on a test data which corresponds to a much larger area. Furthermore, it will be meaningful to apply our new classifier to the classic PolSAR data, such as AIRSAR San Francisco image. The ground-truth annotations provided by Liu *et al.* are used to assess the performance of new TSVM classifier [22]. The original ground-truth data, however, have six classes, including unlabeled background, mountain, water body, urban, vegetation, and bare soil. To measure the accuracy in a fair setting, the background pixels are excluded from evaluation procedure. In addition, the class mountain and vegetation are merged into one class, *i.e.* vegetation. It is noteworthy that the metrics in [14] are not based on semantic classes but on the consistency of entropy/alpha classification plane. As a result, it is not suggested here to make a comparison of the performances of the two classifiers evaluated on the AIRSAR San Francisco data. The confusion matrix of TSVM classifier evaluated on the AIRSAR San Francisco data is presented in Table IV and the corresponding classification result is demonstrated in Fig. 8. It is well known that speckle effect becomes much more dominant with regard to SAR images with normal resolution. It can be seen that the speckle of San Francisco data decreases performance significantly. It should be noted that the total amount of pixels is only 802302 excluding background pixels.

TABLE II
CONFUSION MATRIX FOR LAND CLASSIFICATION BASED ON UNSUPERVISED CLOUDE-POTTIER DECOMPOSITION METHOD

	VE	BS	UR	WB	total	*PA*
VE	4511718	799145	377212	101963	5800038	*77.92%*
BS	564560	1311376	81932	287657	2245525	*58.40%*
UR	1484585	947728	1949323	83717	4465353	*43.65%*
WB	12123	104462	12549	2377150	2506284	*94.85%*
total	6582986	3162711	2421016	2850487	15007200	
UA	*68.69%*	*41.46%*	*80.52%*	*83.39%*		***67.63%***

TABLE III
CONFUSION MATRIX FOR LAND CLASSIFICATION BASED ON NEW PROPOSED METHOD

	VE	BS	UR	WB	total	*PA*
VE	4689992	754475	297754	47817	5790038	*81.00%*
BS	465617	1452614	76015	251279	2245525	*64.69%*
UR	694080	113791	3582009	75473	4465353	*80.22%*
WB	8658	56284	11024	2430318	2506284	*96.97%*
total	5858347	3086220	3257746	2804887	15007200	
UA	*80.06%*	*61.11%*	*90.30%*	*86.65%*		***80.99%***

TABLE IV
CONFUSION MATRIX FOR LAND CLASSIFICATION BASED ON TSVM METHOD EVALUATED ON SAN FRANCISCO DATA

	VE	BS	UR	WB	total	*PA*
VE	80688	15838	18695	1019	116240	*69.42%*
BS	860	11195	709	937	13701	*81.71%*
UR	101911	26947	213909	28	342795	*62.40%*
WB	95378	73093	10799	150296	329566	*45.60%*
total	278837	127073	244112	152280	802302	
UA	*28.94%*	*8.81%*	*87.63%*	*98.70%*		***56.85%***

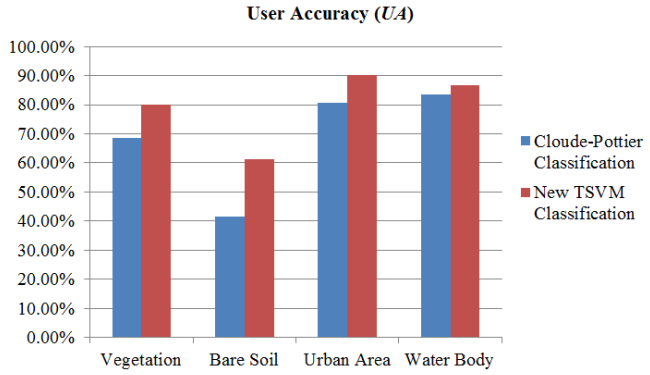


Fig. 5. *UA* of two classification methods over four land covers

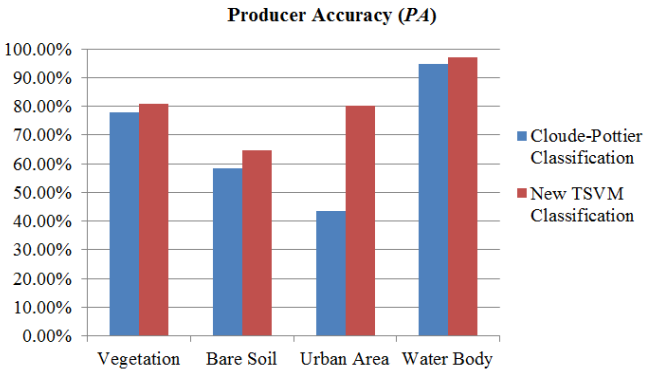


Fig. 6. *PA* of two classification methods over four land covers

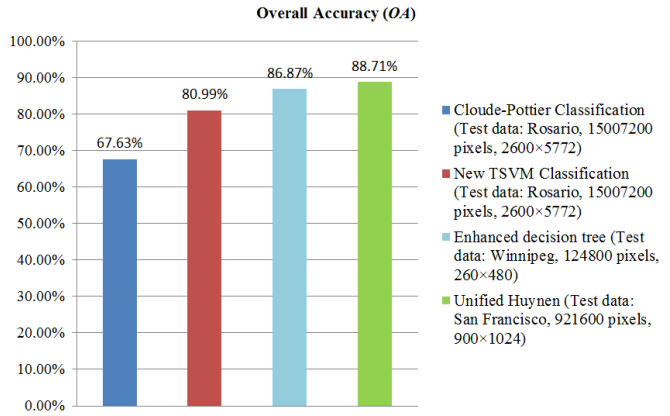


Fig. 7. OA of four classification methods

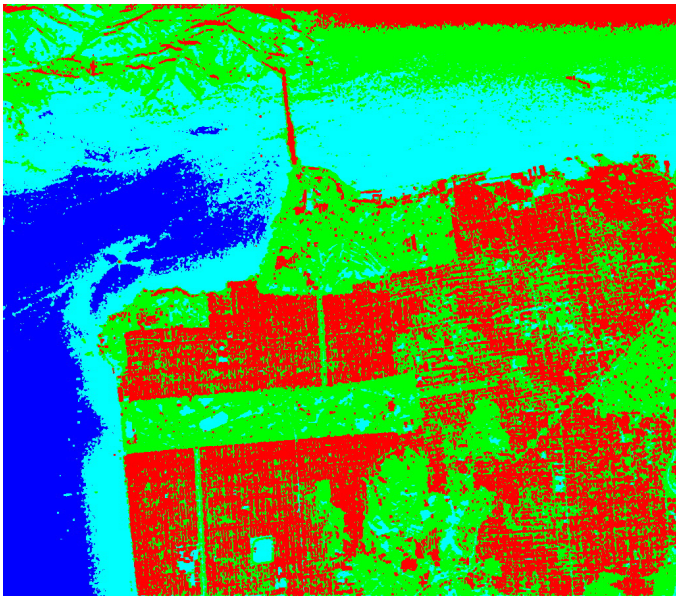


Fig. 8. Classification results evaluated on AIRSAR San Francisco data using the new proposed method. AIRSAR data courtesy NASA

V. Conclusion

The Touzi incoherent decomposition model allows a roll-invariant and unique target characterization. Hence, the Touzi scattering vector model is employed to extract coarse land classification maps in this study. A new unsupervised classifying scheme that incorporates the conventional Wishart statistical models is proposed based on the coarse land classification maps. Quantitative evaluation results validate the effectiveness of the new proposed method. Such sort of classifying method becomes even more important when it is impossible to acquire a large number of training samples with human annotations. In addition, it will be valuable to conduct a further revision to the TSVM model to improve the ability of discerning bare soil and conduct experiments on other airborne very high resolution PolSAR images.

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A Full Adder Design with CNFETs for Real Time, Fault Tolerant and Mission Critical Applications

Jitendra Kumar Saini, Avireni Srinivasulu, and Renu Kumawat

***Abstract*—The VLSI based circuits often pose challenges in the form of various faults (such as transient faults, permanent faults, stuck-at-faults). These faults appear even after testing also. They occur because of reduction in the size of the circuit or during real-time implementation, as these faults are difficult to detect. It is very important to detect and rectify all such faults to make the system foolproof and achieve expected functionality. In this paper, 12 transistors based, full adder circuit (12T-FAC) using Carbon Nanotube Field Effect Transistor (CNFET) technology is proposed. The proposed design based on CNFET provides high fault resistance towards transient, permanent faults and works with least power, delay and power-delay product (PDP). Later, features like fault detection and correction circuit have been added in 12T-FAC. The final version of full adder circuit capable of correcting errors has been used in designing applications like multipliers. The proposed full adder circuit was designed with CNFET technology, simulated at 32 nm with supply voltage +0.9 V using the Cadence Virtuoso CAD tool. The model used is Stanford PTM.**

***Keywords*—CNFET, Full Adder, Fault Detection Full Adder, Fault Correction Full Adder, Multiplier.**

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I. Introduction

INIn the real-time circuits, it is crucial to identify faults else the outcome may be catastrophic for the system and may even claim human lives too. While designing circuits for these applications, fault detection and fault correction have played a crucial role and posed challenges [1]. As Moore's Law states, "The number of transistors in dense integrated circuit doubles every two years", and hence leads to the growth of complexity. The efforts to bring down the size of the circuits have also made the later prone to certain faults like crosstalk, noise, etc. There are other setback issues which remain undetected during the initial testing. These issues are often difficult to detect and more concerned for its rectification and therefore the majority of the researchers usually concentrate on the identification and rectification of such issues [2]. The integrated circuits can be designed using various components like adder being the most common among the preferred by the designers. An adder is the simplest component capable of executing an arithmetic operation. It can be used to design various similar arithmetic and logical circuits [3].

The applications where carbon nanotubes may be used are antennas, invasive nanobots, miniaturized satellites, and Geo-positioning systems [4]. But there are applications where an alternate to resistors may work more effectively in optics based devices wherein Chlorophyll like organic semiconductors such as phthalocyanines (CuPc) with good thermal stability, chemical stability, light resistance, temperature resistance, coating strength and resistance to bases is preferred [4]-[5]. Some such applications are temperature sensors, humidity sensors, photo detectors, solar cells, optoelectronic devices, radio frequency identification, etc [5]. For these applications, the real-time systems need on-the-fly fault detection and correction circuits to make a system truly fault-tolerant. [5]

In VLSI, adders are used extensively and hence while designing a circuit using CNFET [6], adders are an obvious choice.

Carbon nanotube (CNT) is an allotrope of carbon with a cylindrical structure. The structure is found to be either single-walled carbon nano tube (SWCNT) or multi-walled carbon nano tube (MWCNT). SWCNT is a single sheet rolled up cylindrically along a wrapping vector $C = n_1\mathrm{a} + n_2\mathrm{b}$, where n_1 and n_2 are positive integers which specify the Chirality of the tube, and 'a' and 'b' are lattice unit vectors, as shown in Fig. 1.

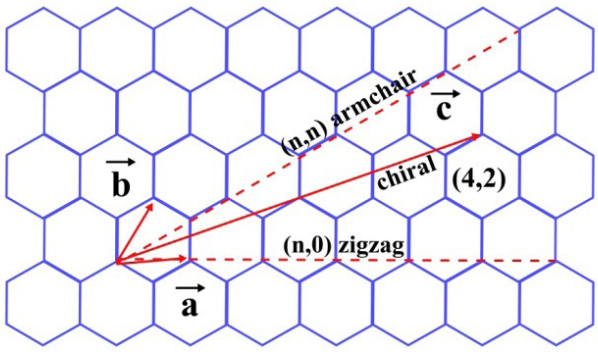

Fig. 1. A spread-out sheet of graphite and Chirality of the CNT tube [8]

Depending upon the value of n_1 and n_2, SWCNT can be either metallic or semiconducting. If the n_1-n_2 is a multiple of 3,

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Jitendra Kumar Saini is with the Department of Electronics and Communication Engineering, Manipal University Jaipur, Jaipur-303007, INDIA (e-mail: jitendraksaini@bitmesra.ac.in).

Avireni Srinivasulu, Senior Member, IEEE, is with the Department of Electronics and Communication Engineering, JECRC University, Jaipur-303905, Rajasthan, INDIA. (E-mail: avireni@jecrcu.edu.in (or) avireni@ieee.org).

Renu Kumawat is with the Department of Electronics and Communication Engineering, Manipal University Jaipur, Jaipur-303007, INDIA (e-mail: renu.kumawat@jaipur.manipal.edu).

SWCNT is metallic or else it is semiconductor.Further classification of SWCNT includes armchair CNT ($n_1 = n_2 = n$), zigzag CNT ($n_1=n$, $n_2 = 0$) and Chiral CNT ($n_1 \neq n_2$ and n_1, $n_2 \neq 0$). The armchair CNTs conductors while zigzag and Chiral CNT's act as either semiconductor or conductor depending upon the difference in indices (i.e. n_1-n_2) [7]-[8].

The expression for the threshold voltage (V_{th}) [7], equivalent to half the band gap of CNFET is shown in (1):

$$V_{th} \approx E_{bg} / 2e \approx 0.436 / D_{CNT}(nm) \quad (1)$$

Where the E_{bg} is the band gap of CNFET, e is the electron charge, D_{CNT} is the diameter of carbon nanotubes as given in (2):

$$D_{CNT} = d \approx 0.0783\sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (2)$$

The thermal efficiency (Z) of the circuit as given in (3) is improved using nano-structuring and bandgap engineering by reducing the lattice thermal conductance and enhancing the Seebeck coefficient [9]. CNT based applications typically offer superior potential where the CNTs increase the power factor with increasing temperature [9].

Efficiency (Z) is calculated from expression [10]:

$$Z = \frac{\sigma\alpha^2}{K} \quad (3)$$

where, σis the electrical conductivity, k is the thermal conductivity and α is the Seeback coefficient. Later a dimensionless figure of merit came into existence which is calculated as ZT.

Temperature (T) as shown in (4) is calculated from expression [10]:

$$T = \frac{T_1 + T_2}{2} \quad (4)$$

where, T_1 and T_2 are the temperature of two contacts. The above equations are applicable for fabricating power generation devices using Bi_2Te_3 and CNT along with silicon adhesive.

Section II and III of theresearch article discuss the existing full adder circuit designs and fault tolerant circuit designs approaching all along the drawbacks. Section IV discusses the proposed design. Section V gives the simulation results, comparative details and finally Section VI give concluding remarks.

II. Existing Full Adde r Circuit Designs

The conventional full adder design [3] consists of 28 transistors and has a larger propagation delay due to the presence of 5 transistors in the output data path. Transmission Gate Adder (TGA) works on transmission gate logic, has a transistor count of 20 and critical data path delay of 4 transistors. This design has a drawback in driving capability [3]. Transmission Function Adder (TFA) carrying 16 transistors works on the principle of the transmission function theory. Similarly TGA and TFA also suffer in its driving capabilities [11].

In the case of Complementary Pass-transistor Logic Transmission Gate (CPL-TG), this design has better driving abilities but however it uses more transistors [12]. Mirror full adder design is an alternative to C-CMOS based full adder circuit. Mirror adder uses Pass Transistor Logic (PTL) approach that has a critical path of 4 transistors. Thus, it results in faster full adder design and lower power delay product along with a high transistor count [13]. Static Energy Recovery Full Adder (SERF) uses only 10 transistors, but suffers from a threshold loss of problem [14]. The 13A full adder circuit uses 10 transistors similar to SERF full adder design and suffers from a specific problem of output voltage level degradation [15]. Hybrid Pass Transistor Logic with Static CMOS output drive (HPSC) full adder is designed using transmission gate logic, pass transistor logic and CMOS logic with a transistor count of 26 [16]. NEW-HPSC full adder consists of 24 transistors and has higher power consumption because it has one extra inverter in the full adder design [17]. Complementary and level restoring carry logic full adder (CLRCL) is based on pass transistor logic and uses only 10 transistors. In this case, power consumption is more due to the presence of inverter circuit in the design of a full adder [18]. The Ours1 full adder consists of double pass-transistor logic (DPL) and that uses 28 transistors in the circuit of full adder. This design suffers from poor driving capability [19]. Hybrid CMOS logic with transmission gate logic full adder (HCTG) consists of 16 transistors and has a critical path delay of 4 transistors. One important drawback in HCTG is that it is not suitable for cascaded stages because it has poor driving capability due to the coupling of inputs and outputs [20]. Removed Single Driving Full Adder (RSD-FA) consists of 26 transistors. This design has an XOR/XNOR circuit that exhibits full driving capability and output delay path of 4 transistors. RSD-FA provide lower power consumption as well as the high speed at the cost of more transistor count [21]. In 1-Bit full adder with 18 transistors [22], five inverters are used that is three at primary inputs and 2 in the intermediate stage which results in poor driving capability. Hybrid Multi-Threshold Full Adder (HMTFA) consists of 23 transistors. Provides Critical path of 4 transistors and experience a threshold problem due to the use of more number of inverters [23].

Literature review of full adders has been verified with different logic families. They are found to vary in their characteristic features, performance, power consumption and propagation delay. The crucial points undermining the approximation and comparison of performance among the devices are delay, power consumption, and power-delay product. Circuit delay along with other factors is largely on account of number of transistors consecutively connected in series all along the channel width and intra-cell wiring capacitances. Similarly, size is directly proportional to the number of transistors and results into complexity while implementation. Thus, by reducing the number of transistors, we can optimize the circuit performance in terms of area and speed.

This paper demonstrates the improvement in circuit performance by reducing the number of transistors and length of the critical path of outputs. One-bit full adder circuit using 12 CNFETs (denoted as 12T-FAC) has been proposed in this paper. In the proposed full adder circuit, care has been taken to minimize the limitations of the earlier proposed full adder and also to improve the overall circuit performance.

III. Existing Fault-Tolerant Circuit Designs Approach

Any fault tolerant system needs to acquire few characteristics by virtue of its design, existing design approaches like redundancy (time, hardware), etc. are summed up to get the features at a glance. Here on Time Redundant design approach deals with fault detection by executing the same operation on two circuits which are identical and at times by adding latency in the input feed of one of the circuits and compare the output thus obtained, where the same output represents no fault and the difference of output represents a defaulted circuit [1]. The Hardware Redundancy design approach requires multiple instances (two, three or more) of the identical circuits with common input feed giving out different results [2]. Operand Width Aware Hardware Reuse design approach uses the combination of the static and dynamic (redundant) adder to design ALUs. The Self-Checking Carry Select Adder design [24] approach detects single bit fault at run time and also capable of detecting a stuck-at fault. Self-Repairing Adder [25] design approach makes use of a pre-defined rule which says, "For 3 input adders, same input values should produce the same output values and if any of the input is flipped, the output differs". The Real-Time Fault Tolerant Full Adder design approach moves one step ahead and is capable of detection and correction of single and double faults at run time [26].

Every technique has got its own advantages and disadvantages like time redundant design approach is unable to detect faults if the results of the initial input feed are incorrect [27]. This approach does not detect stuck-at-faults. In hardware redundant design approach real-time faults and stuck-at faults may not be possible to detect, hence correction circuit cannot be designed, and also there will be a drasticincrease in size of the circuit [28]. In Operand Width Aware Hardware Reuse design approach the computational complexity, power consumption, and fault propagation are the challenges that designers need to address [29]. The Self Checking Carry Select Adder design approach [30] suffers from a probable handicap to detect the fault site if there are multiple faults detected in the circuit. It also restricts its use in self-correcting circuits. The Self Repairing Adder design approach [31] fails while multiple wrong inputs are provided to the adder and are unable to identify the location. In Real-Time Fault-Tolerant Full Adder design approach the number of hardware components is high due to redundancy in design and thus are more costly [32]-[33]. Due to the redundant circuit design, critical path delay is increased and thereby increases the overall circuit delay [34]-[38].

The proposed design of full adder circuit (12T-FAC) along with error detection and correction circuit mechanism deals with delay, reduces the redundant components, identifies stuck-at-fault, can also detect multiple fault locations and is capable of fault corrections. Hence, fabrication of the proposed design, true real-time fault tolerant circuit design can be achieved [39]-[42].

IV. Proposed Design

The proposed system is verified on the basis of the criteria given below:

1) ***Test Strategy:*** We have tested the output under two functional units considering each output (Sum and Carry) to be independent of the other. This strategy allows us to trace back the fault location.
2) ***Hardware Design:*** The circuit reduces the need for redundant adders and it does not make use of multiple rail checkers which allows a comparatively lean hardware design.
3) ***Fault Detection:*** Proposed design is fully capable of fault detection and fault correction in case of sporadically occurring transient and other permanent faults.

The block diagram of the proposed 1-bit adder circuit as represented in Fig. 2 contains three blocks, wherein,*Block-A* takes input A and B to produce intermediate output as XOR/XNOR signal pair. This block is implemented using transistors C_1, C_2, C_3, C_8, C_9, and C_{10}. *Block-B* is a Pass Transistor Logic implementation that takes intermediate output XOR/XNOR as input along with initial carry C_{in} (if any) and generates output Sum. *Block-B* is implemented using C_4, C_5, C_6, and C_{11}. *Block-C* is a multiplexer that takes A, XNOR, and C_{in} as input and produces Carry as output. *Block-C* is implemented using transistors C_7 and C_{12}.

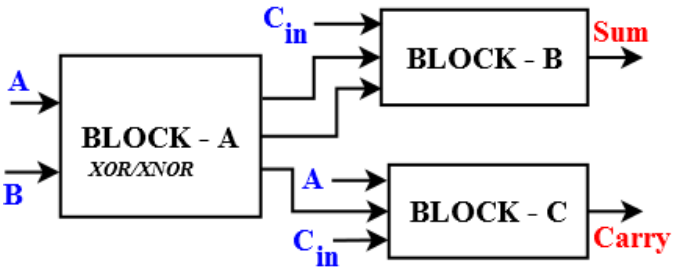

Fig. 2. Block diagram of proposed 12T-FAC

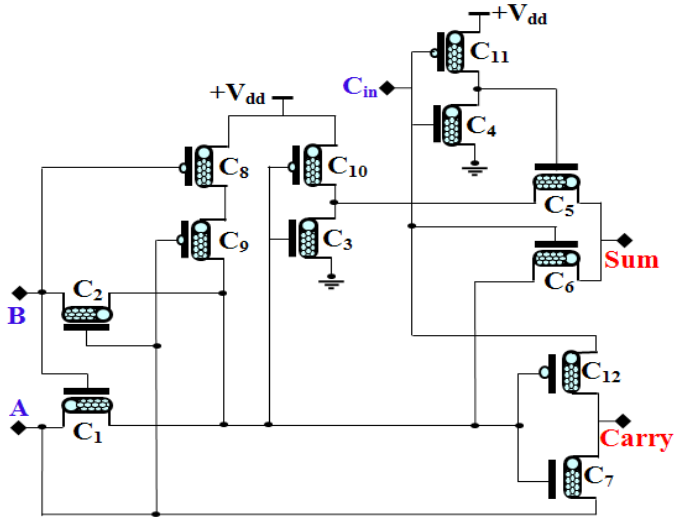

Fig. 3. Schematic of proposed 12T-FAC implemented using CNFET.

The proposed 12 transistors full adder circuit using CNFET is shown in Fig. 3. The proposed 12T-FAC circuit has a critical path delay of 3 and provides full output voltage swing. The Sum and Carry equation of 12T-FAC are:

$$\text{Sum} = \text{A} \oplus \text{B} \oplus \text{C}_{in} \tag{5}$$

$$Sum = \overline{A}\,\overline{B}C_{in} + \overline{A}\text{B}\overline{C_{in}} + \text{A}\overline{B}\,\overline{C_{in}} + ABC_{in} \tag{6}$$

$$\mathbf{Sum = (AB + \overline{A}\,\overline{B})C_{in} + (A\overline{B} + \overline{A}B)\overline{C_{in}}} \tag{7}$$

$$Carry = (A\overline{B} + \overline{A}\text{B})C_{in} + \text{A}(\overline{A}\,\overline{B} + AB) \tag{8}$$

$$\mathbf{Carry = (A\overline{B} + \overline{A}B)C_{in} + AB} \tag{9}$$

Using (2) the value of D_{CNT} was calculated keeping the value of $n_2 = 0$ and varying value of n_1 in the range of 7-19 with step size 2.

$$D_{CNT} = 0.0783 * n_1 \tag{10}$$

Similarly, using (1) and the various D_{CNT} values, the value of V_{th} was calculated as

$$V_{th} = 0.436 / D_{CNT} \tag{11}$$

Using 12T-FAC, theFault Detection Full Adder (FDFA) circuit based on CNFET is proposed. This circuit is capable of detecting multiple faults (single and double) in real-time along with identification of fault site. The schematic of the FDFA is shown in Fig. 4.

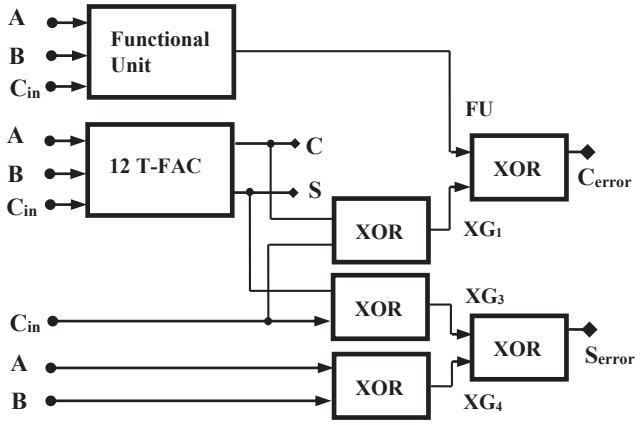

Fig. 4. Schematic of FDFA

Proposed FDFA makes use of 3 input (A, B, C_{in}) and generates 4 output (S, C, S_{error}, C_{error}) where S and C denotes actual results (i.e. Sum and Carry) of FDFA and S_{error} and C_{error} verifies whether there is an error in the sum or carry outputs of FDFA respectively. C_{error} is generated by XOR of XG_1 and Functional Unit (FU) given in (12) whereas, intermediate output stage FU and XG_1 are shown in (12) and (13) respectively.

$$\text{FU} = \overline{(\text{A} + \text{B} + \overline{\text{C}_{in}})(\overline{\text{A}} + \overline{\text{B}} + \text{C}_{in})} \tag{12}$$

$$\text{XG}_1 = \text{C} \oplus \text{C}_{in} \tag{13}$$

$$\mathbf{C_{error} = FU \oplus XG_1} \tag{14}$$

When C_{error} = '0', indicates fault-free FDFA circuit while C_{error} = '1', indicates the faulty FDFA circuit and the fault site is the carry output stream.

Similarly, in regards to the detection of a fault, if fault site is in the sum output stream that requires 3 XOR gates. S_{error} is generated by XOR of XG_3 and XG_4 shown in (17) whereas, intermediate output stage XG_3 and XG_4 are shown in (15) and (16) respectively.

$$\text{XG}_3 = \text{C}_{in} \oplus S \tag{15}$$

$$\text{XG}_4 = \text{A} \oplus \text{B} \tag{16}$$

$$\mathbf{S_{error} = XG_3 \oplus XG_4} \tag{17}$$

When S_{error} = '0', indicates fault-free FDFA circuit, while S_{error} = '1', indicates the faulty FDFA circuit and the fault site is the sum output stream. These would make it capable of detecting single or multiple faults occurring in sum and carry bits and when no error occurs, then S_{error} and C_{error} will remain Zero representing fault free FDFA.

Once the fault site is identified, the proposed FDFA makes use of Fault Correction Full Adder (FCFA) for recovery of erroneous input in real-time. This circuit design deal with all the sporadically occurring transient faults and permanent hardware faults thus make the circuit a real fault-tolerant design.

In this approach, an inverter is used along with multiplexer to correct the output sum and carry, instead of using standby adder to replace the faulty adder as is used in earlier approaches. This substantially reduces the hardware size to a fraction as compared to the other existing design approaches. The schematic of the FCFA is shown in Fig. 5.

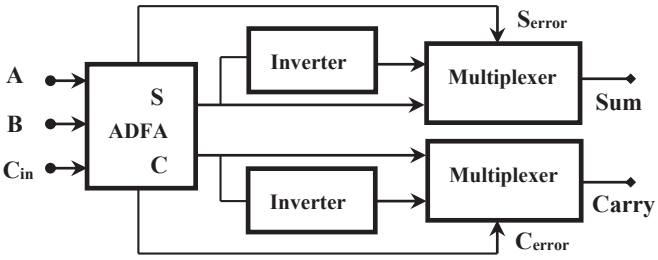

Fig. 5. Schematic of proposed FCFA.

The output (S and C) generated by the 12T-FAC from input (A, B, C_{in}) is fed to the FDFA circuit which produces output (S, C, S_{error} and C_{error}) to be further fed to FCFA, which takes S, C and their complements as input and passes to the Multiplexer where S_{error} and C_{error} are used as select line, depending upon the detection of error output the Sum and Carry are selected.

If the outputs S_{error} and C_{error} are 0, then the S and C outputs of FDFA are directly transferred as final Sum and Carry of FCFA with the help of multiplexer and if S_{error} and C_{error} of FDFA are 1, then the inverted outputs received from the inverter gets selected by multiplexer and are transferred as final Sum or $\overline{\text{Sum}}$ and Carry or $\overline{\text{Carry}}$ of FCFA.

V. Simulation Results And Comparison

The simulation is carried out using the Cadence Virtuoso Tool. The circuit is designed with CNFET 32 nm technology [43] at Supply Voltage ($+V_{dd}$) 0.9 V. The waveform of the 12T-FAC consists of inputs (A, B, C_{in}) and outputs (Sum and Carry) are shown in Fig. 6.

TABLE I
Comparison Between Proposed 12T-FAC And Other Full Adders in Terms of Transistor Count, Delay, Power and PDP.

Full Adder	Transistor Count	Power (µW)	Delay (ps)	PDP (aJ)
C-CMOS [3]	28	0.124	12.355	1.532
TGA [3]	20	0.135	10.104	1.364
TFA [11]	16	0.109	11.701	1.275
SERF [14]	10	3.326	9852.7	32770.0
13A [15]	10	5.819	9507.8	55325.8
NEW-HPSC [17]	24	0.123	30.232	3.718
CLRCL[18]	10	5.903	231.18	1364.6
RSD-FA [21]	26	0.091	9.427	0.857
18T-FA [22]	18	0.088	8.93	0.785
HMTFA [23]	23	0.121	16.909	2.056
This work	12	0.039	6.876	0.268

The simulation results of all the full adders as reported in Section 2 and proposed 12T-FAC are summarized in Table I. However, the supply voltage ($+V_{DD}$) is varied in the range of 0.6 V to 1.4 V with a step size of 0.1 V to verify the fault tolerance of the circuit in varying voltage scenario. It was observed that the proposed circuit performs consistently under variations in various parameters, as could be seen in Table II.

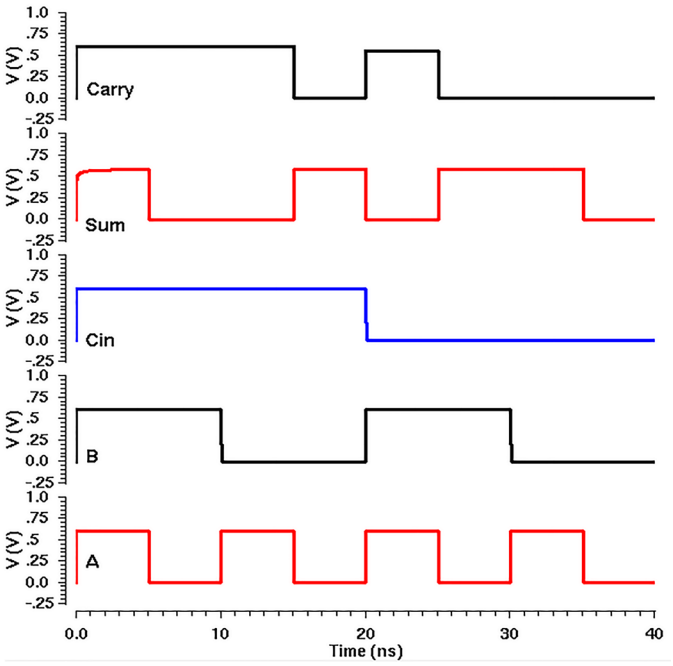

Fig. 6. Waveform of proposed 12T-FAC using CNFET

TABLE II
Comparison of proposed 12T-FAC design in terms of variation in V_{DD} Supply from 0.6 V to 1.4 V for 32 nm CNFET Technology with Vth = 0.289 V.

Proposed Full Adder	V_{DD} (Volts)	12T-FAC
Average Power	0.6	0.018 µW
	0.7	0.022 µW
	0.8	0.029 µW
	0.9	0.039 µW
	1.0	0.059 µW
	1.1	0.076 µW
	1.2	0.095 µW
	1.3	0.119 µW
	1.4	0.166 µW
Delay	0.6	9.353ps
	0.7	8.019ps
	0.8	7.821ps
	0.9	6.876ps
	1.0	6.772ps
	1.1	6.701ps
	1.2	6.559ps
	1.3	6.498ps
	1.4	6.339ps
PDP	0.6	0.168aJ
	0.7	0.176aJ
	0.8	0.227aJ
	0.9	0.268aJ
	1.0	0.400aJ
	1.1	0.509aJ
	1.2	0.623aJ
	1.3	0.773aJ
	1.4	1.052aJ

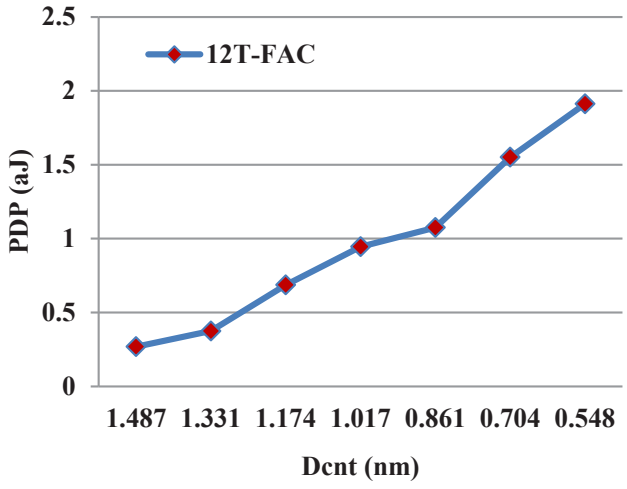

Fig. 7. PDP Versus Dcnt Variations for proposed circuit

The results from (10) and (11) are used to plot parameter variation of power-delay product (PDP) of 12T-FAC with CNFET diameter (D_{CNT}) and threshold voltage (V_{th}) as shown in Figs. 7 and 8, respectively.

The CNT structure used is SWCNT in Zigzag orientation where (n_1 = n, n_2 = 0). For simulation and study purpose, the value of n1 was varied in the range of 7 to 19. Significant PDP results were observed at n_1 = 19 and hence the value was used for further comparisons. Other CNFET parameters used during the simulation are shown in Table III.

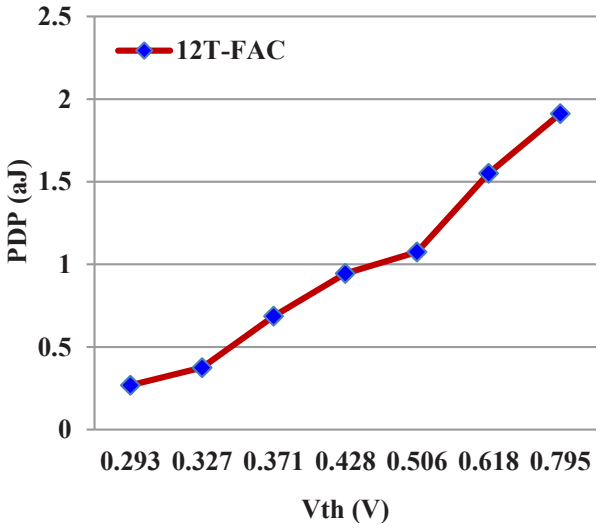

Fig. 8. PDP Versus Vth Variations for proposed circuit.

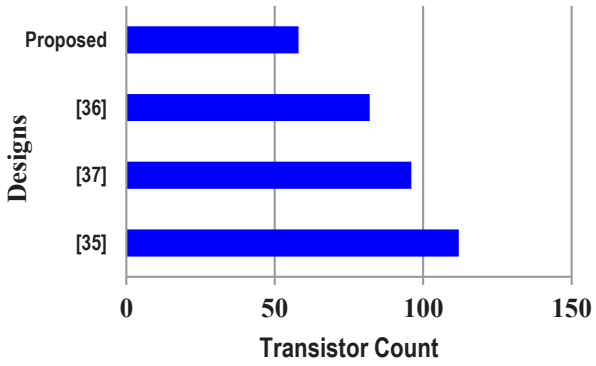

Fig. 9. Comparison of fault tolerant design with transistor count.

TABLE III
CNFET DESCRIPTION, VALUE AND ITS PARAMETER.

Description	Value	CNFET Parameter
Physical channel length	32 nm	Lg
The mean free path in the intrinsic CNT channel	200 nm	Lgeff
The length of doped CNT source-side extension region	32 nm	Lss
The length of doped CNT drain-side extension region	32 nm	Ldd
The Fermi level of the doped S/D tube	6 EV	Efi
The dielectric constant of high-k top gate dielectric material	16	Kgate
The thickness of high-k top gate dielectric material	4 nm	Tox
The coupling capacitance between the channel region and the substrate	20 pf/m	Csub
Distance between the tubes	20 nm	Pitch
Zigzag Structure	19	n1
	0	n2
Number of CNT tubes	3	CNTPos

The impact of temperature variations on the proposed 12T-FAC circuit was observed from the simulations for the temperature range -50°C to 150°C. The simulated temperature stability was observed to be 0.00000035%, as shown in Fig.10.

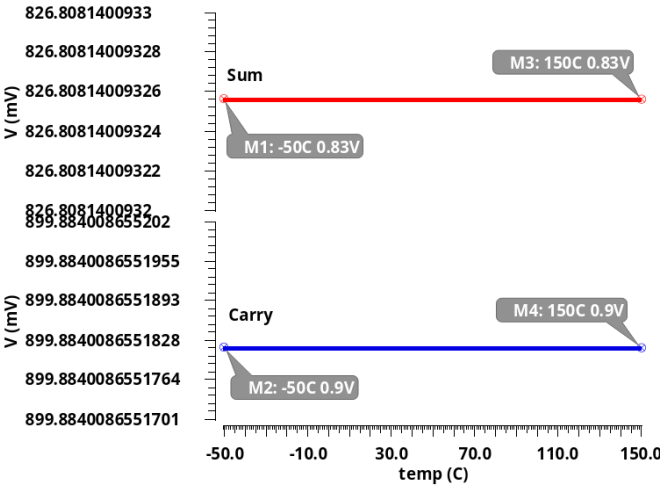

Fig. 10. Simulated temperature stability 12T-FAC

The static power consumption is determined by the clock and all other inputs that are connected with the low logic to check the leakage current.

The dynamic power dissipation is calculated using switching frequency and external load capacitance from relation [5]:

$$P_{dynamic} = \alpha C_L f V_{DD}^2 \quad (18)$$

where α ($0 \le \alpha \le 1$) is switching activity factor, f is the clock frequency and C_L is the load capacitance. The frequency and capacitance are directly proportional to the dynamic power consumption.

To find the static power and leakage current, V_{DD} = 0.9V is supplied with low level inputs (*A, B, Cin*), whereas to calculate total power consumption V_{DD} = 0.9 V is supplied with inputs (*A, B, Cin*). When these parameters were applied to simulate the proposed 12T-FAC leakage current, static power, dynamic power, and total power recorded were 0.275 nA, 0.256 nW, 38.979 nW, and 39.235 nW, respectively.

The average power consumption of 1-bit FCFA was found to be 9.81 nW and delay was 5.382 ps. The power-delay prod-

uct was 0.0528 aj. The circuit thus designed when simulated along with existing designs, was found to be at-par in terms of capabilities like fault detection and fault correction. Also, it is evident that the proposed design reduces the number of transistors by 30% and the size by 45% approximately as depicted in Fig. 9.

TABLE III
CNFET DESCRIPTION, VALUE AND ITS PARAMETER.

Description	Value	CNFET Parameter
Physical channel length	32 nm	*Lg*
The mean free path in the intrinsic CNT channel	200 nm	*Lgeff*
The length of doped CNT source-side extension region	32 nm	*Lss*
The length of doped CNT drain-side extension region	32 nm	*Ldd*
The Fermi level of the doped S/D tube	6 EV	*Efi*
The dielectric constant of high-k top gate dielectric material	16	*Kgate*
The thickness of high-k top gate dielectric material	4 nm	*Tox*
The coupling capacitance between the channel region and the substrate	20 pf/m	*Csub*
Distance between the tubes	20 nm	*Pitch*
Zigzag Structure	19	*n1*
	0	*n2*
Number of CNT tubes	3	*CNTPos*

Table IV gives the capability comparison with the existing design approaches. At the time of simulation, it has been observed that the proposed circuit of FCFA is successfully able to auto correct the error, if any. From Fig. 11, it can be seen that the input sequence (A, B, C_{in}) without any error (S_{error}=C_{error}=0) gives expected output for various input combinations.

TABLE IV
CAPABILITY COMPARISON WITH EXISTING DESIGN APPROACHES.

Designs	[31]	[33]	[32]	Proposed
Individual transistor count	2-Adder 56 4-XNOR 24 2-Eqt 24 2-Mux 08	1-Adder 28 2-XNOR 10 2 AND 14 1 OR 6 1-Fun.Unit 14 2-Mux 08 8-Inverter 16	1-Adder 28 5-XNOR 30 1-Fun. Unit 12 2-Mux 08 2-Inverter 04	1-Adder 12 5-XOR 20 1-Fun. Unit 18 2-Mux 04 2-Inverter 04
Total number of transistors	112	96	82	58
Fault coverage	Single net Multi net Single fault	Single net Multi net Single fault Double fault Stuck-at fault	Single net Multi net Single fault Double fault Stuck-at fault	Single net Multi net Single fault Double fault Stuck-at fault
Fault repairing	Not possible in case of double fault	Possible in all cases	Possible in all cases	Possible in all cases
Output reliability single fault	100%	100%	100%	100%
Output reliability double fault	85.82%	100%	100%	100%
Technology	CMOS	CMOS	CMOS	CMOS/ CNTFET

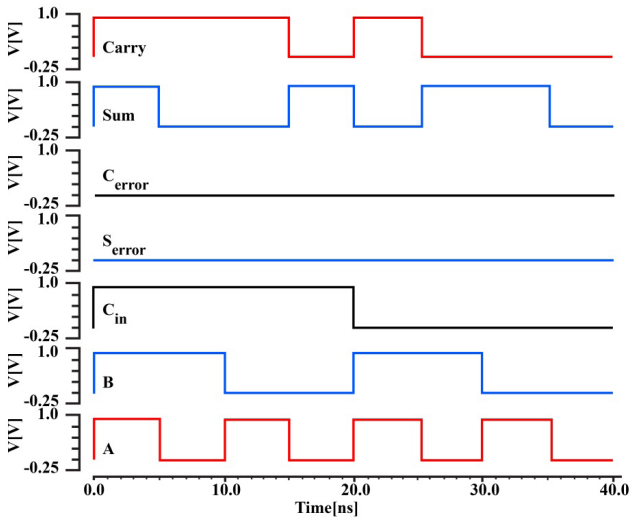

Fig. 11. Output waveform of FCFA with no error.

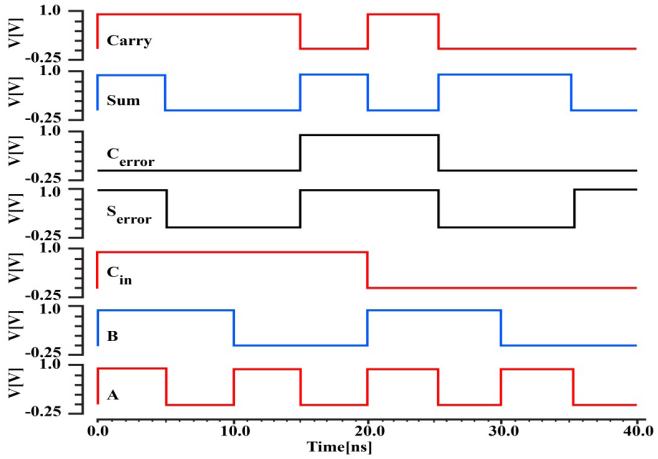

Fig. 12. Output waveform of FCFA with error correction in Sum and Carry

In Fig. 12, the observed output from input sequence (A, B, C_{in}) with fault detected in S_{error} and C_{error} of 12T-FAC shows the capability to auto correct the fault in final Sum and Carry. Further, to test the performance of FCFA in complex circuits, multiplier is designed in both CMOS and CNFET technology as dipicted in Table V.

TABLE V
COMPARISON OF MULTIPLIER DESIGNS.

Multipliers	Power (μW)	Delay (ps)	PDP (aj)	Technology (nm)
4 BIT Multiplier [32]	94.38	598.3	56467.6	CMOS 55
Proposed 4 BIT Multiplier CMOS	24.21	418.3	10127.0	CMOS 45
Proposed 4 BIT Multiplier CNFET	2.884	303.4	875.006	CNFET 32
8 BIT Multiplier [32]	712	1326	944112	CMOS 55
Proposed 8 BIT Multiplier CMOS	498	987.3	491675.4	CMOS 45
Proposed 8 BIT Multiplier CNFET	21.75	672.4	14624.7	CNFET 32

VI. CONCLUSION

In this paper, we have proposed a Full Adder Circuit (12T-FAC) using CNFET, Fault Detection Full Adder (FDFA) Circuit using CNFET, Fault Correction Full Adder (FCFA) Circuit using CNFET, 4-bit and 8-bit multiplier circuit using FCFA and CNFET.

The 12T-FAC is optimized to consume less power, having lesser delay and that too with less than the average number of transistors when compared with other similar designs. The proposed design is capable of performing all the tasks its peers are capable of. The FDFA and FCFA are the functionality extensions of proposed 12T-FAC to detect and correct the input/output. Finally, to test this circuit for its scope, capabilities, and worthiness, it was used to design a multiplier application.

It can also be seen from the simulation results that the Adders and Multipliers thus designed are producing better results as compared to other prevalent designs of a full adder. Table IV shows that the proposed ACFA design reduces the number of transistors required by 30% and the size by approximately 45%. Also, when the application (multiplier) was compared with other similar multiplier designs, the power consumption was found to be substantially low and so the delay. The proposed design deals with faults in real time and performs corrective action, this enables us to conclude that the proposed 12T-FAC is a better-suited design and a choice for future applications.

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Sensitivity Analysis of the UTBSOI Transistor based Two-Stage Operational Amplifier

Rekib Uddin Ahmed, Eklare Akshay Vijaykumar, and Prabir Saha

***Abstract*—In the nanoscale domain, the MOSFETs are prone to various physical effects due to their shorter channel region known as short-channel effects (SCE). The researchers have proposed an advanced structure of MOSFET known as the ultrathin-body silicon-on-insulator (UTBSOI) to overcome the limitations of SCEs. The UTBSOI is a type of double-gate (DG) MOSFET having superior controllability of gates over the shorter channel region. Nowadays, the UTBSOI MOSFETs can be adopted in the circuit simulators through the use of a device model named BSIM-IMG. The BSIM-IMG has made it possible for the circuit designers to simulate any UTBSOI based analog blocks like operational amplifiers (opamp). The performance parameters of an opamp are very much sensitive to any perturbation in size (W/L) of the constituent MOSFETs, that may cause a drastic change in the output. In this paper, the sensitivity analysis procedure has been proposed for the CMOS and UTBSOI based two-stage opamps as the function of perturbation in W/L. In addition to this, an algorithm has also been presented to do the same. From the simulation results, it is observed that the sensitivity of the UTBSOI based opamp (UTBSOI-opamp) is larger than that of CMOS based opamp (CMOS-opamp).**

***Index Terms*—Opamp, sensitivity analysis, UTBSOI.**

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I. Introduction

THE operational amplifier (opamp) is a vital analog building block that is used in many circuits such as switched-capacitor filters, analog-to-digital converters, analog integrator and differentiator, etc. Many design techniques of the analog amplifiers [1]–[5] have been addressed in the literature so far. A design method, dynamic biasing (output impedance enhancement) technique [1], enhances the DC gain but reduces the settling of output [2]. The positive feedback technique [2], [3] also improves the DC gain without limiting its high-frequency performance, but here transistor matching is the main issue [6]. With the downscaling of technology nodes, the cascode topologies of the amplifiers [4], [5] have become less useful due to their limited output voltage swing [7]. Therefore, researchers are trying to achieve high DC gain by cascading or using multistage topologies operated at low bias current [8]. Fig. 1 shows the schematic of a two-stage CMOS opamp (in cascaded topology) [9], where each MOSFET is meant for accomplishing specific function. The MOSFETs M_1 and M_2 are used for differential gain acting as the input voltage to differential current converter. The M_3 and M_4 are acting as current mirror load used for recovering the differential current. The M_5 is acting as the tail current and the M_6 is acting as the voltage to current converter. Finally, M_7 is the current sink load which is acting as the current to voltage converter. The opamp in Fig. 1 is an unbuffered amplifier which is characterised by its high output impedance [9].

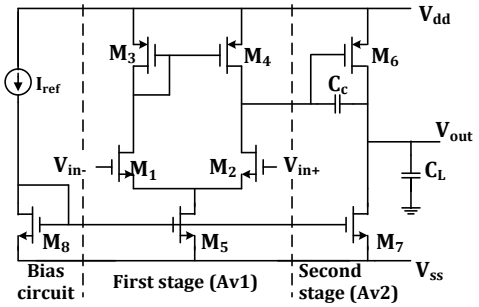

Fig. 1. Schematics showing the two-stage CMOS-opamp.

In this two-stage opamp, the design parameters are mainly the size or aspect ratio (W/L values) of M_1 through M_8 and the current flowing through M_5 and M_7. This opamp topology segregates the gain and output voltage swing requirement where the first stage provides high gain, while the second stage gives large swings. Table I shows the desired specifications of the opamp taken from different sources [9]–[12]. From the desired specifications, the W/L of the MOSFETs have been evaluated through extensive DC simulations [13]–[15] in Cadence-spectre by employing the ratio of transconductance to current consumption (g_m/I_d) methodology [14]–[17]. Table II shows the sizing (W/L) summary of the MOSFETs constituting the opamp. Keeping the same W/L of the MOSFETs [Table II], the opamp topology [Fig. 1] can be simulated at the transistor level by using the ultra-thin-body silicon-on-insulator (UTBSOI) MOSFETs, as demonstrated in [13], [14]. Fig. 2 shows the UTBSOI based opamp (UTBSOI-opamp) that can be simulated by utilizing the BSIM-IMG model [18].

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Rekib Uddin Ahmed is with the Department of Electronics and Communication Engineering, National Institute of Technology Meghalaya, Shillong 793003, India (e-mail: rekib@nitm.ac.in; phone: +919436594902).

Eklare Akshay Vijaykumar is with the Department of Electronics and Communication Engineering, National Institute of Technology Meghalaya, Shillong 793003, India (e-mail: akshayeklare@gmail.com; phone: +919077206858).

Prabir Saha is with the Department of Electronics and Communication Engineering, National Institute of Technology Meghalaya, Shillong 793003, India (e-mail: sahaprabir1@gmail.com; phone: +919485177005; fax: +91364-

TABLE I
DESIRED SPECIFICATIONS OF THE TWO-STAGE OPAMP.

Specifications	Value
Technology	180 nm
Supply voltage	$\pm$ 0.9 V
Unity-gain bandwidth (UGB)	22 MHz
Open-loop DC gain (DC gain)	78 dB
Phase margin (PM)	60°
Common mode rejection ratio (CMRR)	90 dB
Slew-rate	20 V/μs
Minimum common mode input voltage ($V_{iCM,min}$)	$-$0.1 V
Maximum common-mode input voltage ($V_{iCM,max}$)	0.8 V
Reference current (I_{ref})	20 μA
Load capacitor (C_L)	4 pF

TABLE II
SUMMARY OF THE OPAMP MOSFET'S SIZING [13].

MOSFETs	L (μm)	W (μm)
M_1, M_2	0.88	4.37
M_3, M_4	0.88	29.0
M_5	1.18	4.06
M_6	0.196	50.0
M_7	1.18	16.24
M_8	1.18	4.06

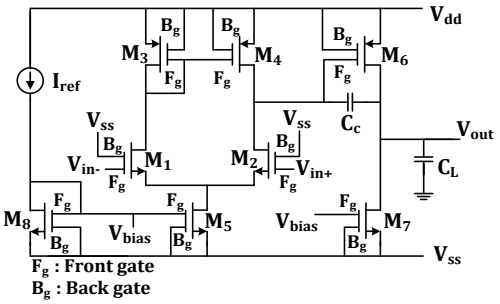

Fig. 2. Schematics showing the two-stage UTBSOI based opamp (UTBSOI-opamp).

guarantee all the desired specifications with a minimal manufacturing cost. From the practical point of view, it is not enough to achieve the desired specification for a given set of data of the component values. It is important to predict the circuit's performance by taking into account of the perturbation in the parameters of the component. So, it is necessary to know the effect on the performance of the circuit due to the perturbation as a function of its components. Any effect of the circuit's performance parameters caused by the immeasurably small perturbations in one or more parameters of the component is referred to as circuit sensitivity [19], [20]. The mathematical definition of circuit sensitivity is [20]:

$$S_x^y = \left| \frac{\Delta y}{\Delta x} \frac{x}{y} \right|. \quad (1)$$

where S_x^y is the sensitivity, x is the changing parameter of the circuit's component, and y is the circuit's function (or performance parameter). Suppose, the parameter x is the W/L of the constituent MOSFETs in an amplifier IC, and it is crucial if the circuit sensitivity with respect to change in this parameter is very large. In other words, the variation in circuit's function is large due to the change in the parameter x. It plays a dominant role in ascertaining the crucial parameters of a component. Since the design of a circuit must be carried out by choosing as many cheap components as possible without degrading the desired specifications, so it is necessary to decide which components are crucial and how much is the required value of tolerance of its parameters.

In this paper, sensitivity of the performance parameters such as DC gain, CMRR, phase margin (PM), and unity-gain bandwidth (UGB) have been analyzed with respect to the perturbation in the W/L of MOSFETs (M_1, M_2, M_6, and M_7) for the both two-stage CMOS and UTBSOI-opamp as shown in Fig. 1 and Fig. 2, respectively. Generally, due to the ageing of an IC, reliability issue like hot-carrier effect [21], [22] in the MOSFETs causes the generation of interface and oxide-trapped charges [23], [24], which in turn reduces the effective channel length of the MOSFETs. This is one of the reason why sensitivity analysis of the opamp as the function of perturbation in W/L of its constituent MOSFETs has been carried out in this paper. The channel lengths (L) of the selected MOSFETs have been changed accordingly to set $\pm$10, $\pm$20% tolerances in perturbations of the W/L values.

II. UTBSOI MOSFETs

For more than four decades, the semiconductor industries are able to provide continuous support for improvement in the performance of electronic systems due to the invention of the MOSFETs. The prediction proclaimed by Moore's law has been achieved through scaling down the MOSFETs. But for the last two decades, the scaling of bulk MOSFETs could not be continued at the same rate as predicted by Moore's law because of several limitations like physical challenges, material challenges, technological challenges, etc [25]. The channel length (L) is one of the most important parameters of the MOSFETs which is defined as the distance between source and drain. Scaling down the L degrades the transconductance of the bulk MOSFETs, the subthreshold slope (SS) [26] degrades, and the threshold voltage (V_{th}) decreases. Due to these phenomena, the device can not be turned off easily even if the gate-to-source voltage (V_{gs}) [27] is lowered below the V_{th}. It also causes leakage current due to the V_{th} reduction. These shortfalls observed in the bulk MOSFETs are collectively known as short-channel effects (SCE) [28]. Due to SCEs, characteristics of the bulk MOSFETs become increasingly sensitive to the L reduction. In addition to this, the process variation parameters of the bulk MOSFETs have become a major cause in degrading the performance of an IC. Different advanced architectures of MOSFETs [27], [29] have been put forward in the literature to overcome the limitations caused by SCEs. Out of those architectures, the dual-gated UTBSOI MOSFET as shown in Fig. 3 is the promising one [30].

The UTBSOI MOSFETs are grown over the SOI substrates with extremely uniform silicon films. The silicon substrate can be used as a back gate to bias the body [Fig. 3] provided that the thickness of the buried oxide (BO_x) is reduced [31]. Through this back gate bias, a flexibility of multiple V_{th} control can be achieved in the UTBSOI [30]. Moreover, the UTBSOI MOSFET has better scalability and superior controllability of gates over the shorter channel region [14] which

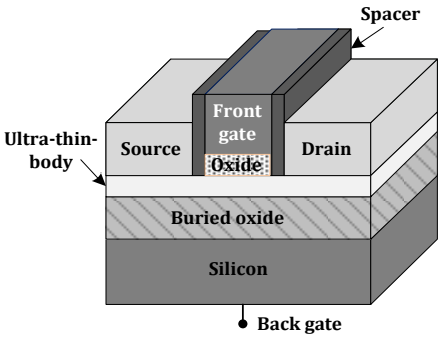

Fig. 3. Schematics showing 3D view of the UTBSOI transistor (Figure courtesy [14]).

increases the transconductance of the device. Analog, digital, or mixed signal circuits are always carefully verified through the circuit simulators, where compact models are used which represent the characteristics or conditions in the device in the form of (a) an equation, (b) an equivalent circuit, and (c) a table, together with the proper reasoning and assumptions [32]. Compact models for the semiconductor devices are very much essential for all types of electronic design and are the fundamental part of a Process-Design Kit (PDK) for a particular technology node. The PDKs consist of a set of technology definitions used to validate an IC from its desired specifications before being reproduced in silicon hardware. BSIM3 was selected as the world's first industry-standard model for the MOSFET by Compact Model Coalition (CMC) in the year 1997, and it is in the production level PDKs especially for 180 nm technology node (BSIM3v3) [27]. The BSIM-IMG [18] is an industry-standard compact model targeted for the UTBSOI MOSFETs which is under standardization by the CMC. However, the post-layout of simulation UTBSOI based circuits is not possible till date due to the non-availability of PDK in the present simulators like Cadence-spectre [33].

III. Results and Discussion

The W/L values of the constituent MOSFETs M_1, M_2, M_6, and M_7 have been chosen as the target components to study the variation in the performance parameters of the CMOS- and UTBSOI-opamps. The mentioned MOSFETs are chosen because these play a pivotal role in deciding the overall performance of the opamps unlike the other MOSFETs. The MOSFET pair M_1 and M_2 ($M_{1,2}$) contributes more to the noise and other performance parameter variation over the M_3, M_4, and M_5. Since resistance is a passive element and it is hard to implement in an IC [34], due to which the MOSFET pair M_3 and M_4 ($M_{3,4}$) are used as the load resistance in the opamp. Thus, W/L of $M_{3,4}$ pair are not considered. The M_5 mirrors the I_{ref} through it. So, change in the W/L of M_5 does not contribute to the variation of the performance parameters. The MOSFETs M_6 and M_7 forms the second stage of the opamp acting as the voltage to current converter [9]. Thus, consideration of W/L of these MOSFETs ($M_{1,2}$, M_6, and M_7) are necessary in this analysis. The method of calculating the L value for -20% tolerance in perturbation of W/L of the $M_{1,2}$ has been illustrated in Example 1.

Example 1. Referring to the Table II, W_{12} =4.37 μm and $L_{12} = 0.880$ μm. The initial aspect ratio x_i is calculated as:

$$x_i = \frac{W_{12}}{L_{12}} = \frac{4.37\mu m}{0.880\ \mu m}, \\ = 4.9659. \tag{2}$$

The following relation yields the -20% tolerance in W/L of $M_{1,2}$:

$$\frac{\Delta x}{x_i} \times 100 = -20\%. \tag{3}$$

Using the value of x_i obtained from (2) in (3) will yield $\Delta x = -0.99318$. The final value of aspect ratio x_f is calculated as:

$$x_f = x_i - 0.99318, \\ = 3.9727. \tag{4}$$

Equation (4) implies: $\frac{W}{L_{12_f}} = 3.9727$, which will give the final value of $L_{12_f} = 1.10$ μm.

Table III shows the calculated values of L to achieve the required tolerances in perturbation of W/L for the selected set of MOSFETs. However, in order to set 10% and 20% tolerances in perturbation of W/L of M_6, the calculated values of L_6 are 178 nm and 163 nm respectively, which does not satisfy for the 180 nm technology. Therefore, these values have not been considered in this analysis (illustrated in Table VI and Table VII).

TABLE III
The calculated values of L of the MOSFETs to achieve the required tolerances ($\pm 10\%$ and $\pm 20\%$) in W/L.

MOSFETs	Values of L (μm)			
	-20%	-10%	10%	20%
M_1, M_2	1.10	0.971	0.794	0.733
M_6	0.245	0.229	0.178	0.163
M_7	1.475	1.311	1.073	0.983

A summary of the simulation results of the opamps [13] are listed in Table IV. To observe the impact of the parasitic capacitance and resistance present in the CMOS-opamp, the layout is designed as shown in Fig. 4, where the open-loop and unity-gain configurations of the opamp are simulated accordingly. Some deviations have been observed between the pre- and post-layout simulation results, and the errors are listed in Table V. The reason for the errors is related to the inaccuracies associated with the parasitic components present

TABLE IV
Summary of the performance parameters achieved by the CMOS and UTBSOI-opamps with the compensation capacitor, C_c =1 pF [13]

Specifications	CMOS-opamp	UTBSOI-opamp
Technology (nm)	180	180
Supply voltage (V)	$\pm$ 0.9	$\pm$ 0.9
UGB (MHz)	19.0	15.6
DC gain (dB)	72.8	65.2
CMRR (dB)	93.4	144.2
PSRR (dB)	73.8	60.0
PM ($^\circ$)	54.5	60.0
Slew-rate (V/μs)	12.19	11.24
Power (mW)	0.189	0.181

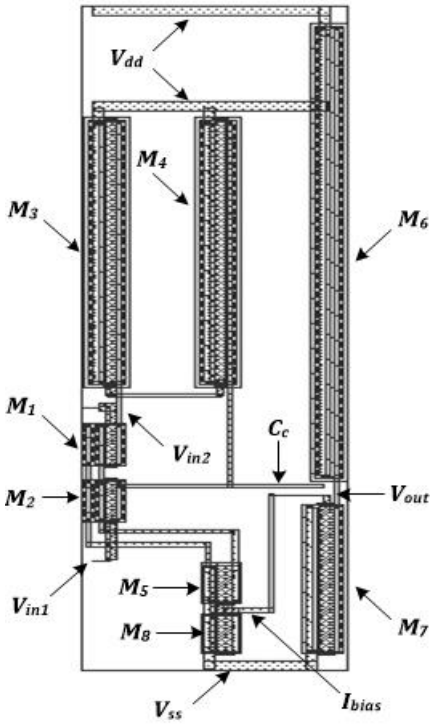

Fig. 4. Extracted layout view of the CMOS-opamp.

TABLE V
SUMMARY OF POST-LAYOUT SIMULATION RESULTS OF CMOS-OPAMP.

Specifications	Pre-layout (as given in Table IV)	Post-layout results	Error (%)
UGB (MHz)	19.0	18.98	−0.10
PM (°)	54.5	55.02	0.95
DC gain (dB)	72.8	73.57	1.05
CMRR (dB)	93.4	77.73	−16.78
Power (mW)	0.189	0.188	0.529
Area (mm^2)	-	1.569×10^{-3}	-

The minus sign (−) signifies the decrease in performance parameter in post-layout simulation.

in the layout. The C_c (=1 pF) present in the CMOS-opamp is hard to include in the layout design since it requires large a channel length and width which exceeds 30 μm for a metal insulator metal capacitor (mimcap). That is why, the C_c has been connected outside the circuit. The area of the CMOS-opamp extracted from the layout design is 1.569×10^{-3} mm^2.

The performance parameters observed for different values of tolerances of perturbation in W/L of $M_{1,2}$, M_6, and M_7 are given in Table VI (shown at the next page). The sensitivity of DC gain, CMRR, PM, and UGB with respect to the perturbation in W/L of the MOSFETs is computed in the MATLAB encoded through Algorithm 1. Table VII shows the sensitivity values of the UTBSOI-opamp obtained in this analysis. The same can also be obtained for the CMOS-opamp using the Algorithm 1.

Comparison charts showing the sensitivity of UTBSOI-opamp in terms of DC gain, CMRR, PM, and UGB are shown in Fig. 5. In the UTBSOI-opamp, the DC gain is least sensitive towards the perturbation in W/L of $M_{1,2}$ [Fig. 5(a)]. A large DC gain sensitivity (∼3.1249) [Table VII] is observed for the

Algorithm 1: Algorithm to compute the sensitivity.

Require: W, L, L_f, $y[\,]$, $y_{new}[\,]$
Ensure: Sensitivity values (S) of DC gain, CMRR, PM, and UGB.
$\{W \rightarrow$ Channel width, $l \rightarrow$ Initial channel length [Table II]
$L_f \rightarrow$ Final channel lengths [Table III]
$y \rightarrow$ Initial performance parameters [Table IV]
$y_{new} \rightarrow$ Final performance parameters [Table VI]$\}$
1: **Start**
2: **repeat**
3: $x \leftarrow W/l$
4: $i \leftarrow 1$
5: **while** $i \leq$LENGTH(L_f) **do**
6: $x_{new}[i] \leftarrow W/L_f[i]$
7: $\Delta x[i] \leftarrow x_{new}[i] - x$ {Perturbation in aspect-ratio of MOSFETs}
8: $\Delta y[i] \leftarrow y_{new}[i] - y$
9: $S[i] \leftarrow \mid (x/y) \times (\Delta y[i]/\Delta x[i]) \mid$
10: **end while**
11: **until** Sensitivity values (S) of DC gain, CMRR, PM, and UGB are obtained.

TABLE VII
SENSITIVITY VALUES OF DC GAIN, CMRR, PM, AND UGB OF THE UTBSOI-OPAMP WITH RESPECT TO THE TOLERANCES OF PERTURBATION IN W/L OF THE SELECTED MOSFETS.

Perturbation in W/L of $M_{1,2}$

Performance parameters	UTBSOI-opamp −20%	−10%	10%	20%
DC gain (dB)	0.0008	0.0360	0.0283	0.0665
CMRR (dB)	0.2382	0.2516	0.3201	0.3818
PM (°)	0.0783	0.1014	0.1323	0.1687
UGB (MHz)	0.2147	0.2052	0.3669	0.4059

Perturbation in W/L of M_6

Performance parameters	UTBSOI-opamp −20%	−10%	10%	20%
DC gain (dB)	2.8474	3.1249	–	–
CMRR (dB)	0.2174	0.2257	–	–
PM (°)	0.9600	1.2549	–	–
UGB (MHz)	1.4391	1.9484	–	–

Perturbation in W/L of M_7

Performance parameters	UTBSOI-opamp −20%	−10%	10%	20%
DC gain (dB)	0.8106	0.9731	1.8149	1.9692
CMRR (dB)	0.0170	0.0187	0.0243	0.0446
PM (°)	0.7975	0.9390	0.9894	0.5821
UGB (MHz)	1.6282	1.6230	2.1856	1.4938

Tolerance (%) in perturbation of W/L: −20, −10, 10, 20

10% tolerance of perturbation in W/L of M_6 [Fig. 5(a)]. This also implies that the W/L of M_6 can be changed accordingly in order to increase the DC gain. The CMRR is more sensitive towards the perturbation in W/L of $M_{1,2}$ and least towards that of M_7 [Fig. 5(b)]. The PM is more sensitive towards the perturbation in W/L of M_7 [Fig. 5(c)] and UGB is more sensitive towards the perturbation in W/L of M_6 [Fig. 5(d)]. The same goes for the sensitivity analysis performed over

TABLE VI
THE DC GAIN, CMRR, PM, AND UGB OF THE CMOS-OPAMP AND UTBSOI-OPAMP WITH RESPECT TO THE TOLERANCES OF PERTURBATION IN W/L OF THE SELECTED MOSFETS.

Perturbation in W/L of $M_{1,2}$

Performance parameters	CMOS-opamp				UTBSOI-opamp			
	-20%	-10%	10%	20%	-20%	-10%	10%	20%
DC gain (dB)	73.31	72.99	72.69	72.53	65.19	64.98	65.40	66.07
CMRR (dB)	93.84	93.52	93.29	93.16	137.33	140.80	149.20	155.24
PM (°)	55.12	55.31	53.73	53.14	60.94	60.57	59.14	57.97
UGB (MHz)	19.14	19.02	19.98	20.35	14.93	15.30	16.22	16.87

Perturbation in W/L of M_6

Performance parameters	CMOS-opamp				UTBSOI-opamp			
	-20%	-10%	10%	20%	-20%	-10%	10%	20%
DC gain (dB)	51.39	54.35	–	–	102.33	94.56	–	–
CMRR (dB)	93.43	93.43	–	–	137.98	139.51	–	–
PM (°)	59.8	58.40	–	–	48.48	49.15	–	–
UGB (MHz)	15.56	16.65	–	–	20.09	19.98	–	–

Perturbation in W/L of M_7

Performance parameters	CMOS-opamp				UTBSOI-opamp			
	-20%	-10%	10%	20%	-20%	-10%	10%	20%
DC gain (dB)	74.79	74.79	65.15	53.02	54.63	58.86	77.00	90.93
CMRR (dB)	93.43	93.43	93.43	93.43	143.71	143.93	144.55	145.49
PM (°)	53.03	52.02	56.37	63.42	69.57	54.37	54.08	53.0
UGB (MHz)	19.31	19.31	19.07	16.53	10.52	13.07	19.00	20.27

Tolerance (%) in perturbation of W/L: -20, -10, 10, 20

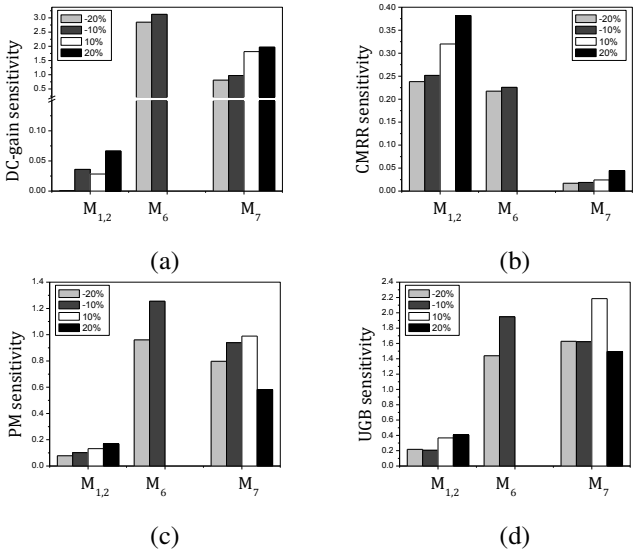

Fig. 5. Sensitivity of different parameters of the UTBSOI-opamp in the open-loop configuration with respect tolerances of perturbation in the aspect ratio (W/L) of $M_{1,2}$, M_6, and M_7 (a) DC gain, (b) CMRR, (c) PM, (d) UGB.

CMOS-opamp. Whereas, it is observed from the Table VI, that the variations in performance parameters of the UTBSOI-opamp due to the perturbation in W/L are larger than that of the CMOS-opmap.

IV. CONCLUSION

The designs of CMOS and UTBSOI-opamps discussed in this paper are simulated in Cadence-spectre through the use of BSIM3v3 and BSIM-IMG models respectively. Moreover, the post-layout simulation has also been considered for the CMOS-opamp. The simulation has been carried out to study the sensitivity of the performance parameters of the opamps as the function of the perturbation in W/L values of the constituent MOSFETs. From the sensitivity analysis, it is concluded that the W/L of M_6 is the crucial parameter for deciding the DC gain and PM. The UGB and CMRR are more sensitive towards the W/L of M_7 and $M_{1,2}$ respectively. The sensitivity observed in UTBSOI-opamp towards the perturbation of W/L of the constituent MOSFETs is higher than that of CMOS-opamp. Analytical modeling of the sensitivity of performance parameters of the opamps as the function of perturbation in W/L would be a welcome step towards the work presented in this paper.

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Preparation of Papers for Electronics (September 2011)

First A. Author, Second B. Author, and Third C. Author

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F. A. Author is with the Faculty of Electrical Engineering, University of Banja Luka, Banja Luka, Bosnia and Herzegovina (corresponding author to provide phone: +387-51-222-333; fax: +387-51-111-222; e-mail: author@et-fbl.net).

S. B. Author was with Faculty of Technical Sciences, University of Novi Sad, Novi Sad, Serbia. He is now with the Institute "Mihailo Pupin", Belgrade, Serbia (e-mail: author@pupin.rs).

T. C. Author is with the School of Electrical Engineering, University of Belgrade, Belgrade, Serbia, on leave from the Faculty of Electronic Engineering, University of Niš, Niš, Serbia (e-mail: author@elfak.ni.ac.rs).

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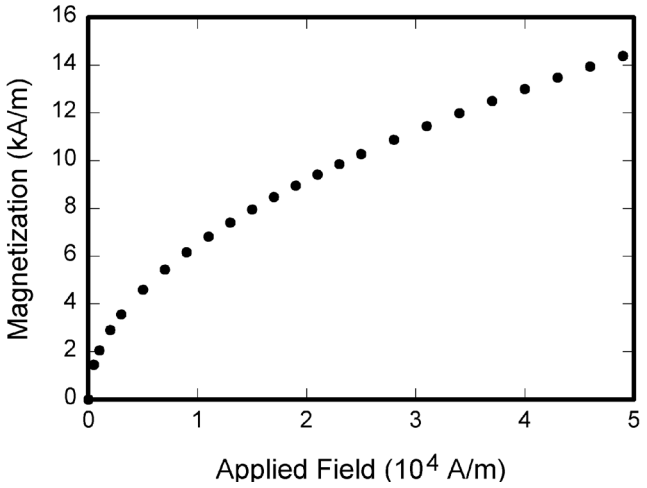

Fig. 1. Magnetization as a function of applied field. Note that "Fig." is abbreviated. There is a period after the figure number, followed by two spaces. It is good practice to explain the significance of the figure in the caption.

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Use either SI (MKS) or CGS as primary units. (SI units are strongly encouraged.) English units may be used as secondary units (in parentheses). **This applies to papers in data storage.** For example, write "15 Gb/cm^2 (100 Gb/in^2)." An exception is when English units are used as identifiers in trade, such as "3½-in disk drive." Avoid combining SI and CGS units, such as current in amperes and magnetic field in oersteds. This often leads to confusion because equations do not balance dimensionally. If you must use mixed units, clearly state the units for each quantity in an equation.

The SI unit for magnetic field strength H is A/m. However, if you wish to use units of T, either refer to magnetic flux density B or magnetic field strength symbolized as $\mu_0 H$. Use the center dot to separate compound units, e.g., "A·m^2."

TABLE I
Units for Magnetic Properties

Symbol	Quantity	Conversion from Gaussian and CGS EMU to SI [a]
Φ	magnetic flux	1 Mx $\rightarrow 10^{-8}$ Wb = 10^{-8} V·s
B	magnetic flux density, magnetic induction	1 G $\rightarrow 10^{-4}$ T = 10^{-4} Wb/m^2
H	magnetic field strength	1 Oe $\rightarrow 10^3/(4\pi)$ A/m
m	magnetic moment	1 erg/G = 1 emu $\rightarrow 10^{-3}$ A·m^2 = 10^{-3} J/T
M	magnetization	1 erg/(G·cm^3) = 1 emu/cm^3 $\rightarrow 10^3$ A/m
$4\pi M$	magnetization	1 G $\rightarrow 10^3/(4\pi)$ A/m
σ	specific magnetization	1 erg/(G·g) = 1 emu/g $\rightarrow$ 1 A·m^2/kg
j	magnetic dipole moment	1 erg/G = 1 emu $\rightarrow 4\pi \times 10^{-10}$ Wb·m
J	magnetic polarization	1 erg/(G·cm^3) = 1 emu/cm^3 $\rightarrow 4\pi \times 10^{-4}$ T
χ, κ	susceptibility	1 $\rightarrow 4\pi$
χ_ρ	mass susceptibility	1 cm^3/g $\rightarrow 4\pi \times 10^{-3}$ m^3/kg
μ	permeability	1 $\rightarrow 4\pi \times 10^{-7}$ H/m = $4\pi \times 10^{-7}$ Wb/(A·m)
μ_r	relative permeability	$\mu \rightarrow \mu_r$
w, W	energy density	1 erg/cm^3 $\rightarrow 10^{-1}$ J/m^3
N, D	demagnetizing factor	1 $\rightarrow 1/(4\pi)$

Vertical lines are optional in tables. Statements that serve as captions for the entire table do not need footnote letters.

[a]Gaussian units are the same as cgs emu for magnetostatics; Mx = maxwell, G = gauss, Oe = oersted; Wb = weber, V = volt, s = second, T = tesla, m = meter, A = ampere, J = joule, kg = kilogram, H = henry.

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Multipliers can be especially confusing. Write "Magnetization (kA/m)" or "Magnetization (10^3 A/m)." Do not write "Magnetization (A/m) x 1000" because the reader would not know whether the top axis label in Fig. 1 meant 16000 A/m or 0.016 A/m. Figure labels should be legible, approximately 8 to 12 point type.

B. References

Number citations consecutively in square brackets [1]. The sentence punctuation follows the brackets [2]. Multiple references [2], [3] are each numbered with separate brackets [1]–[3]. When citing a section in a book, please give the relevant page numbers [2]. In sentences, refer simply to the reference number, as in [3]. Do not use "Ref. [3]" or "reference [3]" except at the beginning of a sentence: "Reference [3] shows ... ." Please do not use automatic endnotes in *Word*, rather, type the reference list at the end of the paper using the "References" style.

Number footnotes separately in superscripts (Insert | Footnote).[1] Place the actual footnote at the bottom of the column in which it is cited; do not put footnotes in the reference list (endnotes). Use letters for table footnotes (see Table I).

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$$\int_0^{r_2} F(r,\varphi)\,\mathbf{d}\,d\varphi = [\sigma r_2/(2\mu_0)] \cdot \int_0^{\infty} \exp(-\lambda\,|z_j - z_i|)\,\lambda^{-1} J_1(\lambda r_2)\,J_0(\lambda r_i)\,d\lambda\,. \tag{1}$$

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E. Other Recommendations

Use one space after periods and colons. Hyphenate complex modifiers: "zero-field-cooled magnetization." Avoid dangling participles, such as, "Using (1), the potential was calculated." [It is not clear who or what used (1).] Write instead, "The potential was calculated by using (1)," or "Using (1), we calculated the potential."

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[1] It is recommended that footnotes be avoided (except for the unnumbered footnote with the receipt date and authors' affiliations on the first page). Instead, try to integrate the footnote information into the text.

VI. Some Common Mistakes

The word "data" is plural, not singular. The subscript for the permeability of vacuum μ_0 is zero, not a lowercase letter "o." The term for residual magnetization is "remanence"; the adjective is "remanent"; do not write "remnance" or "remnant." Use the word "micrometer" instead of "micron." A graph within a graph is an "inset," not an "insert." The word "alternatively" is preferred to the word "alternately" (unless you really mean something that alternates). Use the word "whereas" instead of "while" (unless you are referring to simultaneous events). Do not use the word "essentially" to mean "approximately" or "effectively." Do not use the word "issue" as a euphemism for "problem." When compositions are not specified, separate chemical symbols by en-dashes; for example, "NiMn" indicates the intermetallic compound $Ni_{0.5}Mn_{0.5}$ whereas "Ni–Mn" indicates an alloy of some composition Ni_xMn_{1-x}.

Be aware of the different meanings of the homophones "affect" (usually a verb) and "effect" (usually a noun), "complement" and "compliment," "discreet" and "discrete," "principal" (e.g., "principal investigator") and "principle" (e.g., "principle of measurement"). Do not confuse "imply" and "infer."

Prefixes such as "non," "sub," "micro," "multi," and "ultra" are not independent words; they should be joined to the words they modify, usually without a hyphen. There is no period after the "et" in the Latin abbreviation "*et al.*" (it is also italicized). The abbreviation "i.e.," means "that is," and the abbreviation "e.g.," means "for example" (these abbreviations are not italicized).

An excellent style manual and source of information for science writers is [9].

VII. Editorial Policy

Each manuscript submitted is subjected to the following review procedure:

- It is reviewed by the editor for general suitability for this publication
- If it is judged suitable, two reviewers are selected and a single-blinded review process takes place
- Based on the recommendations of the reviewers, the editor then decides whether the particular paper should be accepted as is, revised or rejected.

Do not submit a paper you have submitted or published elsewhere. Do not publish "preliminary" data or results. The submitting author is responsible for obtaining agreement of all coauthors and any consent required from sponsors before submitting a paper. It is the obligation of the authors to cite relevant prior work.

Every paper submitted to "Electronics" journal are single-blind reviewed. For conference-related papers, the decision to accept or reject a paper is made by the conference editors and publications committee; the recommendations of the referees are advisory only. Undecipherable English is a valid reason for rejection.

VIII. Publication Principles

The contents of "Electronics" are peer-reviewed and archival. The "Electronics" publishes scholarly articles of archival value as well as tutorial expositions and critical reviews of classical subjects and topics of current interest.

Authors should consider the following points:

1) Technical papers submitted for publication must advance the state of knowledge and must cite relevant prior work.
2) The length of a submitted paper should be commensurate with the importance, or appropriate to the complexity, of the work. For example, an obvious extension of previously published work might not be appropriate for publication or might be adequately treated in just a few pages.
3) Authors must convince both peer reviewers and the editors of the scientific and technical merit of a paper; the standards of proof are higher when extraordinary or unexpected results are reported.
4) Because replication is required for scientific progress, papers submitted for publication must provide sufficient information to allow readers to perform similar experiments or calculations and use the reported results. Although not everything need be disclosed, a paper must contain new, useable, and fully described information. For example, a specimen's chemical composition need not be reported if the main purpose of a paper is to introduce a new measurement technique. Authors should expect to be challenged by reviewers if the results are not supported by adequate data and critical details.
5) Papers that describe ongoing work or announce the latest technical achievement, which are suitable for presentation at a professional conference, may not be appropriate for publication in "Electronics".

IX. Conclusion

A conclusion section is not required. Although a conclusion may review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions.

Appendix

Appendixes, if needed, appear before the acknowledgment.

Acknowledgment

The preferred spelling of the word "acknowledgment" in American English is without an "e" after the "g." Use the singular heading even if you have many acknowledgments. Avoid expressions such as "One of us (S.B.A.) would like to thank ... ." Instead, write "F. A. Author thanks ... ." **Sponsor and financial support acknowledgments are placed in the unnumbered footnote on the first page, not here.**

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